RCA

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Linear Integrated Circuits

RCA
Linear Integrated Circuits

This DATABOOK contains complete technical information on the full line of RCA standard commercial linear integrated circuits and MOS field-effect transistors for both industrial and consumer applications. An Index to Devices provides a complete listing of types, together with an indication of package options available for each of them.

The pages immediately following the Index to Devices include photographs of the packages used for RCA linear integrated circuits and MOS/FET's, a product-classification chart, recommended operating and handling considerations, a list of special terms and symbols used in the characterization of RCA linear integrated circuits and MOS/FET's, and a cross-reference directory that indicates RCA types recommended as direct replacements for other manufacturers' types.

Three separate data sections provide definitive ratings and electrical characteristics for (1) Linear Integrated Circuits for Industrial Applications, (2) Linear Integrated Circuits for Consumer Applications, and (3) MOS Field-Effect Transistors (MOS/FET's). Data pages for individual devices are included as nearly as possible in alpha-numerical sequence of type numbers. Because some devices are grouped together to show similarity of function or data, individual type numbers may be out of sequence. If you don't find the data on a specific type where you expect it to be, check the Index to Devices.

The DATABOOK also includes dimensional outlines for all currently available packages and selected RCA Application Notes on RCA Linear Integrated Circuits and MOS/FET's.

Table of Contents

Page
Index to Devices 3
Packages 5
Product Classification Chart 7
Operating and Handling Considerations 8
Terms and Symbols 10
Cross-Reference Directory 12
Linear Integrated Circuits for Industrial Applications—Technical Data 17
Linear Integrated Circuits for Consumer Applications—Technical Data 291
MOS Field-Effect Transistors—Technical Data 433
Dimensional Outlines 475
Application Notes 483
RCA Sales Offices, Manufacturers' Representatives, and Authorized Distributors 559

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The device data shown for some types are indicated as preliminary. **Preliminary data** are intended for guidance purposes in evaluating devices for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. For current information on the status of preliminary programs, please contact your local RCA sales office.

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Printed in USA/11-78

Index to Devices — Linear IC's

Type Number	Package Suffix						Data Bulletin File No.	Page
CA101	T	S	—	—	—	—	786	18
CA101A	T	S	G	—	—	—	786	18
CA107	T	S	G	—	—	—	785	22
CA111	T	S	G	—	—	—	797	25
CA124	E	G	—	—	—	—	796	29
CA139	E	G	—	—	—	—	795	32
CA139A	E	G	—	—	—	—	795	32
CA158	T	S	G	—	—	—	1019	35
CA158A	T	S	G	—	—	—	1019	35
CA201	T	S	—	—	—	—	786	18
CA201A	T	S	G	—	—	—	786	18
CA207	T	S	G	—	—	—	785	22
CA211	T	S	G	—	—	—	797	25
CA224	E	G	—	—	—	—	796	29
CA239	E	G	—	—	—	—	795	32
CA239A	E	G	—	—	—	—	795	32
CA258	T	S	G	—	—	—	1019	35
CA258A	T	S	G	—	—	—	1019	35
CA270	W	—	—	—	—	—	879E	292
CA301A	T	S	E*	G	H	—	786	18
CA307	T	S	E*	G	H	—	785	22
CA311	T	S	E*	G	—	—	797	25
CA324	E	G	H	GH	—	—	796	29
CA339	E	G	H	GH	—	—	795	32
CA339A	E	G	—	—	—	—	795	32
CA358	T	S	G	H	GH	—	1019	35
CA358A	T	S	G	—	—	—	1019	35
CA555	T	S	E*	G	—	—	834	42
CA555C	T	S	E*	G	H	—	834	42
CA723	T	E	—	—	—	—	788	46
CA723C	T	E	H	—	—	—	788	46
CA741	T	S	E*	G	L	—	531	50
CA741C	T	S	E*	G	H	GH	531	50
CA747	T	E	G	—	—	—	531	50
CA747C	T	E	G	H	GH	—	531	50
CA748	T	S	E*	G	—	—	531	50
CA748C	T	S	E*	G	H	GH	531	50
CA758	E	—	—	—	—	—	760	295
CA810	Q	QM	—	—	—	—	1154	298
CA810A	Q	QM	—	—	—	—	1154	298
CA920	E	—	—	—	—	—	1132	301
CA1190	Q	—	—	—	—	—	1155	303
CA1310	E	—	—	—	—	—	761	306
CA1352	E	—	—	—	—	—	961	309
CA1391	E*	—	—	—	—	—	981	310
CA1394	E*	—	—	—	—	—	981	310
CA1398	E	—	—	—	—	—	686	312
CA1458	T	S	E*	G	H	GH	531	50
CA1541	D	H	—	—	—	—	536	54
CA1558	T	S	E*	G	—	—	531	50
CA2002	⊕	M	—	—	—	—	1156	314
CA2004	⊕	M	—	—	—	—	1105	317
CA2111A	E	Q	—	—	—	—	612	57
CA2904	G	—	—	—	—	—	1019	35
CA3000	■	H	—	—	—	—	121	59
CA3001	■	H	—	—	—	—	122	61
CA3002	■	H	—	—	—	—	123	64
CA3004	■	H	—	—	—	—	124	66
CA3005	■	H	—	—	—	—	125	69
CA3006	■	—	—	—	—	—	125	69

Type Number	Package Suffix						Data Bulletin File No.	Page
CA3007	■	—	—	—	—	—	126	72
CA3008	▲	—	—	—	—	—	316	74
CA3008A	▲	—	—	—	—	—	310	78
CA3010	■	—	—	—	—	—	316	74
CA3010A	■	—	—	—	—	—	310	78
CA3011	■	—	—	—	—	—	128	82
CA3012	■	H	—	—	—	—	128	82
CA3013	■	—	—	—	—	—	129	84
CA3014	■	—	—	—	—	—	129	84
CA3015	■	L	H	—	—	—	316	74
CA3015A	■	—	—	—	—	—	310	78
CA3016	▲	—	—	—	—	—	316	74
CA3016A	▲	—	—	—	—	—	310	78
CA3018	■	L	H	—	—	—	338	87
CA3018A	■	—	—	—	—	—	338	87
CA3019	■	H	—	—	—	—	236	90
CA3020	■	H	—	—	—	—	339	92
CA3020A	■	—	—	—	—	—	339	92
CA3021	■	—	—	—	—	—	243	96
CA3022	■	—	—	—	—	—	243	96
CA3023	■	H	—	—	—	—	243	96
CA3026	■	H	—	—	—	—	338	99
CA3028A	■	S	L	—	H	—	382	103
CA3028B	■	S	—	—	—	—	382	103
CA3029	•	—	—	—	—	—	316	74
CA3029A	•	—	—	—	—	—	310	78
CA3030	•	—	—	—	—	—	316	74
CA3030A	•	—	—	—	—	—	310	78
CA3035	■	VI	H	—	—	—	274	319
CA3036	■	—	—	—	—	—	275	108
CA3037	†	—	—	—	—	—	316	74
CA3037A	†	—	—	—	—	—	310	78
CA3038	†	—	—	—	—	—	316	74
CA3038A	†	—	—	—	—	—	310	78
CA3039	■	L	H	—	—	—	343	109
CA3040	■	—	—	—	—	—	363	111
CA3041	♁	—	—	—	—	—	318	320
CA3042	♁	—	—	—	—	—	319	323
CA3043	■	H	—	—	—	—	331	326
CA3044	■	VI	—	—	—	—	340	328
CA3045	†	F	L	H	—	—	341	114
CA3046	†	—	—	—	—	—	341	114
CA3048	•	—	—	—	—	—	377	117
CA3049	T	L	H	—	—	—	611	120
CA3050	†	—	—	—	—	—	361	124
CA3051	•	—	—	—	—	—	361	124
CA3052	•	—	—	—	—	—	387	331
CA3053	■	S	—	—	—	—	382	103
CA3054	•	L	H	—	—	—	388	99
CA3058	†	—	—	—	—	—	490	127
CA3059	•	H	—	—	—	—	490	127
CA3060	D	E	H	—	—	—	537	132
CA3060A	D	—	—	—	—	—	537	132
CA3060B	D	—	—	—	—	—	537	132
CA3064	E	—	—	—	—	—	396	335
CA3065	♁	—	—	—	—	—	412	337
CA3066	♁	—	—	—	—	—	466	340
CA3067	♁	—	—	—	—	—	466	340
CA3068	♁	—	—	—	—	—	467	343
CA3070	•	—	—	—	—	—	468	345

Index to Devices — Linear IC's

Type Number	Package Suffix						Data Bulletin File No.	Page
CA3071	•	—	—	—	—	—	468	345
CA3072	•	—	—	—	—	—	468	345
CA3075	♠	H	—	—	—	—	429	138
CA3076	■	H	—	—	—	—	430	140
CA3078	T	S	—	H	—	—	535	142
CA3078A	T	S	—	—	—	—	535	142
CA3079	•	—	—	—	—	—	490	127
CA3080	■	E*	S	H	—	—	475	146
CA3080A	■	E*	S	—	—	—	475	146
CA3081	•	F	H	—	—	—	480	152
CA3082	•	F	H	—	—	—	480	152
CA3083	•	F	L	H	—	—	481	154
CA3084	•	L	H	—	—	—	482	156
CA3085	■	E*	S	L	H	—	491	159
CA3085A	■	S	E*	—	—	—	491	159
CA3085B	■	S	—	—	—	—	491	159
CA3086	•	F	—	—	—	—	483	162
CA3088	E	—	—	—	—	—	560	352
CA3089	E	—	—	—	—	—	561	354
CA3090A	Q	—	—	—	—	—	684	357
CA3091	D	H	—	—	—	—	534	164
CA3093	E	H	—	—	—	—	533	170
CA3094	T	S	E*	H	—	—	598	173
CA3094A	T	S	E*	—	—	—	598	173
CA3094B	T	S	—	—	—	—	598	173
CA3095	E	H	—	—	—	—	591	181
CA3096	E	H	—	—	—	—	595	186
CA3096A	E	—	—	—	—	—	595	186
CA3096C	E	—	—	—	—	—	595	186
CA3097	E	H	—	—	—	—	633	193
CA3098	T	S	E*	H	—	—	896	199
CA3099	E	H	—	—	—	—	620	203
CA3100	T	S	F	H	—	—	625	206
CA3102	E	H	—	—	—	—	611	120
CA3118	T	H	—	—	—	—	532	210
CA3118A	T	—	—	—	—	—	532	210
CA3120	E	—	—	—	—	—	907	359
CA3121	E	—	—	—	—	—	688	363
CA3123	E	—	—	—	—	—	631	367
CA3125	E	—	—	—	—	—	685	369
CA3126	Q	—	—	—	—	—	860	370
CA3127	E	—	—	—	—	—	662	215
CA3128	Q	—	—	—	—	—	1161	372
CA3130	T	S	E*	H	—	—	817	218
CA3130A	T	S	E*	—	—	—	817	218
CA3130B	T	S	—	—	—	—	817	218
CA3131	EM	—	—	—	—	—	1157	373
CA3132	EM	—	—	—	—	—	1157	373
CA3134	G	GM	GQM	—	—	—	1097	374
CA3135	G	—	—	—	—	—	1021	378

Type Number	Package Suffix						Data Bulletin File No.	Page
CA3136	E	—	—	—	—	—	1158	383
CA3137	E	—	—	—	—	—	970	386
CA3138	G	GH	—	—	—	—	1131	228
CA3138A	G	—	—	—	—	—	1131	228
CA3139	E	Q	—	—	—	—	905	390
CA3140	T	S	E*	H	—	—	957	230
CA3140A	T	S	E*	—	—	—	957	230
CA3140B	T	S	—	—	—	—	957	230
CA3141	E	—	—	—	—	—	906	242
CA3142	E	—	—	—	—	—	907	359
CA3143	E	—	—	—	—	—	1138	393
CA3144	G	—	—	—	—	—	1137	395
CA3146	E	H	—	—	—	—	532	210
CA3146A	E	—	—	—	—	—	532	210
CA3151	G	—	—	—	—	—	1160	399
CA3153	G	—	—	—	—	—	1142	402
CA3159	G	—	—	—	—	—	1136	408
CA3160	T	S	E*	H	—	—	976	244
CA3160A	T	S	E*	—	—	—	976	244
CA3160B	T	S	—	—	—	—	976	244
CA3161	E	—	—	—	—	—	1079	256
CA3162	E	—	—	—	—	—	1080	258
CA3163	G	—	—	—	—	—	1092	410
CA3164	E	—	—	—	—	—	1139	262
CA3166	E	—	—	—	—	—	1110	412
CA3168	E	—	—	—	—	—	1140	415
CA3170	E	—	—	—	—	—	1129	417
CA3172	G	—	—	—	—	—	1130	420
CA3183	E	H	—	—	—	—	532	210
CA3183A	E	—	—	—	—	—	532	210
CA3189	E	—	—	—	—	—	1046	422
CA3221	G	—	—	—	—	—	1057	427
CA3240	E*	E1§	—	—	—	—	1050	265
CA3240A	E*	E1§	—	—	—	—	1050	265
CA3290	T	S	E*	E1§	—	—	1049	274
CA3290A	T	S	E*	E1§	—	—	1049	274
CA3290B	T	S	—	—	—	—	1049	274
CA3401	E	G	H	GH	—	—	630	280
CA3600	E	—	—	—	—	—	619	282
CA3724	G	GH	—	—	—	—	884	287
CA3725	G	GH	—	—	—	—	884	287
CA6078A	T	S	H	—	—	—	592	289
CA6741	T	S	—	—	—	—	592	289

■ No designated suffix letter for this type in TO-5-style package

▲ No designated suffix letter for this type in ceramic flat package

• No designated suffix letter for this type in dual-in-line plastic package

† No designated suffix letter for this type in dual-in-line ceramic package

♠ No designated suffix letter for this type in quad-in-line plastic package

* In 8-lead dual-in-line Mini-DIP package

§ In 14-lead dual-in-line plastic package

⊕ No designated suffix letter for this type in TO-220-style package with vertical-mount lead form

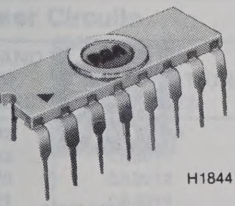
Index to Devices — MOS/FET's

Type Number	Package	Data Bulletin File No.	Page
3N128	TO-72	309	434
3N138	TO-72	283	436
3N139	TO-72	284	437
3N140	TO-72	285	438
3N141	TO-72	285	438
3N142	TO-72	286	441
3N143	TO-72	309	434
3N152	TO-72	314	442
3N153	TO-72	320	443
3N154	TO-72	335	444
3N159	TO-72	336	459
3N187	TO-72	326	446
3N200	TO-72	436	450
3N204	TO-72	959	453
3N205	TO-72	959	453
3N206	TO-72	959	453
3N211	TO-72	875	458

Type Number	Package	Data Bulletin File No.	Page
3N212	TO-72	875	458
3N213	TO-72	875	458
40467A	TO-72	324	462
40468A	TO-72	323	463
40559A	TO-72	323	463
40600	TO-72	333	464
40601	TO-72	333	464
40602	TO-72	333	464
40603	TO-72	334	465
40604	TO-72	334	465
40673	TO-72	381	466
40819	TO-72	463	467
40820	TO-72	464	468
40821	TO-72	464	468
40822	TO-72	465	470
40823	TO-72	465	470
40841	TO-72	489	471

Packages

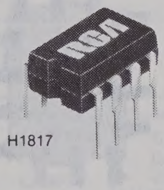
D Suffix
Dual-In-Line Welded-Seal Ceramic Package



H1844

14 and 16-lead versions

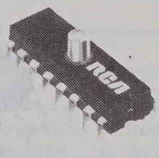
E Suffix
Dual-In-Line Plastic Package



H1817

8, 14, and 16-lead versions

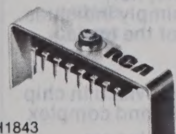
E Suffix
Power Stud Plastic Dual-In-Line Package



H1828

CA3134E only

EM Suffix
Modified 16-lead Dual-In-Line Plastic Package



H1843

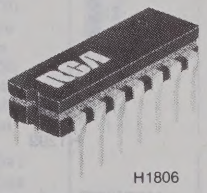
CA3134EM only

EM Suffix
Modified 16-lead Dual-In-Line Plastic Package

H1827

CA3131EM, CA3132EM only

F Suffix
Dual-In-Line Frit-Seal Ceramic Package

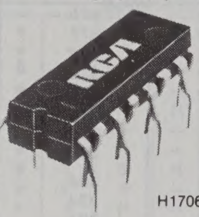


H1806

14 and 16-lead versions

Packages

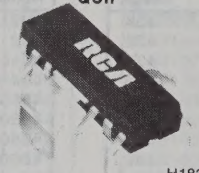
Q Suffix
Quad-in-Line Plastic Package (QUIP)



H1706

14 and 16-lead versions

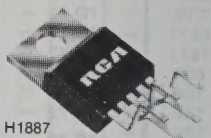
Q Suffix
Modified 16-lead QUIP



H1825

CA810Q, CA810AQ, and CA1190Q only
(A flat wing-tab version, QM suffix is also available for the CA810, CA810A).

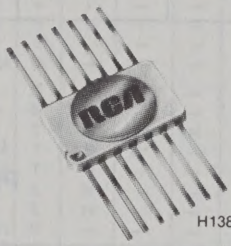
VERSA-V TO-220 Style Plastic Package with Vertical-Mount Lead Form



H1887

CA2002, CA2004 only
(Versions with Horizontal-Mount Lead Form—CA2002M and CA2004M are also available)

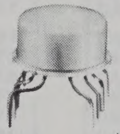
K Suffix
Ceramic Flat Package



H1383R1

14-lead version

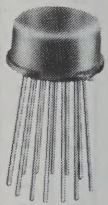
S Suffix
TO-5 Style Package with Dual-In-Line Formed Leads (DIL-CAN)



H1787

8-lead version

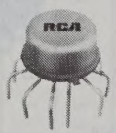
T Suffix
TO-5 Style Package with Straight Leads



H1463

8, 10, and 12-lead versions

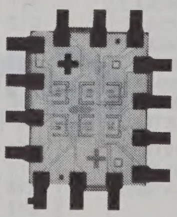
V1 Suffix
TO-5 Style Package with Radial Formed Leads



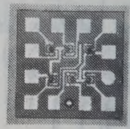
H1561

8, 10, and 12-lead versions

L Suffix
Beam-Lead

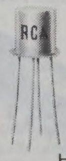


H Suffix
Chip



92CS-22137

JEDEC TO-72



H1299

MOS/FET's only

Notes:

1. Some types may have an additional "M" suffix following the package designation suffix, i.e., CA3131EM. The additional "M" suffix simply indicates that the device is a mechanical variant of the basic package type.

2. RCA Linear integrated circuits are provided in chip form to allow customer design of special and complex circuits to suit individual needs. Linear chips are electrically identical to and offer the features of their counterparts, sealed in ceramic, TO-5, and plastic packages.

Product Classification Chart

Industrial Circuits

OPERATIONAL AMPLIFIERS				DIFFERENTIAL AMPLIFIERS	ARRAYS		
General Purpose		General Purpose Wideband	Variable		Amplifier/ Diode	Transistor	
Single Unit	Dual Unit	Single Unit	High Current	CA3000	Amplifier	CA3018	CA3095
CA101	CA158	CA3008	CA3094	CA3001	CA3026	CA3036	CA3096
CA107	CA258	CA3010	Micropower	CA3004	CA3035	CA3045	CA3097
CA201	CA358	CA3015	CA3060	CA3005	CA3048	CA3046	CA3118
CA207	CA747	CA3016	CA3078	CA3006	CA3049	CA3050	CA3127
CA301	CA1458	CA3029	CA3080	CA3007	CA3052	CA3051	CA3138
CA307	CA1558	CA3030	CA6078•	CA3026	CA3054	CA3081	CA3146
CA741	CA2904	CA3037		CA3028	CA3060	CA3082	CA3183
CA748	Quad Unit	CA3038		CA3049	CA3102	CA3083	CA3600▲
CA6741•	CA124	CA3100*		CA3050	Diode	CA3084	CA3724
	CA224	CA3130*		CA3051	CA3019	CA3086	CA3725
	CA324	CA3140*		CA3053	CA3039	CA3093	
	CA3401	CA3160*		CA3054	CA3141		
		Dual Unit		CA3102			
		CA3240*					

VOLTAGE REGULATORS	ZERO-VOLTAGE SWITCHES	VOLTAGE COMPARATORS	SPECIAL-FUNCTION CIRCUITS	MOS/FET's	
CA723	CA3058	Single Unit	A/D Converter	Single Gate	Dual Gate
CA3085	CA3059	CA111	CA3162	3N128	3N140
	CA3079	CA211	BCD-to-7-Segment Decoder/Driver	3N138	3N141
		CA311	CA3161	3N139	3N159
		CA3098^{+}	Memory Sense Amplifier	3N142	Dual Gate Protected
		CA3099^{+}	CA1541	3N143	
		Dual Unit	Four-Quadrant Multiplier	3N152	3N187
		CA3290*	CA3091	3N153	3N200
		Quad Unit	Timer	3N154	40819
		CA139	CA555		
		CA239	Programmable Schmitt Trigger		
		CA339	CA3098		

Consumer Circuits

BROADBAND (VIDEO) AMPLIFIERS	AM/FM COMMUNICATIONS CIRCUITS	AUDIO CIRCUITS	FM IF CIRCUITS	TV RECEIVER CIRCUITS		MOS/FET's	
CA3002	CA2111A	Preamplifiers	Subsystems	Tuning	Chroma Systems	Single Gate	Dual Gate Protected
CA1352	CA3011	CA3036	CA2111A	CA3163	CA1398	40467A	
CA3020	CA3012	CA3052	CA3013	CA3166	CA3066	40468A	3N204
CA3021	CA3013	Drivers	CA3014	CA3168	CA3067	40559A	3N205
CA3022	CA3014	CA3094	CA3043	AFT	CA3070	Dual Gate	3N206
CA3023	CA3043	Power Amplifiers	CA3075	CA3044	CA3071	40600	3N211
CA3040	CA3075	CA810	CA3089	CA3064	CA3072	40601	3N212
	CA3076	CA2002	CA3189	CA3139	CA3121	40602	3N213
MULTIPLEX DECODERS	CA3088	CA2004	Gain Blocks	Sound IF	CA3125	40603	40673
	CA3089	CA3131	CA3011	CA1190	CA3126	40604	40820
CA758	CA3123	CA3132	CA3012	CA2111A	CA3128		40821
C1310	CA3163		CA3076	CA3041	CA3151		40822
CA3090A	CA3189			CA3042	CA3170		40823
				CA3065	Luminance Processors		40841
				CA3134			
				PIX IF	CA3135		
				CA270	CA3143		
				CA1352	CA3144		
				CA3068	Horizontal Systems		
				CA3136			
				Remote Control	CA1391		
				CA3035	CA1394		
				"Jungle" Circuits	CA920A		
				CA3120	CA3159		
				CA3142	CA3172		

• Low-noise versions of CA741 and CA3078   * BiMOS types   ▲CMOS type   + Programmable

Operating and Handling Considerations

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of linear integrated circuits and MOS field-effect transistors.

The ratings included in RCA data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by integrated circuits and MOS/FET's makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of these devices provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

MOUNTING

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

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* MIL-38510A, paragraph 3.5.6.1(a), lead material.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

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*Trade Mark: Emerson and Cumming, Inc.

Terms and Symbols

A	closed-loop voltage gain
A_{AF}	audio amplifier gain
A_{DIFF}	differential voltage gain
ACC	automatic chroma control
AFC	automatic frequency control
AFT	automatic fine tuning
AGC	automatic gain control
AMR	am rejection
A_{OL}	open-loop voltage gain
A_{V}	amplifier voltage gain
b_{fs}	small-signal, common-source, forward transfer susceptance (imaginary part of corresponding admittance; see y_{fs})
b_{is}	small-signal, common-source, input susceptance (imaginary part of corresponding admittance; see y_{is})
b_{os}	small-signal, common-source, output susceptance (imaginary part of corresponding admittance, see y_{os})
b_{rs}	small-signal, common-source, reverse transfer susceptance (imaginary part of corresponding admittance, see y_{rs})
BW	bandwidth (unity gain)
BW_{OL}	open-loop bandwidth
C_{BI}	base-to-substrate capacitance
C_{CB}	collector-to-base capacitance
C_{EB}	emitter-to-base capacitance
C_{EXT}	external capacitance
C_{FB}	feedback capacitance
C_{I}	input capacitance
C_{ios}	small-signal output capacitance
C_{is}	small-signal input capacitance
C_{iss}	small-signal, common-source short-circuit input capacitance
$C_{I\text{-}O}$	input-to-output capacitance; data in/out capacitance
CMMR	common-mode rejection ratio
C_{O}	output capacitance
C_{os}	feedthrough capacitance
C_{oss}	small-signal, common-source short-circuit output capacitance
C_{QP}	charge-pump capacitance
C_{rss}	small-signal, common-source short-circuit, reverse transfer capacitance
e_{i}	input sensitivity
E_{N}	I/F noise voltage
e_{N}	low-frequency noise voltage; equivalent short-circuit input noise voltage (μV $\sqrt{\text{Hz}}$)
$e_{N(total)}$	wideband noise voltage referenced to input
e_{O1}/e_{O2}	channel separation
E_{ON}	broadband output noise voltage
f_{CL}	clock input frequency
f_{max}	maximum operating frequency
f_{p}	charge-pump input-pulse frequency
f_{t}	unity-gain crossover frequency; gain-bandwidth product
f_{ϕ}	input-pulse frequency
G_{p}	power gain
G_{m}	forward transconductance (large-signal)
h_{FE}	static forward-current transfer ratio (beta)
h_{fe}	small-signal forward-current transfer ratio
I^{+}	dc supply current
I^{-}	dc supply current
I_{A}	amplifier supply current
I_{ABC}	amplifier bias current
I_{AGC}	AGC source current
I_{B}	base current
I_{C}	collector current
I_{CBO}	collector cutoff current
I_{CEO}	collector cutoff current
$I_{CE(OFF)}$	output leakage current
I_{D}	drain current
$I_{D(ON)}$	dc on-state drain current
I_{DARK}	dark current
I_{DF}	diode forward current
I_{DDO}	supply current for drain supply voltage (V_{DD})
I_{DS}	zero-gate (bias) drain current (dual-gate types)
I_{DSS}	zero-gate (bias) drain current (single-gate types)
I_{F}	forward current
I_{G}	channel (input) gate lead current
I_{GR}	channel (input) gate reverse current
I_{GS}	gate terminal current (single-gate types)
I_{G1S}	gate-No.1 terminal current dual-gate types
I_{G2S}	gate-No. 2 terminal current dual-gate types
I_{GSSF}	gate-to-source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{G1SSF}	gate-No.1 source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{G2SSF}	gate-No. 2-to-source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{GSSR}	gate-to-source reverse leakage current, all other terminals shorted to source (single-gate types).
I_{G1SSR}	gate-No. 1-to-source reverse leakage current, all other terminals shorted to source (dual-gate types).
I_{G2SSR}	gate-No.2-to-source reverse leakage current, all other terminals shorted to source (dual-gate types).
I_{GT}	gate trigger current; gate terminal current
I_{I}	input current
I_{IB}	input bias current
I_{IBC}	internal bias current
I_{IO}	input offset current
αI_{IO}	average temperature coefficient of input offset current
$\Delta I_{IO}/\Delta T$	temperature coefficient of input offset current (drift)
I_{LIM}	short-circuit limiting current
I_{MTR}	current-mirror transfer ratio
I_{N}	I/F noise current
i_{N}	equivalent open-circuit noise current (pA/ $\sqrt{\text{Hz}}$)
I_{O}	output current
$I_{O(DIFF)}$	differential output current (sink)
I_{OO}	output offset current
	output leakage current, low
I_{OM}	peak output current
$\lvert I_{OM} \rvert$	magnitude of peak output current
I_{OM}^{+}	maximum output current (source)
I_{OM}^{-}	maximum output current (sink)
I_{p}	photo current
$I_{p\text{-}p}$	peak-to-peak output current
I_{Q}	total quiescent current
I_{QPL}	charge-pump input current
I_{R}	dc reverse (leakage) current
I_{REFO}	supply current for reference supply voltage
I_{SSO}	strobe load current voltage (V_{SS})
I_{SXO}	supply current for supply voltage
I_{TH}	threshold current
I_{TOTAL}	total supply current
k_{N}	normalized factor ($k_N = k/k_r$)
MAG	maximum available power gain
MUG	maximum useable power gain (unneutralized)
NF	noise factor
P_{O}	power output
P_{D}	device dissipation
P_{SRR}	power supply rejection ratio
$r_{ds(off)}$	small-signal drain-to-source off-state resistance
$r_{ds(on)}$	static drain-to-source on-state resistance
R_{GS}	gate leakage-current resistance
R_{O}	output resistance
R_{o}	low-frequency output resistance
r_{o}	small-signal output resistance
r_{oss}	small-signal, short-circuit, common-source output resistance
R_{I}	differential input resistance
r_{i}	small-signal input resistance
r_{iss}	small-signal, short-circuit, common-source input resistance
R_{i}	low-frequency input resistance
R_{ON}	ON resistance; the ON-state resistance of an analog switch at specified input and load conditions.
ΔR_{ON}	ΔON resistance; the difference in ON-state resistance between any 2 analog switches at specified input and load conditions.
S/N	signal-to-noise ratio
SR	slew rate
T_{A}	ambient temperature
t_{d}	delay time
t_{DR}	differential recovery time
t_{f}	fall time
$t_{f\phi}$	input-pulse rise time
THD	total harmonic distortion
t_{off}	turn-off time
t_{on}	turn-on time
t_{r}	rise time
$t_{R\phi}$	input-pulse rise time
t_{rr}	reverse recovery time
t_{S}	setup time
t_{STG}	storage time
t_{W}	pulse width
V^{+}	DC positive supply voltage
V^{-}	DC negative supply voltage
V_{ABC}	amplifier bias voltage
V_{BB}	substrate voltage
V_{BE}	base-to-emitter voltage

Terms and Symbols

$V_{BE(sat)}$	base-to-emitter saturation voltage
$V_{(BR)CBO}$	collector-to-base breakdown voltage
$V_{(BR)CES}$	collector-to-emitter breakdown voltage
$V_{(BR)DI}$	dc breakdown voltage between diode and substrate
$V_{(BR)R}$	dc reverse breakdown voltage
$V_{(BR)EBO}$	emitter-to-base breakdown voltage
$V_{(BR)GSSF}$	dc gate-to-source forward breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G1SSF}$	dc gate-No.1-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)G2SSF}$	dc gate No.2-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)GSSR}$	dc gate-to-source reverse breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G2SSR}$	dc gate-No.2-to-source reverse breakdown voltage, all other terminals shorted to source (dual-gate types)
V_{CBO}	collector-to-base voltage
V_{CC}	drain supply voltage used as a second positive supply voltage. It is $\leqslant V_{DD}$ and referenced to V_{SS}
VCO	voltage controlled oscillator
V_{CEO}	collector-to-emitter voltage
$V_{CEO(sus)}$	collector-to-emitter sustaining voltage
V_{CIO}	collector-to-substrate voltage
V_{CP}	charge pump voltage
V_{DD}	drain supply voltage (the most positive supply voltage; always referenced to ground)
V_{DG}	drain-to-gate voltage (single-gate types)
V_{DG1}	drain-to-gate-No.1 voltage (dual-gate types)
V_{DG2}	drain-to-gate-No.2 voltage (single-gate types)
V_{DIO}	diode-to-substrate voltage
V_{DR}	diode reverse voltage
V_{DS}	drain-to-source voltage
V_{EE}	source voltage (the most negative supply voltage in a 3-supply voltage system)
V_F	dc forward voltage
$\Delta V_F/\Delta T$	temperature coefficient of forward voltage drop
V_{GH}	channel gate input voltage, high level
V_{GL}	channel gate input voltage, low level
V_{GS}	gate-to-source voltage
$V_{GS}(TH)$	gate-to-source threshold voltage
$V_{GS}(Off)$	gate-to-source cutoff voltage (single-gate types)
V_{G1S}	gate-No.1-to-source voltage (dual-gate type)
$V_{G1S}(Off)$	gate-No.1-to-source cutoff voltage (dual-gate types)
V_{G2S}	gate-No.2-to-source voltage (dual-gate types)
$V_{G2S}(off)$	gate-No.2-to-source cutoff voltage (dual-gate types)
V_I	input voltage
$V_{I(Lim)}$	input limiting voltage
V_{ICR}	common-mode input voltage range
V_{IL}	input-voltage, low level
V_{IH}	input-voltage, high level
V_{IO}	input offset voltage
$\lvert V_{IO}\rvert$	magnitude of input offset voltage
$\Delta V_{IO}/\Delta T$	temperature coefficient of magnitude of input offset voltage
$\Delta V_{IO}/\Delta T$	temperature coefficient of input offset voltage drift
$\Delta V_{IO}/\Delta V^+$	positive input-offset-voltage sensitivity
$\Delta V_{IO}/\Delta V^-$	negative input-offset-voltage sensitivity
αV_{IO}	average temperature coefficient of input-offset voltage
$V_{i(Lim)}$	input limiting voltage (knee)
V_{knee}	protective diode knee voltage (protected gate types)
V_N	output noise voltage
V_O	output voltage
$\Delta V_O/\Delta V^-$	dc supply voltage sensitivity
$\Delta V_O/\Delta V^+$	dc supply voltage sensitivity
$V_{O(rms)}$	open-loop output voltage swing
ΔV_O	output voltage temperature coefficient
$V_{Op\text{-}p}$	output voltage swing
$V_{O(af)}$	recovered af voltage
V_{OL}	output voltage, low level; the voltage level at an output when the input logic conditions have been set to establish logic LOW output.
V_{OO}	output offset voltage
V_{OH}	output voltage, high level; the voltage level at an output when the input logic conditions have been set to establish a logic HIGH output.
$V_{OM}{}^+$	maximum output voltage
$V_{OM}{}^-$	maximum output voltage
V_{QP}	charge pump voltage
V_{QPL}	charge pump input voltage, low level
V_{QPH}	charge-pump input voltage, high level
V_{REF}	reference voltage
V_{REG}	regulated supply voltage
V_{RR}	supply voltage rejection ratio
V_{TH}	input threshold voltage
V_Z	zener voltage
Y_{fs}	magnitude of small-signal, common-source, short-circuit forward transfer admittance (transadmittance)
Y_{is}	small-signal, common-source, short-circuit, input-admittance (conductance, real part of admittance; susceptance, imaginary part of admittance)
Y_{os}	small-signal, common-source, short-circuit, output admittance
$\lvert Y_{rs}\rvert$	magnitude of small-signal, common-source, short-circuit, reverse transadmittance
$\angle Y_{rs}$	phase angle of small-signal, common-source, short-circuit, reverse transadmittance
$(-)_{rs}$	angle of reverse transadmittance, common-source circuit
Z_1	input impedance
Z_O	output impedance
Z_Z	zener impedance
ϕ	phase angle
ϕ	phase margin
η	efficiency
$\phi \cdot L$	open-loop phase lag

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
AD101AH	CA101AT
AD101AN	CA101AG,CA101AE
AD201AH	CA201AT
AD201AN	CA201AG,CA201AE
AD301AH	CA301AT
AD301AN	CA301AG,CA301AE
AD741H	CA741T
AD741N	CA741G,CA741E
AD741CH	CA741CT
AD741CN	CA741CG,CA741CE
AD2020	CA3162E
AMLM101AD	CA101AG
AMLM101AH	CA101AT
AMLM101H	CA101T
AMLM107D	CA107G
AMLM107H	CA107T
AMLM111D	CA111G
AMLM111H	CA111T
AMLM201AD	CA201AG
AMLM201AH	CA201AT
AMLM201D	CA201G
AMLM201H	CA201T
AMLM207D	CA207G
AMLM207H	CA207T
AMLM211D	CA2111G
AMLM211H	CA2111T
AMLM301AD	CA301AG
AMLM301AH	CA301AT
AMLM301H	CA301T
AMLM307D	CA307G
AMLM307H	CA307T
AMLM311D	CA311G
AMLM311H	CA311T
AM723HC	CA723CT
AM723HM	CA723T
AM741DC	CA741CG
AM741DM	CA741G
AM741HC	CA741CT
AM741HM	CA741T
AM747DC	CA747CG
AM747DM	CA747G
AM747HC	CA747CT
AM747HM	CA747T
AM748DC	CA748CG
AM748HC	CA748CT
AM748DM	CA748G
AM1458H	CA1458T
AM1558H	CA1558T
DH3724CN	CA3724G
DH3725CN	CA3725F
FPQ3724	CA3724G
FPQ3725	CA3725G
HA1-2111-2	CA111G
HA1-2211-4	CA211G
HA1-2311-5	CA311G
HA1-2630	CA3020
HA1-2650	CA1558G, CA1558E
HA1-2655	CA1458G, CA1458E
HA1-2720	CA6078
HA2-2111-2	CA111T
HA2-2111-4	CA211T
HA2-2311-5	CA311T
HA2-2520	CA3100T
HA2-2650	CA1558T
HA2-2655	CA1458T
HA2-2720	CA3078E
ITT1352N	CA1352E
ITT3064C	CA3064T
ITT3064N	CA3064E
ITT3065N	CA3065E
L4001M9	2N5756
LM100	CA3085E
LM101AD	CA101AG
LM101ADE	CA101AG
LM101AF	CA101AG
LM101AH	CA101AT
LM101AJ	CA101AG
LM101AJG	CA101AG
LM101AL	CA101AT
LM101AN	CA101AG,CA101AE
LM101AP	CA101AG, CA101AE
LM101AT	CA101AT
LM101D	CA101G
LM101F	CA101G
LM101H	CA101T
LM101J	CA101G
LM101N	CA101G, CA101E
LM101T	CA101T
LM107D	CA107G
LM107DE	CA107G
LM107F	CA107G
LM107H	CA107T
LM111JG	CA111G
LM107N	CA107G, CA107E
LM111P	CA111G, CA111E
LM107T	CA107T
LM111D	CA111G
LM111H	CA111T
LM111L	CA111T
LM111N	CA111G, CA111E
LM111T	CA111T
LM111V	CA111G,CA111E
LM124D	CA124G
LM124F	CA124G
LM124J	CA124G
LM124N	CA124G, CA124E
LM139AD	CA139AG
LM139AF	CA139AG
LM139AJ	CA139AG
LM139AN	CA139AG, CA139AE
LM139A	CA139G,CA139E
LM139D	CA139G
LM139F	CA139G
LM139J	CA139G
LM139N	CA139G, CA139E
LM158AH	CA158AT
LM158AN	CA158AG, CA158AE
LM158AT	CA158AT
LM158JG	CA158G
LM158L	CA158T
LM158N	CA158G, CA158E
LM158P	CA158G, CA158E
LM158T	CA158T
LM201AD	CA201AG
LM201AF	CA201G
LM201AH	CA201AT
LM201AJ	CA201AG
LM201AJG	CA201AG
LM201AL	CA201AT
LM201AN	CA201AG, CA201AE
LM201AP	CA201AG,CA201AE
LM201AT	CA201AT
LM201AV	CA201AG, CA201AE
LM201D	CA201G
LM201F	CA201G
LM201H	CA201T
LM201J	CA201G
LM201N	CA201G, CA201E
LM201N-14	CA201G,CA201E
LM201T	CA201T
LM207D	CA207G
LM207F	CA207G
LM207H	CA207T
LM207J	CA207G
LM207N	CA207G, CA207E
LM207T	CA207T
LM211D	CA211G
LM211H	CA211T
LM211N	CA211G, CA211E
LM211T	CA211T
LM224A	CA224G,CA224E
LM224D	CA224G
LM224F	CA224G
LM224N	CA224G,CA224E
LM224T	CA224G
LM239AD	CA239AG
LM239AF	CA239AG
LM239AJ	CA239AG
LM239AN	CA239AG, CA239AE
LM239A	CA239G, CA239E
LM239D	CA239G
LM239F	CA239G
LM239J	CA239G
LM239N	LM239G, CA239E
LM258AH	CA258AT
LM258AN	CA258AG, CA258AE
LM258AT	CA258AT
LM258AJ	CA258AG
LM258JG	CA258G
LM258H	CA258T
LM258L	CA258T
LM258N	CA258G, CA258E
LM258P	CA258G, CA258E
LM258T	CA258T
LM301AD	CA301AG
LM301AH	CA301AT
LM301AF	CA301AG
LM301AJ	CA301AG
LM301AJG	CA301AG
LM301AL	CA301AT
LM301AN	CA301AG, CA301AE
LM301AP	CA301AG, CA301AE
LM301AT	CA301AT
LM301AV	CA301AG, CA301AE
LM301T	CA301T
LM307DE	CA307G
LM307D	CA307G
LM307F	CA307G
LM307H	CA307T
LM307N	CA307G, CA307E
LM307T	CA307T
LM311D	CA311G
LM311F	CA311G
LM311H	CA311T
LM311JG	CA311G

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
LM311L	CA311T
LM311N	CA311G, CA311E
LM311N-14	CA311G,CA311E
LM311P	CA311G, CA311E
LM311T	CA311T
LM318H	CA3130T
LM324AD	CA324AG
LM324AN	CA324AG, CA324AF
LM324D	CA324G
LM324F	CA324G
LM324J	CA324G
LM324N	CA324G, CA324E
LM339AD	CA339AG
LM339AF	CA339AG
LM339AJ	CA339AG
LM339AN	CA339AG, CA339AE
LM339A	CA339G, CA339E
LM339D	CA339G
LM339F	CA339G
LM339J	CA339G
LM339N	CA339G, CA339E
LM358AH	CA358AT
LM358AN	CA358AG, CA358AE
LM358AT	CA358AT
LM358JG	CA358G
LM358H	CA358
LM358L	CA358T
LM358N	CA358G, CA358E
LM358P	CA358G, CA358E
LM358T	CA358T
LM393N	CA3290E
LM555CH	CA555CT
LM555CN	CA555CG, CA555CE
LM555H	CA555T
LM555N	CA555G, CA555E
LM723CD	CA723CE
LM723CH	CA723CT
LM723CN	CA723CE
LM723D	CA723E
LM723H	CA723T
LM723N	CA723E
LM741CH	CA741CT
LM741CJ	CA741CG
LM741CN	CA741CG, CA741CE
LM741H	CA741T
LM741N	CA741G, CA741E
LM746N	CA3072
LM747CD	CA747CG
LM747CH	CA747CT
LM747CJ	CA747CG
LM747CN	CA747CG, CA747CE
LM747D	CA747G
LM747H	CA747T
LM747J	CA747G
LM748CH	CA748CT
LM748CJ	CA748CG
LM748CN	CA748CG, CA748CE
LM748H	CA748T
LM748J	CA748G
LM1310N	CA1310E
LM1391N	CA1391E
LM1394N	CA1394E
LM1458H	CA1458T
LM1458J	CA1458G
LM1458N	CA1458G, CA1458E
LM1558H	CA1558T
LM1558J	CA1558G
LM1558N	CA1558G, CA1558E
LM1800N	CA758E
LM1820N	CA3123E
LM1845N	CA3120E
LM2111N	CA2111AE
LM2901N	CA339G
LM2904N	CA2904G
LM2904P	CA2904G
LM3011H	CA3011
LM3018H	CA3018
LM3018AH	CA3018A
LM3019H	CA3019
LM3026H	CA3026
LM3028AH	CA3028A
LM3028B	CA3028B
LM3039H	CA3039
LM3045D	CA3045
LM3046N	CA3046
LM3053H	CA3053
LM3054N	CA3054
LM3064H	CA3064T
LM3064N	CA3064E
LM3065N	CA3065
LM3066N	CA3066
LM3067N	CA3067
LM3070N	CA3070
LM3071N	CA3071
LM3075N	CA3075
LM3086N	CA3086
LM3089N	CA3089E, CA3189E
LM3126N	CA3126E
LM3146AN	CA3146AE
LM3401N	CA3401G, CA3401E
MC1310P	CA1310E
MC1352P	CA1352E
MC1357P	CA2111AE
MC1357PQ	CA2111AQ
MC1358P	CA3065
MC1364G	CA3064T
MC1364P	CA3064E
MC1370P	CA3070
MC1371P	CA3071
MC1375P	CA3075
MC1389P	CA3089E, CA3189E
MC1391P	CA1391E
MC1394P	CA1394E
MC1398P	CA1398E
MC1455G	CA555CT
MC1455P1	CA555CG, CA555CE
MC1455U	CA555CG
MC1458JG	CA1458G
MC1458G	CA1458T
MC1458L	CA1458T
MC1458P	CA1458G, CA1458E
MC1458P1	CA1458G, CA1458E
MC1458T	CA1458T
MC1541L	CA1541D
MC1555G	CA555T
MC1555P1	CA555CG, CA555CE
MC1555U	CA555G
MC1558JG	CA1558T
MC1558G	CA1558T
MC1558L	CA1558T
MC1558P	CA1558G, CA1558E
MC1558P1	CA1558G, CA1558E
MC1558T	CA1558T
MC1558U	CA1558G
MC1723CG	CA723CT
MC1723CP	CA723CE
MC1723G	CA723T
MC1741CG	CA741CT
MC1741CL	CA741CG
MC1741CP1	CA741CG, CA741CE
MC1741CP2	CA741CG,CA741CE
MC1741G	CA741T
MC1741L	CA741G
MC1741U	CA741G
MC1747CG	CA747CT
MC1747CL	CA747CG
MC1747G	CA747T
MC1747L	CA747G
MC1748CG	CA748CT
MC1748CP1	CA748CG, CA748CE
MC1748CU	CA748CG
MC1748G	CA748T
MC1748U	CA748G
MC3346P	CA3046
MC3386P	CA3086
MC3401L	CA3401G
MC3401P	CA3401E
MLM101AG	CA101AT
MLM101AU	CA101AG
MLM107G	CA101T
MLM107U	CA101G
MLM111G	CA111T
MLM111U	CA111G
MLM124L	CA124G
MLM139AL	CA139AG
MLM139L	CA139G
MLM158G	CA158T
MLM158P1	CA158G, CA158E
MLM158U	CA158G
MLM201AG	CA201AT
MLM201AP1	CA201AG, CA201AE
MLM201AU	CA201AG
MLM207G	CA207T
MLM207U	CA207G
MLM211G	CA211T
MLM211U	CA211G
MLM224L	CA224G
MLM224P	CA224G, CA224E
MLM239AL	CA239AG
MLM239AP	CA239AG, CA239AE
MLM239L	CA239G
MLM239P	CA239G, CA239E
MLM258G	CA258T
MLM258U	CA258G
MLM301AD	CA301AG
MLM301AG	CA301AT
MLM301AP1	CA301AG, CA301AE
MLM301AU	CA301AG
MLM307G	CA307T
MLM307P1	CA307G, CA307E
MLM307U	CA307G
MLM311G	CA311T
MLM311P1	CA311G, CA311E
MLM311U	CA311G
MLM324L	CA324G, CA324E

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
MLM324P1	CA324G
MLM339AL	CA339AG
MLM339AP	CA339AG, CA339AE
MLM339L	CA339G
MLM339P	CA339G, CA339E
MLM358G	CA358T
MLM358P1	CA358G, CA358E
MLM358U	CA358G
MPQ3724	CA3724G
MPQ3725	CA3725G
NE555JG	CA555CG
NE555P	CA555CG,CA555CE
NE555L	CA555T
NE555T	CA555CT
NE555V	CA555CG, CA555CE
PM741J	CA741T
PM741CJ	CA741CT
PM741Y	CA741G
PM741CY	CA741CG
PM747K	CA747T
PM747CK	CA747CT
PM747Y	CA747G
PM747CY	CA747CG
Q2T3725	CA3725G
RC555DE	CA555CG
RC555NB	CA555CG, CA555CE
RC555T	CA555CT
RC723DB	CA723CE
RC723T	CA723CT
RC1458DE	CA1458G
RC1458NB	CA1458G, CA1458E
RC1458T	CA1458T
RC3401DB	CA3401G, CA3401E
RC741DB	CA741CG,CA741CE
RC741DC	CA741CG
RC741DE	CA741CG
RC741NB	CA741CG, CA741CE
RC741T	CA741T
RC747DC	CA747CG
RC747DB	CA747CG, CA747CE
RC747T	CA747T
RM555DE	CA555G
RM555T	CA555T
RM723T	CA723T
RM741DC	CA741G
RM741DE	CA741G
RM741T	CA741T
RM747DC	CA747G
RM747T	CA747T
RM1558DE	CA1558G
RM1558T	CA1558T
SE555JG	CA555G
SE555L	CA555T
SE555N	CA555G, CA555E
SE555P	CA555G, CA555E
SE555T	CA555T
SE9300	RCA120
SE9301	RCA121
SE9302	RCA122
SE9303	2N6384
SE9304	2N6385
SFC2101A	CA101AT
SFC2107M	CA107T
SFC211M	CA111T
SFC2201A	CA201AT
SFC2207	CA207T
SFC2211	CA211T
SFC2301A	CA301AT
SFC2301ADC	CA301AE
SFC2307	CA307T
SFC2311	CA311T
SFC2741C	CA741CT
SFC2741M	CA741T
SFC2748DC	CA748CE
SFC2748C	CA748CT
SG101AD	CA101AG
SG101D	CA101G
SG107D	CA107G
SG111D	CA111G
SG111M	CA111G, CA111E
SG111T	CA111T
SG201AD	CA201AG
SG201AM	CA201AG
SG201N	CA201G, CA201E
SG201M	CA201G, CA201E
SG207D	CA207G
SG207N	CA207G, CA207E
SG207T	CA207T
SG211D	CA211G
SG211M	CA211G, CA211E
SG211T	CA211T
SG301AM	CA301AG, CA301AE
SG301AT	CA301AT
SG301N	CA301G, CA301E
SG301T	CA301T
SG307D	CA307G
SG307N	CA307G, CA307E
SG307T	CA307T
SG311D	CA311G
SG311M	CA311G, CA311E
SG311T	CA311T
SG723CN	CA723CE
SG723CT	CA723CT
SG723T	CA723T
SG741CD	CA741CG
SG741CM	CA741CG
SG741CN	CA741CG,CA741CE
SG741CT	CA741CT
SG741D	CA741G
SG741T	CA741T
SG747CD	CA747CG
SG747CN	CA747CG, CA747CE
SG747CT	CA747CT
SG747D	CA747G
SG747T	CA747T
SG748CM	CA748CG
SG748CN	CA748CG, CA748CE
SG748CT	CA748CT
SG748T	CA748T
SG1458M	CA1458G, CA1458E
SG1458T	CA1458T
SG1558T	CA1558T
SG3018T	CA3018
SG3018AT	CA3018A
SG3058J	CA3058D
SG3059J	CA3059D
SG3079J	CA3079D
SG3081N	CA3081E
SG3081J	CA3081F
SG3082N	CA3082E
SG3082J	CA3082F
SG3083J	CA3083F
SG3401N	CA3401G, CA3401E
SN52101AJ	CA101AG
SN52101AL	CA101AT
SN52101AN	CA101AG
SN52101AP	CA101AG, CA101AE
SN52107L	CA107T
SN52107P	CA107G, CA107E
SN52111L	CA111T
SN5211P	CA111G, CA111E
SN52555L	CA555T
SN52555P	CA555G, CA555E
SN52558L	CA1558T
SN52558P	CA1558G, CA1558E
SN52723N	CA723E
SN52723L	CA723T
SN52741J	CA741CG
SN52741L	CA741CT
SN52741N	CA741CG,CA741CE
SN52741P	CA741CG, CA741CE
SN52747L	CA747T
SN52747N	CA747G, CA747E
SN52748J	CA748G
SN52748L	CA748T
SN52748N	CA748G,CA748E
SN52748P	CA748G, CA748E
SN72301AJ	CA301AG
SN72301AL	CA301AT
SN72301AN	CA301AG,CA301AE
SN72301AP	CA301AG
SN72307L	CA307T
SN72307N	CA307G,CA307E
SN72307P	CA307G, CA307E
SN72311L	CA311T
SN72311P	CA311G, CA311E
SN72555L	CA555CT
SN72555P	CA555CG, CA555CE
SN72558L	CA1458T
SN72558P	CA1458G, CA1458E
SN72723N	CA723CE
SN72723L	CA723CT
SN72741J	CA741CG
SN72741L	CA741CT
SN72741N	CA741CG,CA741CE
SN72741P	CA741CG, CA741CE
SN72747J	CA747CG
SN72747L	CA747CT
SN72747N	CA747CG, CA747CE
SN72748J	CA748CG
SN72748L	CA748CT
SN72748N	CA748CG,CA748CE
SN72748P	CA748CG, CA748CE
SN76115N	CA1310E
SN76116N	CA758E
SN76242N	CA3070
SN76243AN	CA3071
SN76264N	CA3072
SN76266N	CA3066
SN76267N	CA3067
SN76298N	CA1398E
SN76564N	CA3064
SN76565N	CA3064E
SN76635N	CA3123E
SN76650N	CA1352E

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
SN76666N	CA3065
SN76675N	CA3075
SN76676P	CA3076
SN76689N	CA3089E, CA3189E
SP3724	CA3724G
SP3725	CA3725G
SSS101AJ	CA101AT
SSS101AP	CA101AG, CA101AE
SSS107J	CA107T
SSS107P	CA107G, CA107E
SSS201AJ	CA201AT
SSS201AP	CA201AG, CA201AE
SSS207J	CA207T
SSS301AJ	CA301AT
SSS301AP	CA301AG, CA301AE
SSS741CJ	CA741CT
SSS1458J	CA1458T
SSS1558J	CA1558T
TBA810S	CA810Q
TBA810AS	CA810QM
TDA2002V	CA2002
TDA2002H	CA2002M
TBB0747	CA747CT
TBB0748	CA748CT
TBB0748B	CA748CE
TBB1458B	CA1458E
TBC0747	CA747T
TCA270	CA270
TDA3081N	CA3081
TDA3082N	CA3082
TDA3083N	CA3083
TDB0723	CA723CT
TDB0723A	CA723CE
TDC0723	CA723T
U5B7741312	CA741T
U5B7741393	CA741CT
U5B7748312	CA748T
U5B7748393	CA748CT
U5R7723312	CA723T
U5R7723393	CA723CT
U6A7723393	CA723CG, CA723CE
U9T7758393	CA1458G
U9T7741393	CA741CG, CA741CE
ULN2111A	CA2111AE
ULN2111N	CA2111AQ
ULN2114A	CA3072
ULN2124A	CA3070
ULN2125A	CA3120E
ULN2127A	CA3071
ULN2129A	CA3075
ULN2137A	CA3123E
ULN2165A	CA3065
ULN2210A	CA1310E
ULN2212B	CA3012
ULN2262A	CA3126Q
ULN2264A	CA3064
ULN2266A	CA3066
ULN2267A	CA3067
ULN2269A	CA3121E
ULN2289A	CA3089E, CA3189E
ULN2298A	CA1398E
ULX2244A	CA758E
µA101AH	CA101AT
µA101AD	CA101AG
µA101D	CA101G
µA101H	CA101T
µA107H	CA107T
µA111H	CA111T
µA111R	CA111G
µA201AD	CA201AG
µA201AH	CA201AT
µA201D	CA201G
µA201H	CA201AT
µA207H	CA207T
µA301AD	CA301AG
µA301AH	CA301AT
µA307H	CA307T
µA307T	CA307G, CA307E
µA301AT	CA301AG, CA301AE
µA311H	CA311T
µA311R	CA311G
µA311T	CA311G, CA311E
µA555HC	CA555CT
µA555HM	CA555T
µA555TC	CA555CG, CA555CE
µA720PC	CA3123E
µA723CA	CA723CE
µA723CK	CA723CT
µA723CL	CA723CT
µA723CN	CA723CE
µA723DM	CA723E
µA723HC	CA723CT
µA723HM	CA723T
µA723K	CA723T
µA723MN	CA723E
µA723ML	CA723T
µA723PC	CA723CE
µA741CJG	CA741CG
µA741CJ	CA741CG
µA741CN	CA741CG,CA741CE
µA741CL	CA741T
µA741CP	CA741CG, CA741CE
µA741CT	CA741CT
µA741DC	CA741G
µA741DM	CA741G
µA741HC	CA741CT
µA741HM	CA741T
µA741MJG	CA741G
µA741MJ	CA741G
µA741ML	CA741T
µA741MN	CA741G,CA741E
µA741MP	CA741G, CA741E
µA741PC	CA741G, CA741E
µA746PC	CA3072
µA747CA	CA747CE
µA747CJ	CA747CG
µA747CK	CA747CT
µA747CL	CA747CT
µA747CN	CA747CG, CA747CE
µA747DC	CA747CG
µA747DM	CA747G
µA747HC	CA747CT
µA747HM	CA747T
µA747MJ	CA747G
µA747ML	CA747T
µA747MN	CA747G, CA747E
µA747PC	CA747G, CA747E
µA747A	CA747E
µA747K	CA747T
µA748CJG	CA748G
µA748CJ	CA748CG
µA748CL	CA748T
µA748CN	CA748G,CA748E
µA478CP	CA748G,CA748E
µA748CT	CA748CT
µA748DC	CA748CG
µA748DM	CA748G, CA748E
µA748HC	CA748CT
µA748HM	CA748T
µA748MJG	CA748G
µA748MJ	CA748G
µA748ML	CA748T
µA748MN	CA748G,CA748E
µA748MP	CA748G, CA748E
µA748T	CA748T
µA748TC	CA748CG, CA748CE
µA758PC	CA758E
µA780PC	CA3070
µA781PC	CA3071
µA787PC	CA3126Q
µA1391T	CA1391E
µA1394T	CA1394E
µA1458HC	CA1458T
µA1458R1	CA1458G
µA1458HC	CA1458G, CA1458E
µA1558HM	CA1558T
µA3018HM	CA3018
µA3018AHM	CA3018A
µA3019HM	CA3019
µA3026HM	CA3026
µA3036HM	CA3036
µA3039HM	CA3039
µA3045DM	CA3045
µA3046DC	CA3046
µA3064HC	CA3064T
µA3064PC	CA3064E
µA3065PC	CA3065
µA3066PC	CA3066
µA3075PC	CA3075
µA3086DC	CA3086F
µA3089E	CA3089E, CA3189E
µA3401P	CA3401G, CA3401E
µPC151A	CA741CT
µPC151C	CA741CG, CA741CE
µPC157A	CA301AT
µPC157C	CA301AG, CA301AE
µPC251A	CA747CT
µPC251C	CA1458G, CA1458E
µPC301AC	CA301AG, CA301AE
µPC311C	CA311G, CA311E
µPC324C	CA324G, CA324E
µPC339C	CA339G, CA339E
µPC741C	CA741CG, CA741CE
µPC1458C	CA1458G, CA1458E

Linear Integrated Circuits for Industrial Applications

Technical Data

CA101, CA201, CA301 Types

Operational Amplifiers

For Commercial, Industrial, and Military Applications

RCA-CA101, CA101A, CA201, CA201A, and CA301A are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These types, which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain; unity-gain compensation can be obtained with a single 30-pF capacitor. Types CA101A and CA201A have all the desirable features and characteristics of the CA101 and CA201, respectively, plus superior input-offset characteristics, and improved noise performance.

All types are available in hermetic gold-CHIP dual-in-line plastic packages (G suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA301A is also available in the 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

"G" Suffix Types—Hermetic Gold-CHIP Dual-In-Line Plastic Package
"E" Suffix Types—Standard Dual-In-Line Plastic Package
"T" and "S" Suffix Types—TO-5 Style Package

Features:

- Short-circuit protection and latch-free operation
- Unity-gain phase compensation with a single 30-pF capacitor
- Replacement for industry types 101, 101A, 201, 201A, 301A

Applications:

- Long-interval integrator
- Timers
- Sample and hold circuits
- Summing amplifiers
- Multivibrators
- Comparators
- Instrumentation
- AC/DC converters
- Inverting amplifiers
- Sine- & square-wave generators
- Capacitance multipliers & simulated inductors

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^oC$*

DC SUPPLY VOLTAGE (between V^+ and V^- terminals):		
CA101, CA101A, CA201, CA201A	44	V
CA301A	36	V
DC INPUT VOLTAGE	±15	V
(For supply voltage less than ± 15 V, the Input Voltage rating is equal to the DC Supply Voltage)		
DIFFERENTIAL INPUT VOLTAGE	± 30	V
OUTPUT SHORT-CIRCUIT DURATION	Indefinite*	
DEVICE DISSIPATION:		
Up to $T_A = 75^oC$	500	mW
Above $T_A = 75^oC$	derate linearly at 6.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating –		
CA101, CA101A	–55 to +125	°C
CA201A	–25 to +85	°C
CA201, CA301A	0 to +70	°C
Storage (All types)	–65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

---

* At $T_A \leqslant 70^oC$ and $T_C \leqslant 125^oC$ (CA101);
$T_A \leqslant 75^oC$ and $T_C \leqslant 125^oC$ (CA101A, CA201A);
$T_A \leqslant 55^oC$ and $T_C \leqslant 70^oC$ (CA201, CA301A).

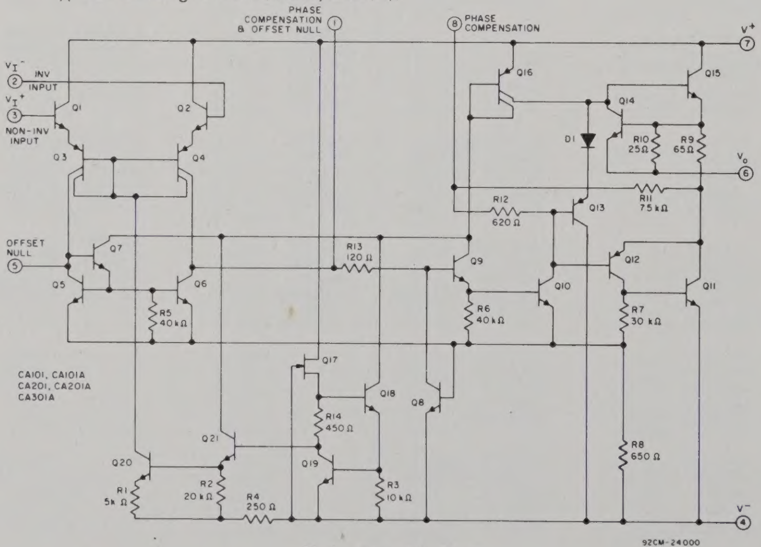
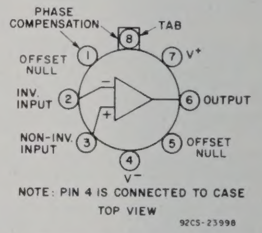
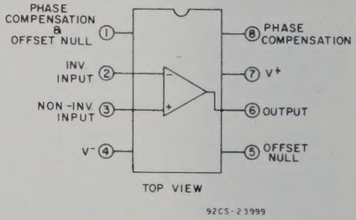


Fig.1 – Schematic diagram.



a – TO-5 style package for all types

T-Suffix
S-Suffix



b – Plastic package for CA301A

G-Suffix
E-Suffix

Fig.2 – Functional diagrams.

CA101, CA201, CA301 Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS▲ Supply Voltage ($V^{\pm}$) = 5 to 15 V		CA101			CA201			UNITS	CA101A CA201A			CA301A			UNITS
			Min.	Typ.	Max.	Min.	Typ.	Max.		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage V_{IO}	T_A=25°C	$R_S \leqslant 10k\Omega$	–	1	5	–	2	7.5	mV	–	–	–	–	–	–	mV
		$R_S \leqslant 50k\Omega$	–	–	–	–	–	–		–	0.7	2	–	2	7.5	
		$R_S \leqslant 10k\Omega$	–	–	6	–	–	10		–	–	–	–	–	–	
		$R_S \leqslant 50k\Omega$	–	–	–	–	–	–		–	–	3	–	–	10	
Average Temperature Coefficient of Input Offset Voltage αV_{IO}		$R_S \leqslant 10k\Omega$	–	6	–	–	10	–	μV/°C	–	–	–	–	–	–	μV/°C
		$R_S \leqslant 50\Omega$	–	3	–	–	6	–		–	–	–	–	–	–	
			–	–	–	–	–	–		–	3	15	–	6	30	
Average Temperature Coefficient of Input Offset Current αI_{IO}	–55°C to +25°C		–	–	–	–	–	–	nA/°C	–	0.02	0.2	–	–	–	nA/°C
	0°C to +25°C		–	–	–	–	–	–		–	–	–	–	0.02	0.6	
	+25°C to +70°C		–	–	–	–	–	–		–	–	–	–	0.01	0.3	
	+25°C to +125°C		–	–	–	–	–	–		–	0.01	0.1	–	–	–	
Input Offset Current I_{IO}	T_A=0°C		–	–	–	–	150	750	nA	–	–	–	–	–	–	nA
	T_A=25°C		–	40	200	–	100	500		–	1.5	10	–	3	50	
	T_A=70°C		–	–	–	–	50	400		–	–	–	–	–	–	
	T_A=125°C		–	10	200	–	–	–		–	–	–	–	–	–	
			–	–	–	–	–	–		–	–	20	–	–	70	
	T_A=–55°C		–	100	500	–	–	–		–	–	–	–	–	–	
Input Bias Current I_{IB}	T_A=–55°C		–	0.28	1.5	–	–	–	μA	–	–	–	–	–	–	μA
	T_A=0°C		–	–	–	–	0.32	2		–	–	–	–	–	–	
	T_A=25°C		–	0.12	0.5	–	0.25	1.5		–	0.03	0.075	–	0.07	0.25	
			–	–	–	–	–	–		–	–	0.1	–	–	0.3	
Supply Current $I^{\pm}$	T_A=25°C	$V^{\pm}$=15V	–	–	–	–	–	–	mA	–	–	–	–	1.8	3	mA
		$V^{\pm}$=20V	–	1.8	3	–	1.8	3		–	1.8	3	–	–	–	
	T_A=125°C	$V^{\pm}$=20V	–	1.2	2.5	–	–	–		–	1.2	2.5	–	–	–	
Open-Loop Differential Voltage Gain A_{OL}	T_A=25°C V_O=±10V	$V^{\pm}$=15V $R_L \geqslant 2k\Omega$	50	160	–	20	150	–	V/mV	50	160	–	25	160	–	V/mV
	V_O=±10V	$V^{\pm}$=15V $R_L \geqslant 2k\Omega$	25	–	–	15	–	–		25	–	–	15	–	–	
Input Resistance R_I	T_A=25°C		0.3	0.8	–	0.1	0.4	–	MΩ	1.5	4	–	0.5	2	–	MΩ
Output Voltage Swing V_{OPP}	$V^{\pm}$=15V	R_L=10kΩ	±12	±14	–	±12	±14	–	V	±12	±14	–	± 12	±14	–	V
	$V^{\pm}$=15V	R_L=2kΩ	±10	±13	–	±10	±13	–		±10	±13	–	±10	±13	–	
Common-Mode Input-Voltage Range V_{ICR}	$V^{\pm}$=15V		±12	–	–	±12	–	–	V	–	–	–	±12	–	–	V
	$V^{\pm}$=20V		–	–	–	–	–	–		±15	–	–	–	–	–	
Common-Mode Rejection Ratio CMRR		$R_S \leqslant 10k\Omega$	70	90	–	65	90	–	dB	–	–	–	–	–	–	dB
		$R_S \leqslant 50k\Omega$	–	–	–	–	–	–		80	96	–	70	90	–	
Supply-Voltage Rejection Ratio PSRR		$R_S \leqslant 10k\Omega$	70	90	–	70	90	–	dB	–	–	–	–	–	–	dB
		$R_S \leqslant 50k\Omega$	–	–	–	–	–	–		80	96	–	70	90	–	

▲ Characteristics applicable over operating temperature range (T_A) as shown below, unless otherwise specified: CA101, CA101A: –55 to +125°C; CA201A: –25 to +85°C; CA201, CA301A: 0 to 70°C

		CA101	CA201	CA101A	CA201A	CA301A	
Max. V_{IO}	T_A = 25°C	5	7.5	2	2	7.5	mV
Max. I_{IO}		200	500	10	10	50	nA
Min. A_{OL}		50	20	50	50	25	V/mV
T_A Range (Operating)		–55 to +125	0 to +70	–55 to +125	–25 to +85	0 to +70	°C
Slew Rate (Summing ampl.)		–	–	10	10	10	V/μs

CA101, CA201, CA301 Types

TYPICAL STATIC CHARACTERISTICS

Type CA101

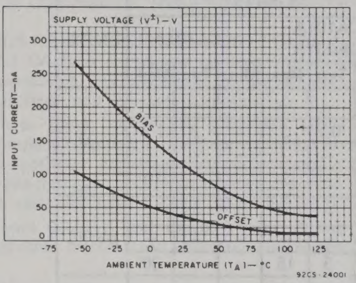


Fig.3 — Input current (I_{IO}, I_{IB}) vs. temperature.

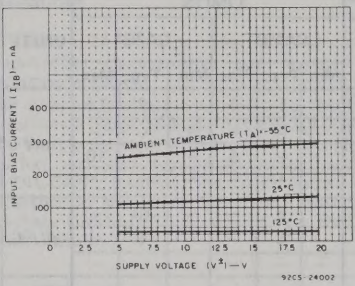


Fig.4 — Input bias current vs. supply voltage.

Types CA101, CA101A, and CA201A

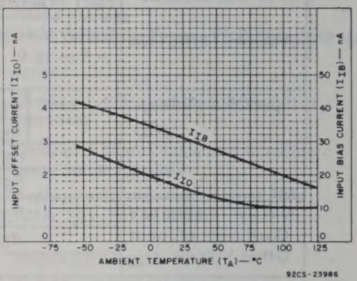


Fig. 5 — Input current (I_{IO}, I_{IB}) vs. temperature (CA101A and CA201A only).

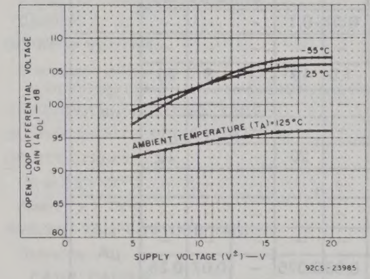


Fig.6 — Voltage gain vs. supply voltage.

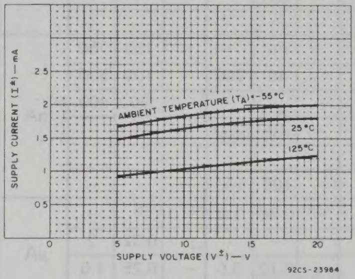


Fig.7 — Supply characteristics.

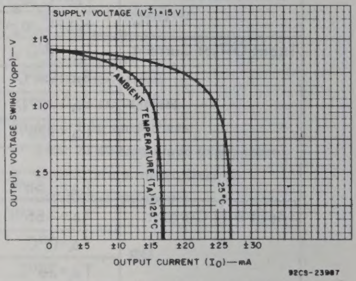


Fig.8 — Output characteristics.

Type CA301A

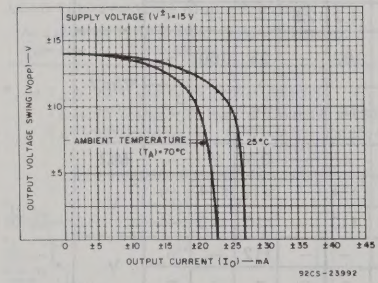


Fig. 9 — Output characteristics.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA101A AND CA201A

Single-Pole Compensation

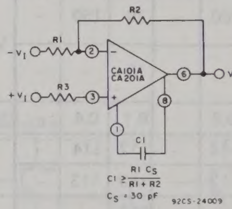


Fig. 10 — Test circuit employing single-pole compensation.

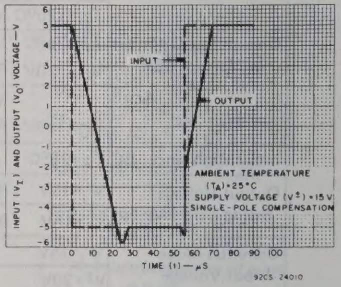


Fig. 11 — Voltage follower (V_I, V_O) pulse response.

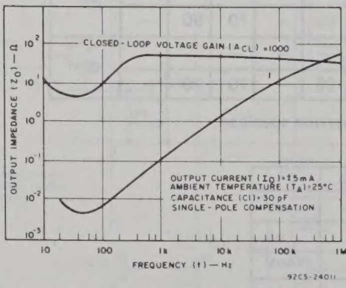


Fig. 12 — Closed-loop output impedance vs. frequency.

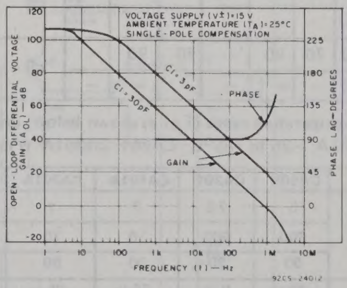


Fig. 13 — Voltage gain and phase lag vs. frequency.

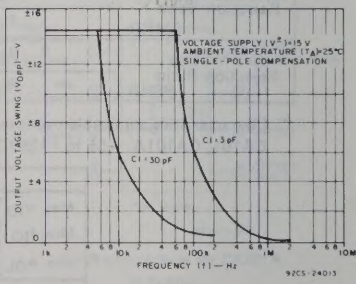


Fig. 14 — Output voltage swing vs. frequency.

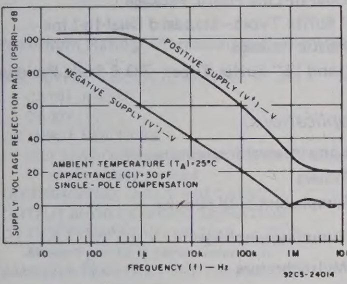


Fig. 15 — Supply voltage rejection ratio vs. frequency.

Two-Pole Compensation

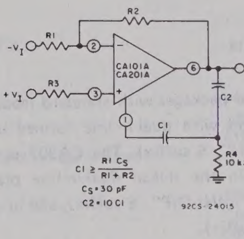


Fig. 16 — Test circuit employing two-pole compensation.

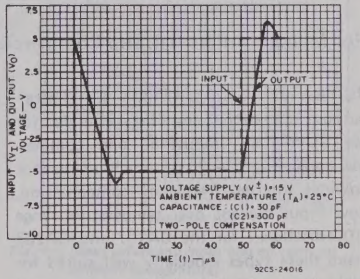


Fig. 17 — Voltage follower pulse response.

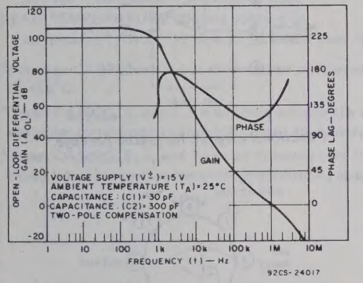


Fig. 18 — Voltage gain and phase lag vs. frequency.

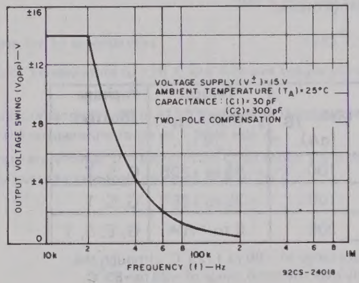


Fig. 19 — Output voltage swing vs. frequency.

Feed-Forward Compensation

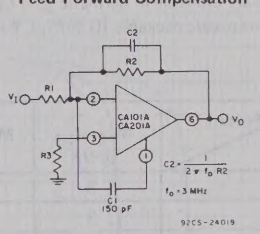


Fig. 20 — Test circuit employing feedforward compensation.

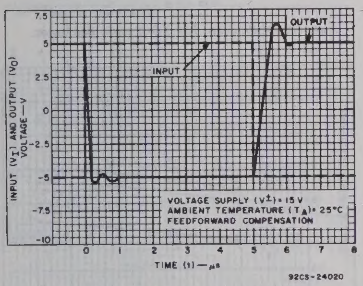


Fig. 21 — Inverter pulse response.

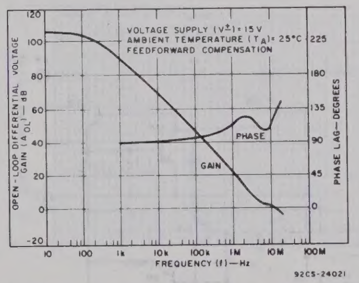


Fig. 22 — Voltage gain and phase lag vs. frequency.

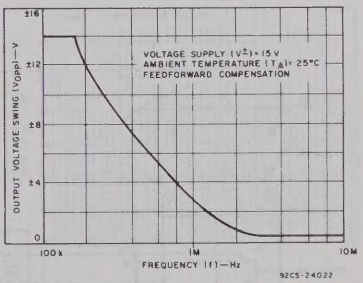


Fig. 23 — Output voltage swing vs. frequency.

CA101A AND CA201A

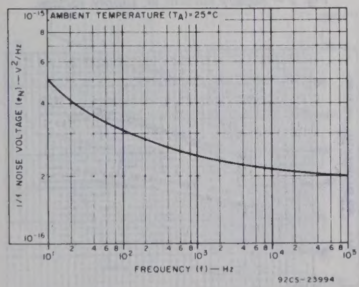


Fig. 24 — 1/f noise voltage vs. frequency.

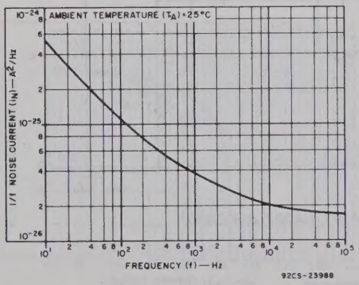


Fig. 25 — 1/f noise current vs. frequency.

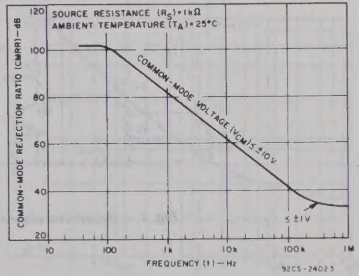


Fig. 26 — Common-mode rejection ratio vs. frequency.

CA107, CA207, CA307 Types

Operational Amplifiers

For Military, Industrial, and Commercial Applications

RCA-CA107, CA207, CA307 are general-purpose operational amplifiers intended for use in military, industrial, and commercial applications. A 30-pF on-chip capacitor provides internal frequency compensation. Low input current over temperature range (100 nA max.) for the CA107 and CA207 make these types especially well suited for applications such as long interval timers and sample-and-hold circuits.

All types are available in hermetic gold-CHIP dual-in-line plastic packages (G suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA307 is also available in the 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

The CA107, CA207, and CA307 are direct replacements for industry types 107, 207, and 307 in packages with similar terminal arrangements.

Feature / Type	Max. V_{IO} (mV)	Max. I_{IO} (nA)	Max. I_{IB} (nA)	Temp. Range (T_A) °C	Package (Suffix)
CA107	3	20	100	−55 to +125	G, S, T
CA207	3	20	100	−25 to +85*	G, S, T
CA307	10	70	300	0 to +70▲	G, E, S, T

*Types CA207G, S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temp. range of −25 to +85°C.

▲Types CA307G, E, S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temp. range of 0 to 70°C.

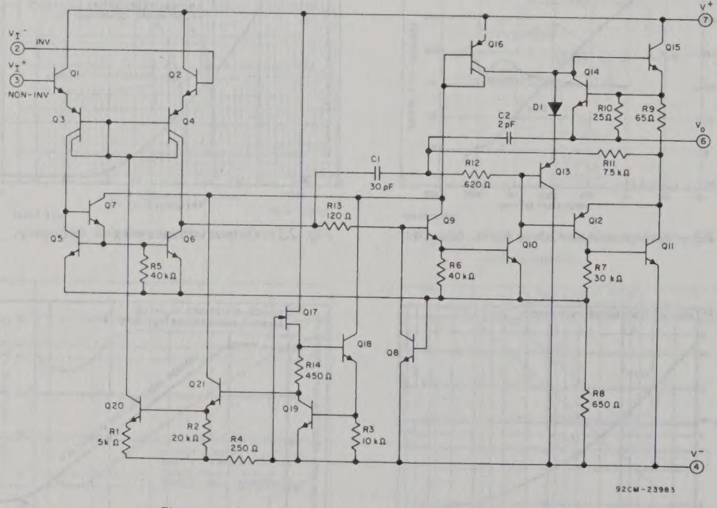


Fig. 1 – Schematic diagram of CA107, CA207, and CA307.

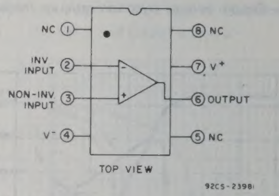
"G" Suffix Types—Hermetic Gold-CHIP in Dual-In-Line Plastic Package

"E" Suffix Types—Standard Dual-In-Line Plastic Package

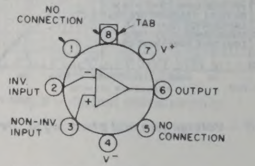
"T" and "S" Suffix Types—TO-5 Style Package

Applications:

- **Long-interval integrators**
- **Timers**
- **Sample-and-hold circuits**
- **Summing amplifiers**
- **Multivibrators**



Functional diagram for plastic package.



NOTE: PIN 4 IS CONNECTED TO CASE
TOP VIEW
92CS-23982

Functional diagram for TO-5 style packages.

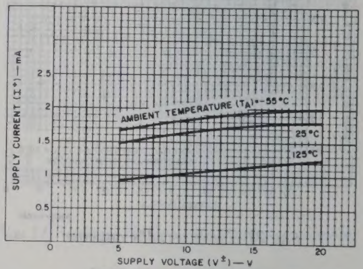


Fig. 2 – Supply current vs. supply voltage.

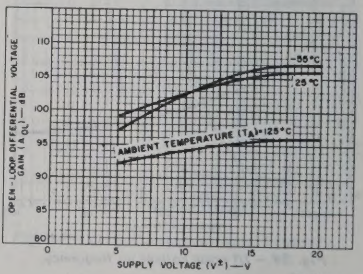


Fig. 3 – Open-loop differential voltage gain vs. supply voltage.

CA107, CA207, CA307 Types

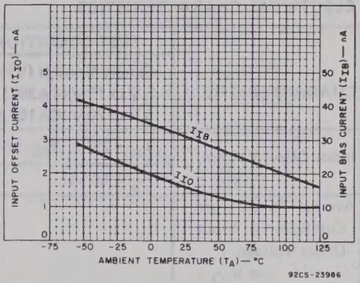
Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals):		
CA107, CA207	44	V
CA307	36	V
DC INPUT VOLTAGE	±15	V
(For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage)		
DIFFERENTIAL INPUT VOLTAGE	±30	V
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite	
DEVICE DISSIPATION UP TO T_A = 70°C	500	mW
Above T_A = 70°C Derate linearly at	6.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Operating – CA107	–55°C to +125°C	
CA207	–25°C to +85°C▲	
CA307	0°C to +70°C†	
Storage – All Types	–65°C to +150°C	
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C	

*For type CA307 continuous short circuit is allowed for Case Temperature to +70°C and ambient temperature to +55°C.

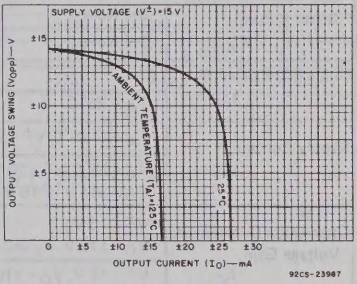
▲Types CA207G, S, and T can be operated over the temperature range of –55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of –25 to +85°C.

†Types CA307G, E, S, and T can be operated over the temperature range of –55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.



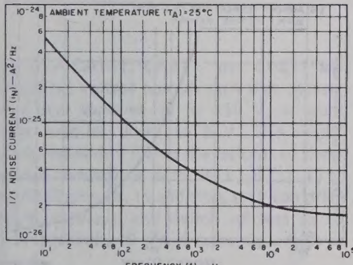
92CS-23986

Fig. 4 – Input offset and input bias currents vs. ambient temperature.



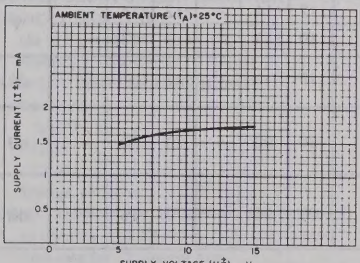
92CS-23987

Fig. 5 – Output voltage swing vs. output current.



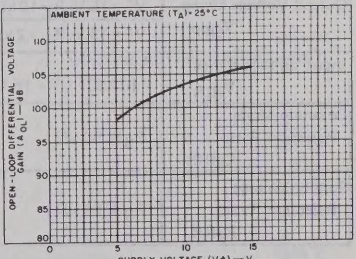
92CS-23988

Fig. 6 – 1/f noise current vs. frequency.



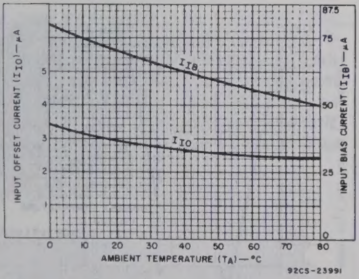
92CS-23989

Fig. 7 – Supply current vs. supply voltage.



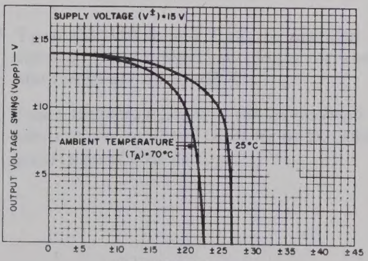
92CS-23990

Fig. 8 – Open-loop differential voltage gain vs. supply voltage.



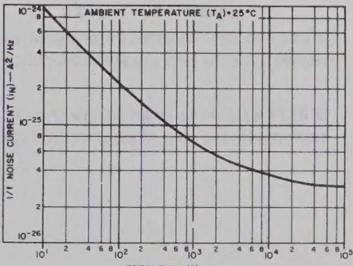
92CS-23991

Fig. 9 – Input offset and input bias current vs. ambient temperature.



92CS-23992

Fig. 10 – Output voltage swing vs. output current.



92CS-23993

Fig. 11 – 1/f noise current vs. frequency.

CA107, CA207, CA307 Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS▲ Supply Voltage ($V\pm$) = 5 V to 15 V (CA307) 5 V to 20 V (CA107,CA207)	LIMITS CA107 CA207			LIMITS CA307			UNITS
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	T_A = 25°C, $R_S \leq 50$ kΩ	–	0.7	2	–	2	7.5	mV
	$R_S \leq 50$ kΩ	–	–	3	–	–	10	
Average Temperature Coefficient of Input Offset Voltage, αV_{IO}		–	3	15	–	6	30	µV/°C
Input Offset Current, I_{IO}		–	–	20	–	–	70	nA
	T_A = 25°C	–	1.5	10	–	3	50	
Average Temperature Coefficient of Input Offset Current, αI_{IO}	See Note 1	–	0.01	0.1	–	0.01	0.3	nA/°C
	See Note 2	–	0.02	0.2	–	0.02	0.6	
Input Bias Current, I_{IB}		–	–	100	–	–	300	nA
	T_A = 25°C	–	30	75	–	70	250	
Supply Current, $I^{\pm}$	T_A = +125°C, $V^{\pm}$ = 20 V	–	1.2	2.5	–	–	–	mA
	T_A = 25°C, $V^{\pm}$ = 20 V, (CA307 $V^{\pm}$ = 15 V)	–	1.8	3	–	1.8	3	
Open-Loop Differential Voltage Gain, A_{OL}	$V^{\pm}$ = 15 V, V_O = ±10 V, $R_L \geq 2$ kΩ	25	–	–	15	–	–	V/mV
	$V^{\pm}$ = 15 V, V_O = ±10 V $R_L \geq 2$ kΩ, T_A = 25°C	50	160	–	25	160	–	
Input Resistance, R_I	T_A = 25°C	1.5	4	–	0.5	2	–	MΩ
Output Voltage Swing, V_{OPP}	$V^{\pm}$ = 15 V, R_L=10 kΩ	±12	±14	–	±12	±14	–	V
	$V^{\pm}$ = 15 V, R_L = 2 kΩ	±10	±13	–	±10	±13	–	
Input Voltage Range, V_{ICR}	$V^{\pm}$ = 20 V, (CA307 $V^{\pm}$ = 15 V)	±15	–	–	±12	–	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 50$ kΩ	80	96	–	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq 50$ kΩ	80	96	–	70	96	–	dB

Note 1: For CA107, +25, to +125°C; For CA207, +25 to +85°C: For CA307, +25 to 70°C.

Note 2: For CA107, –55 to +25°C; For CA207, –25 to +25°C: For CA307, 0 to +25°C.

▲ Characteristics applicable over operating temperature range as shown below unless otherwise specified.

CA107 – T_A = –55 to +125°C
CA207 – T_A = –25 to +85°C
CA307 – T_A = 0 to 70°C

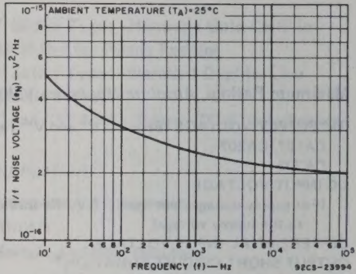


Fig. 12 – 1/f noise voltage vs. frequency.

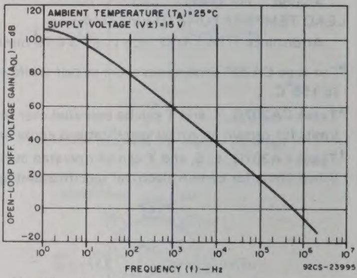


Fig. 13 – Open-loop differential voltage gain vs. frequency.

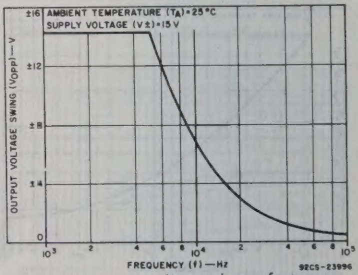


Fig. 14 – Output voltage swing vs. frequency.

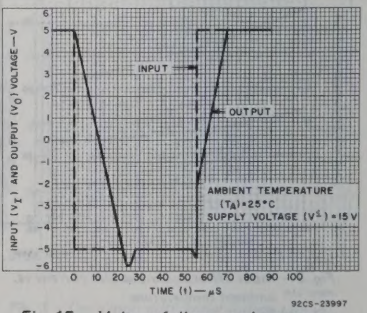


Fig. 15 – Voltage follower pulse response.

CA111, CA211, CA311 Types

Voltage Comparators

For Commercial and Industrial Applications

"G" Suffix Types—Hermetic Gold-CHIP in Dual-In-Line Plastic Package

"E" Suffix Types—Standard Dual-In-Line Plastic Package

"T" and "S" Suffix Types—TO-5 Style Package

Applications

- **Multivibrators**
- **Positive and negative peak detectors**
- **Crystal oscillators**
- **Zero-crossing detectors**
- **Solenoid, relay, and lamp drivers**

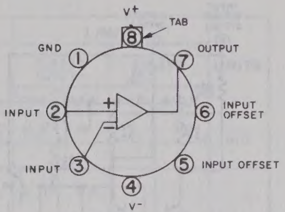
Features

- **Single- or dual-supply operation**
- **Power consumption — 135 mW at ±15 V**
- **Strobe capability**
- **Low input-offset current:**
  - **CA111, CA211 — 4 nA(typ.)**
  - **CA311 — 6 nA(typ.)**
- **Differential input-voltage range — ±30 V**
- **Directly interchangeable with National Semiconductor LM111, LM211, and LM311 Series types**

The RCA-CA111, CA211, and CA311 are monolithic voltage comparators that operate from dual supplies up to ±15 V, or from single supplies down to 5 V. This single-supply capability makes the outputs of these devices compatible with RTL, DTL, TTL, and MOS circuits. In addition, they can drive lamps or relays, and switch voltages up to 50 V (CA311, 40 V) at currents as high as 50 mA.

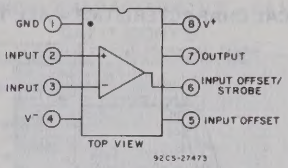
The inputs and the outputs of the CA111, CA211, and CA311 can be isolated from system ground, allowing the output to drive loads referred to ground, V^+, or V^-.

All types are available in hermetic gold-CHIP dual-in-line plastic packages (G suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA311 is also available in the 8-lead dual-in-line plastic package ("MINI-DIP",E suffix), and in chip form (H suffix).



NOTE : PIN 4 IS CONNECTED TO CASE 92CS-24379

Functional diagram for TO-5 style package.



Functional diagram for plastic package.

Feature / Type	Max. V_{IO} (mV)	Max. I_{IO} (nA)	Max. I_{IB} (nA)	Temp. Range (T_A) °C	Package (Suffix)
CA111	3	10	100	−55 to +125	G,S,T
CA211	3	10	100	−25 to +85▲	G,S,T
CA311	7.5	50	250	0 to +70 †	G,E,S,T

MAXIMUM RATINGS, ***Absolute Maximum Values at T_A = 25°C***

DC SUPPLY VOLTAGE (between V^+ and V^- terminals) . . . . 36 V
DC INPUT VOLTAGE* . . . . ±15 V
DIFFERENTIAL INPUT VOLTAGE . . . . ±30 V
OUTPUT TO NEGATIVE SUPPLY VOLTAGE ($V_{7\text{-}4}$):
CA111, CA211 . . . . 50 V
CA311 . . . . 40 V
GROUND TO NEGATIVE SUPPLY VOLTAGE ($V_{1\text{-}4}$) . . . . 30 V
OUTPUT SHORT-CIRCUIT DURATION . . . . 10 s
DEVICE DISSIPATION:
Up to T_A = 25°C . . . . 500 mW
Above T_A = 25°C . . . . derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating:
CA111 . . . . −55 to +125°C
CA211 . . . . −25 to +85°C▲
CA311 . . . . 0 to +70°C †
Storage, all types . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm)
from case for 10 seconds max. . . . . +265°C

*This rating applies for ±15 V supplies. The positive input-voltage limit is 30 V above the negative supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

▲ Types CA211G,S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of −25 to +85°C.

† Types CA311G,E,S and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.

CA111, CA211, CA311 Types

TYPICAL CHARACTERISTICS – ALL TYPES

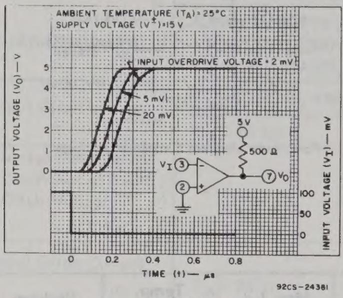


Fig. 1 — Response time for various input overdrive voltages—positive input.

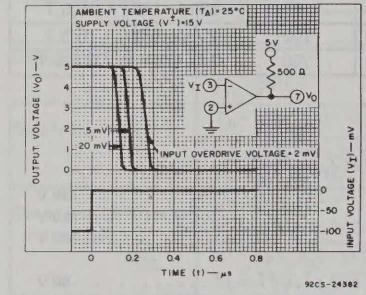


Fig. 2 — Response time for various input overdrive voltages—negative input.

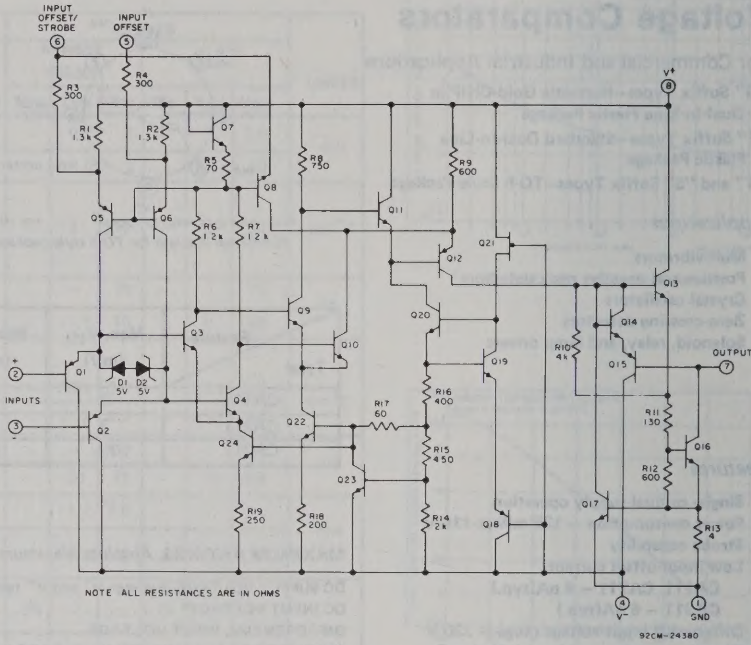


Fig. 3 — Schematic diagram for CA111, CA211, and CA311.

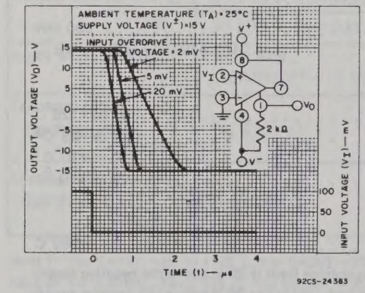


Fig. 4 — Response time for various input overdrive voltages—positive input.

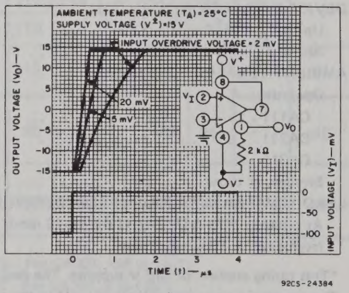


Fig. 5 — Response time for various input overdrive voltages—negative input.

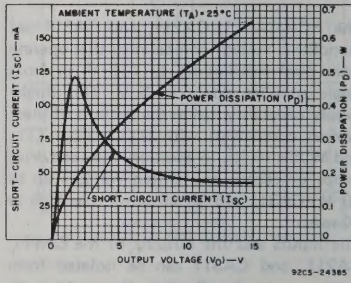


Fig. 6 — Output limiting characteristics.

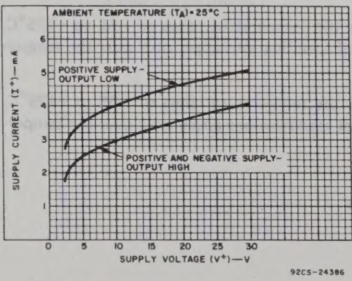


Fig. 7 — Supply current vs. supply voltage.

TYPICAL CHARACTERISTCS –CA111, CA211

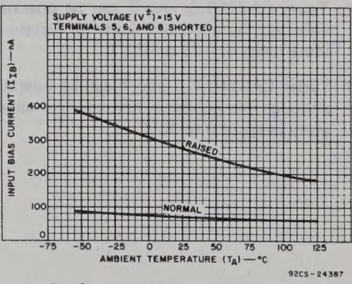


Fig. 8 — Input bias current vs. ambient temperature.

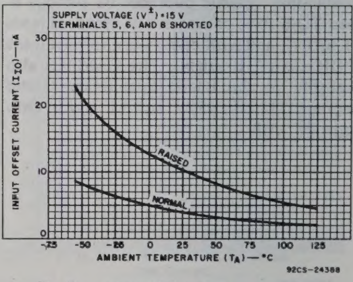


Fig. 9 — Input offset current vs. ambient temperature.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS SUPPLY VOLTAGE ($V^{\pm}$) = 15 V UNLESS OTHERWISE SPECIFIED		LIMITS CA111 CA211 TYP.	CA111 CA211 MAX.	CA311 TYP.	CA311 MAX.	UNITS
Input Offset Voltage, V_{IO}	$R_s \leqslant 5\ k\Omega$, Note 2	T_A=25°C	0.7	3	2	7.5	mV
		Note 1	–	4	–	10	
Saturation Voltage	V_I = –5 mV, I_o = 50 mA (For CA311, $V_I \leqslant$ –10 mV)	T_A=25°C	0.75	1.5	–	–	V
	$V^+ \geqslant$4.5 V, V^-=0, $V_I \leqslant$ –6 mV, $I_{SINK} \leqslant$ 8 mA (For CA311, $V_I \leqslant$ –10 mV)	Note 1	0.23	0.4	–	–	
Input Voltage Range, V_{IPP}		Note 1	±14	–	±14	–	V
Input Offset Current, I_{IO}	Note 2	T_A = 25°C	4	10	6	50	nA
		Note 1	–	20	–	70	
Input Bias Current, I_{IB}	Note 2	T_A=25°C	60	100	100	250	nA
		Note 1	–	150	–	300	
Positive Supply Current; I^+		T_A = 25°C	5.1	6	5.1	7.5	mA
Negative Supply Current, I^-		T_A=25°C	4.1	5	4.1	5	mA
Output Leakage Current	$V_I \geqslant$5 mV, V_o = 35 V (For CA311, $V_I \geqslant$ –10 mV)	T_A=25°C	0.2	10	–	–	nA
		Note 1	0.1	0.5	–	–	μA
Strobe On Current		T_A=25°C	3	–	3	–	mA
Voltage Gain, A		T_A=25°C	200	–	200	–	V/mV
Response Time	100 mV Input Step with 5 mV overdrive voltage	T_A=25°C	200	–	200	–	ns

Note 1: Ambient temperature (T_A) over applicable operating temperature range as shown below.

CA111	CA211	CA311
–55 to +125°C	–25 to +85°C	0 to +70°C

Note 2: The input offset characteristics given are the values required to drive the output to within 1 V of either supply with a 1-mA load. These characteristics define an error band which takes into account the worst-case effects of voltage gain and input impedance. The input offset voltage, input offset current, and input bias current specifications apply for any supply voltage from a 5 V single supply up to a ±15 V dual supply.

TYPICAL CHARACTERISTICS – CA111, CA211 (CONT'D)

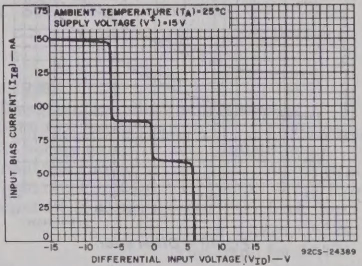


Fig. 10 – Input characteristcs.

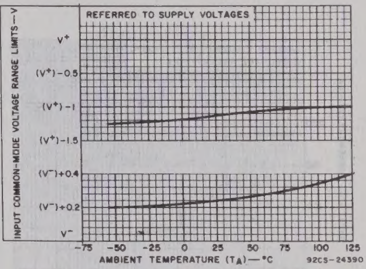


Fig. 11 – Common-mode voltage range limits vs. ambient temperature.

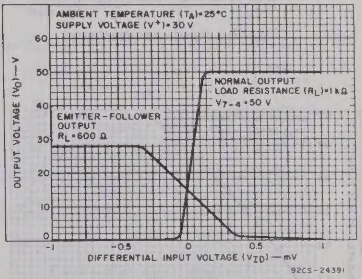


Fig. 12 – Transfer function.

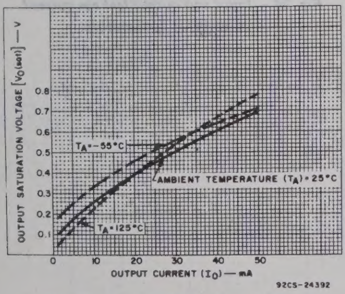


Fig. 13 – Output saturation voltage vs. output current.

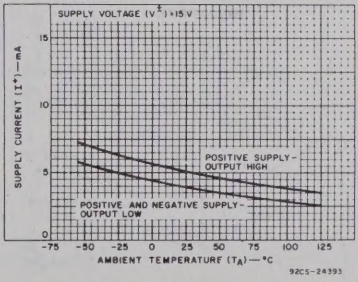


Fig. 14 – Supply current vs. ambient temperature.

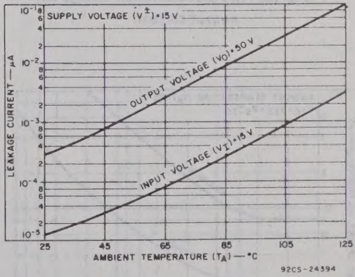


Fig. 15 – Input and output leakage current vs. ambient temperature.

CA111, CA211, CA311 Types

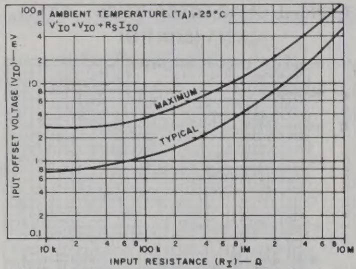


Fig. 16 – Offset error.

TYPICAL CHARACTERISTICS – CA311

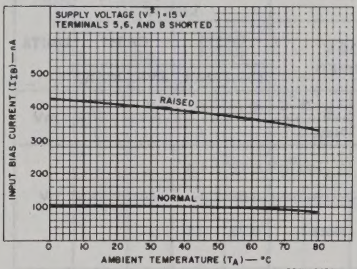


Fig. 17 – Input bias current vs. ambient temperature.

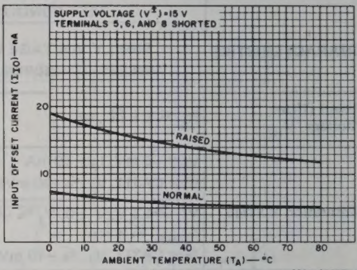


Fig. 18 – Input offset current vs. ambient temperature.

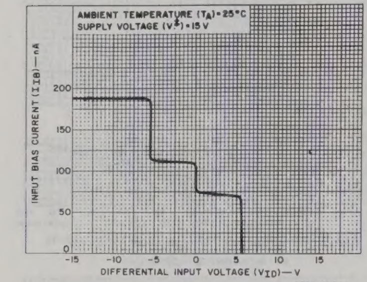


Fig. 19 – Input characteristics.

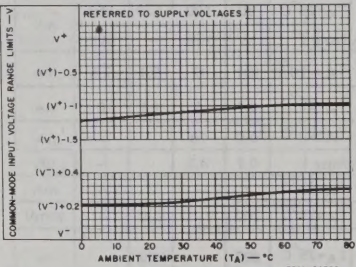


Fig. 20. – Common-mode voltage range limits vs. ambient temperature.

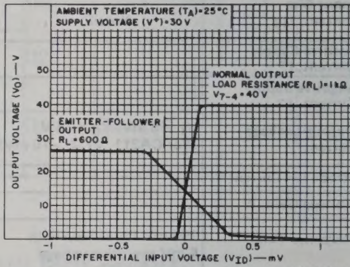


Fig. 21 – Transfer function.

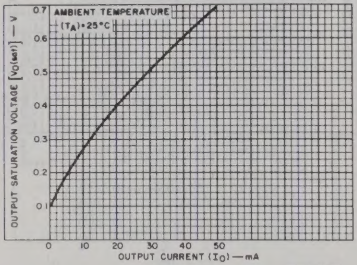


Fig. 22 – Output saturation voltage vs. output current.

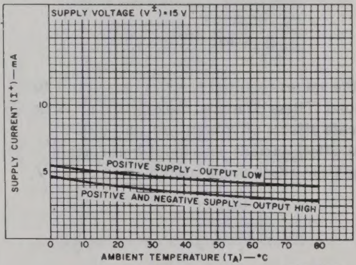


Fig. 23 – Supply current vs. ambient temperature.

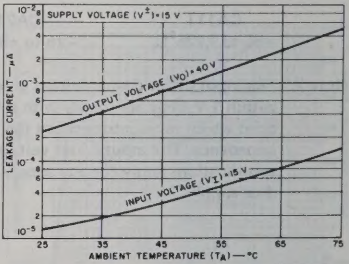


Fig. 24 – Input and output leakage current vs. ambient temperature.

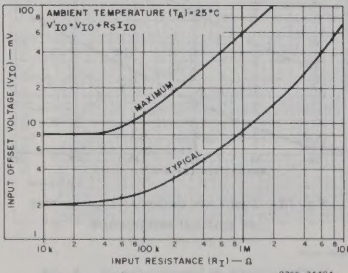


Fig. 25 – Offset error.

CA124, CA224, CA324 Types

"E" Suffix Types: Standard Dual-In-Line Plastic Package

"G" Suffix Types: Hermetic Gold-Chip Dual-In-Line Plastic Package

Quad Operational Amplifiers

For Commercial, Industrial, and Military Applications

The RCA-CA124, -CA224, and -CA324 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specifically to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range of from 0 V to $V^+ - 1.5$ V (single-supply operation) make the CA124, CA224, and CA324 suitable for battery operation.

The CA124, CA224, and CA324 are supplied in a 14-lead dual-in-line plastic package (E suffix), or in a hermetic gold-chip 14-lead dual-in-line plastic package (G suffix) to provide true hermetic performance. The CA324 is also available in chip form (H suffix), and as a hermetic gold-chip (HG suffix).

Features:

■ **Operation from single or dual supplies**	
■ **Unity-gain bandwidth**	**1 MHz (typ.)**
■ **DC voltage gain**	**100 dB (typ.)**
■ **Input bias current**	**45 nA (typ.)**
■ **Input offset voltage**	**2 mV (typ.)**
■ **Input offset current**	**5 nA (typ.) for CA224, CA324** **3 nA (typ.) for CA124**
■ **Replacement for industry types 124, 224, 324**	

Applications

- **Summing amplifiers**
- **Multivibrators**
- **Oscillators**
- **Transducer amplifiers**
- **DC gain blocks**

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE	32 V or ±16 V
DIFFERENTIAL INPUT VOLTAGE	±32 V
INPUT VOLTAGE	–0.3 V to +32 V
INPUT CURRENT ($V_I < -0.3$ V)†	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leqslant 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	–55 to +125°C
Storage	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

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*The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device.

†This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than –0.3 V dc.

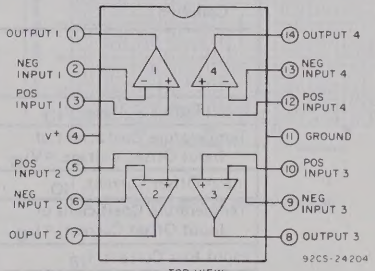


Fig. 1 – Functional diagram.

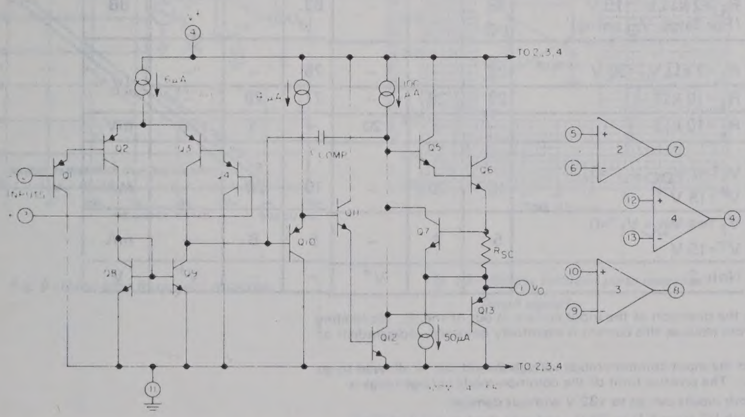


Fig. 2–Schematic diagram–one of four operational amplifiers.

CA124, CA224, CA324 Types

ELECTRICAL CHARACTERISTICS (Values apply for each operational amplifier)

CHARACTERISTIC	TEST CONDITIONS Supply Voltage (V^+) = 5 V Unless Otherwise Specified	CA124 LIMITS			CA224, CA324 LIMITS			UNITS
		Min.	Typ.	Max.	Min.	Typ.	Max.	
	T_A = 25°C							
Input Offset Voltage, V_{IO}	Note 3	–	2	5	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	$V^+-1.5$	0	–	$V^+-1.5$	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+=30 V	0	–	$V^+-1.5$	0	–	$V^+-1.5$	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	–	45	250	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	94	100	–	88	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	65	100	–	dB
Amplifier-to-Amplifier Coupling	f=1 to 20 kHz (Input referred)	–	–120	–	–	–120	–	dB
		T_A = –55 to +125°C			T_A = -40 to +85°C (CA224), T_A = 0 to 70°C (CA324)			
Input Offset Voltage, V_{IO}	Note 3	–	–	7	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_s = 0	–	7	–	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	300	–	–	500	nA
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.8	2	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+-2	0	–	V^+-2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	–	–	83	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L=2 kΩ, V^+=30 V	26	–	–	26	–	–	V
	R_L=10 kΩ	27	28	–	27	28	–	
Low-Level, V_{OL}	R_L=10 kΩ	–	5	20	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

TYPICAL CHARACTERISTICS CURVES

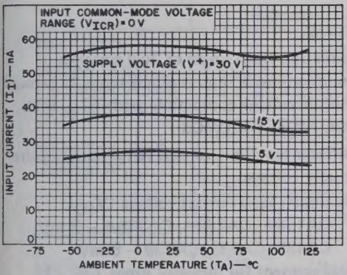


Fig. 3—Input current vs. ambient temperature.

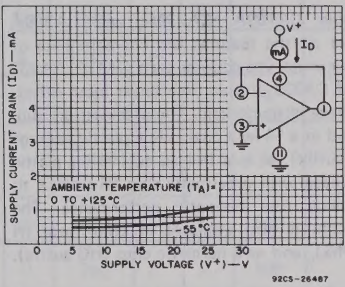


Fig. 4—Supply current drain vs. supply voltage.

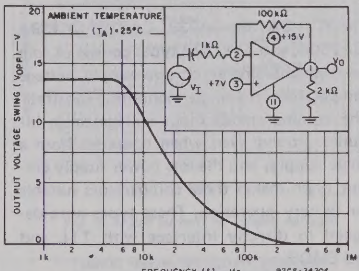


Fig. 5—Large-signal frequency response.

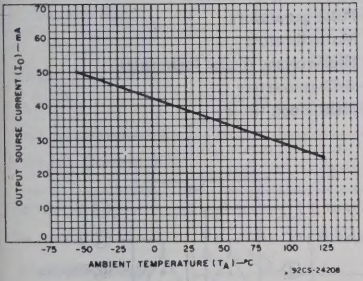


Fig. 6—Output current vs. ambient temperature.

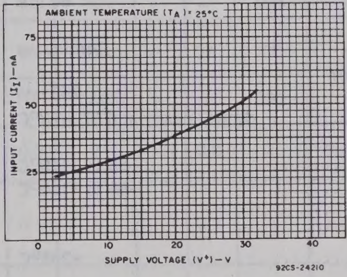


Fig. 7—Input current vs. supply voltage.

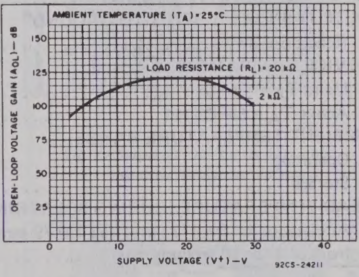


Fig. 8—Voltage gain vs. supply voltage.

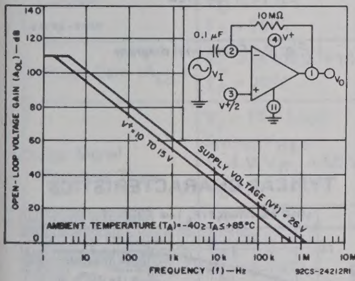


Fig. 9—Open-loop frequency response.

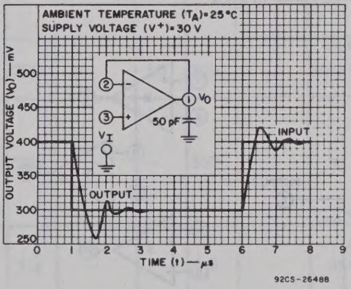


Fig. 10—Voltage follower pulse response (small signal).

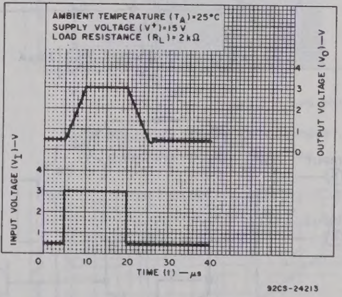


Fig. 11—Voltage follower pulse response.

CA139, CA239, CA339 Types

Quad Voltage Comparators

For Industrial, Commercial, and Military Applications

The RCA-CA139, -CA239, -CA339, -CA139A, -CA239A, and -CA339A types consist of four independent single- or dual-supply voltage comparators on a single monolithic substrate. The common-mode input voltage range includes ground even when operated from a single supply, and the low power supply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and and CMOS.

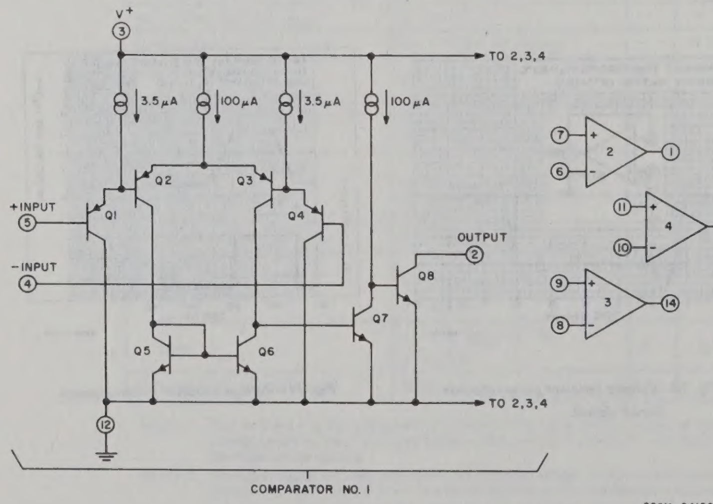
Types CA139A, CA239A, and CA339A have all the features and characteristics of their prototype counter parts CA139, CA239, and CA339 plus an even lower input-offset-voltage characteristic. These devices are supplied in a 14-lead dual-in-line plastic package (E suffix), or in a 14-lead dual-in-line plastic package with a hermetic chip (G suffix), to provide true hermetic performance. The CA339 is also available in chip form (H suffix), and as a hermetic chip (HG suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C:*

DC SUPPLY VOLTAGE	36 V or ±18 V
DC DIFFERENTIAL INPUT VOLTAGE	±36 V
INPUT VOLTAGE	−0.3 V to +36 V
INPUT CURRENT (V_I < −0.3 V)*	50 mA
OUTPUT SHORT CIRCUIT TO GROUND▲ (Single Supply)	Continuous
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

* Inputs must not go more negative than −0.3 V.

▲Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current independent of V^+ is approximately 20 mA.



92CM-24150R1

Fig. 1 —Schematic diagram.

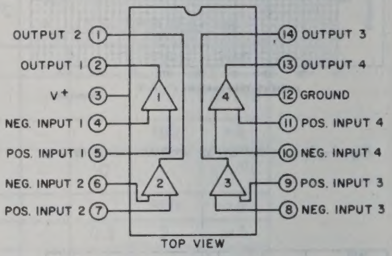
"E" Suffix Types: Standard Dual-In-Line Plastic Package
"G" Suffix Types: Hermetic Gold-Chip Dual-In-Line Plastic Package

Features:

- **Operation from single or dual supplies**
- **Common-mode input-voltage range to ground**
- **Output voltage compatible with TTL, DTL, ECL, MOS, and CMOS**
- **Differential input-voltage range equal to the supply voltage**
- **Maximum input-offset voltage (V_{IO}):**
  - **CA139A, CA239A, CA339A – 2 mV**
  - **CA139, CA239, CA339 – 5 mV**
- **Replacement for industry types 139, 239 339, 139A, 239A, and 339A**

Applications:

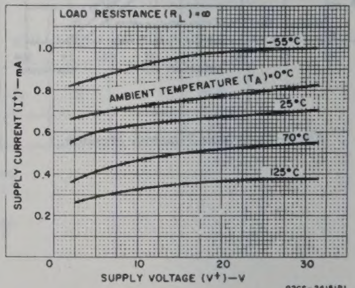
- **Square-wave generators**
- **Time-delay generators**
- **Pulse generators**
- **Multivibrators**
- **High-voltage digital logic gates**
- **A/D converters**
- **MOS clock timers**



92CS-24149

Fig. 2 —Functional diagram.

TYPICAL CHARACTERISTICS



92CS-24151R1

Fig. 3—Supply current vs. supply voltage.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	$V^+ = 5$ V Unless otherwise indicated		CA139			CA139A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage (V_{IO}) At Output Switch Point V ≅ 1.4 V	V_{REF} = 1.4 V, $R_S = 0$	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ⩾0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	$V_I^- = 1$ V, $V_I^+ = 0$ V, $I_{SINK} \leqslant$ 4 mA	25°C	–	250	500	–	250	500	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	$V^+ -1.5$	0	–	$V^+ -1.5$	V
		Note 1	0	–	$V^+ -2$	0	–	$V^+ -2$	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	3	25	–	3	25	nA
		Note 1	–	–	100	–	–	100	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	100	–	25	100	nA
		Note 1	–	–	300	–	–	300	
Supply Current (I^+)	$R_L = \infty$ on all comparators, $T_A = 25°C$		–	0.8	2	–	0.8	2	mA
Output Leakage Current	$V_I^+ \geqslant 1$ V, $V_I^- = 0$, $V_O = 5$ V	25°C	–	0.1	–	–	0.1	–	nA
	$V_I^+ \geqslant 1$ V, $V_I^- = 0$, $V_O = 30$ V	Note 1	–	–	1	–	–	1	µA
Output Sink Current	$V_I^- \geqslant 1$ V, $V_I^+ = 0$, $V_O \leqslant +1.5$ V, $T_A = 25°C$		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	$R_L \geqslant 15$ kΩ, $V^+ = 15$ V, $T_A = 25°C$		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, $V_{RL} = 50$ V, $R_L = 5.1$ kΩ, $T_A = 25°C$		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	$V_{RL} = 5$ V, $R_L = 5.1$ kΩ, $T_A = 25°C$		–	1.3	–	–	1.3	–	µs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.

CA139 CA139A	(–55 to +125°C)	CA239 CA239A	(–25 to +85°C)	CA339 CA339A	(0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is $(V^+) - 1.5$ V, but either or both inputs can go to +30 V without damage.

TYPICAL CHARACTERISTICS (Cont'd)

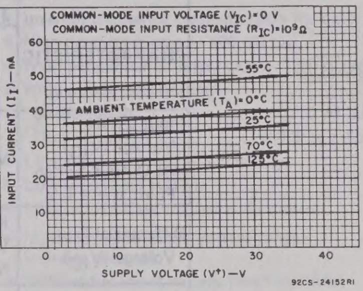


Fig. 4—Input current vs. supply voltage.

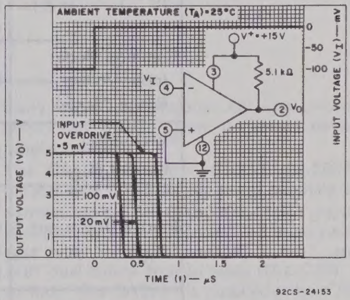


Fig. 5—Response time for various input overdrives—negative transition.

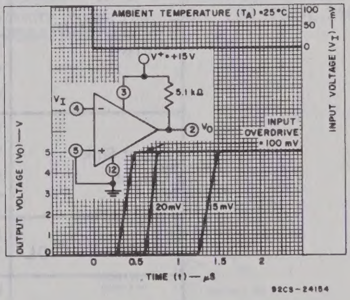


Fig. 6—Response time for various input overdrives—positive transition.

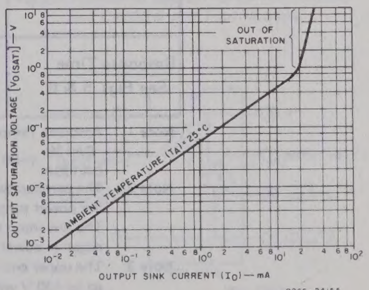


Fig. 7—Output saturation voltage vs. output sink current.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	$V^+ = 5$ V Unless otherwise indicated		CA239, CA339			CA239A, CA339A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage (V_{IO}) At Output Switch Point $V \cong 1.4$ V	$V_{REF} = 1.4$ V, $R_S = 0$	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ≥0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	$V_I^- = 1$ V, $V_I^+ = 0$ V, $I_{SINK} \leq$ 4 mA	25°C	–	250	500	–	250	500	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	$V^+ - 1.5$	0	–	$V^+ - 1.5$	V
		Note 1	0	–	$V^+ - 2$	0	–	$V^+ - 2$	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	5	50	–	5	50	nA
		Note 1	–	–	150	–	–	150	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	250	–	25	250	nA
		Note 1	–	–	400	–	–	400	
Supply Current (I^+)	$R_L = \infty$ on all comparators, $T_A = 25°C$		–	0.8	2	–	0.8	2	mA
Output Leakage Current	$V_I^+ \geq 1$ V, $V_I^- = 0$, $V_O = 5$ V	25°C	–	0.1	–	–	0.1	–	nA
	$V_I^+ \geq 1$ V, $V_I^- = 0$, $V_O = 30$ V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	$V_I^- \geq 1$ V, $V_I^+ = 0$, $V_O \leq +1.5$ V, $T_A = 25°C$		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	$R_L \geq 15$ kΩ $V^+ = 15$ V, $T_A = 25°C$		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, $V_{REF} = +1.4$ V, $V_{RL} = 50$ V, $R_L = 5.1$ kΩ, $T_A = 25°C$		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	$V_{RL} = 5$ V, $R_L = 5.1$ kΩ, $T_A = 25°C$		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.
CA139 CA139A (−55 to +125°C) CA239 CA239A (−25 to +85°C) CA339 CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than −0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is $(V^+) - 1.5$ V, but either or both inputs can go to +30 V without damage.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

Dual Operational Amplifiers

For Commercial, Industrial, and Military Applications

Features:

- **Internal frequency compensation for unity gain**
- **High dc voltage gain – 100 dB typ.**
- **Wide bandwidth at unity gain – 1 MHz typ.**
- **Wide power supply range:**
  - **Single supply . . . . . . 3 to 30 V**
  - **Dual supplies . . . . . ± 1.5 to ± 15 V**
- **Low supply current – 1.5 mA typ.**
- **Low input bias current**
- **Low input offset voltage and current**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to V^+ range**
- **Large output voltage swing – 0 to V^+ –1.5 V**

The RCA-CA158, –CA158A, –CA258, –CA258A, –CA358, –CA358A, and CA-2904 types consist of two independent, high gain, internally frequency compensated operational amplifiers which are designed specifically to operate from a single power supply over a wide range of voltages. They may also be operated from split power supplies. The supply current is basically independent of the supply voltage over the recommended voltage range.

These devices are particularly useful in interface circuits with digital systems and can be operated from the single common 5 Vdc power supply. They are also intended for transducer amplifiers, dc gain blocks and many other conventional op amp circuits which can benefit from the single power supply capability.

The CA158, CA158A, CA258, CA258A, CA358 and CA358A types are supplied in hermetic gold-CHIP 8-lead dual-in-line plastic packages (G suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads (DIL-CAN, S suffix). The CA2904 is supplied only in the gold-CHIP plastic package (G suffix).

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are an equivalent to or a replacement for the industry types 158, 158A, 258, 258A, 358, 358A, and 2904.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE, V^+:	
CA2904	26 V or ± 13 V
Other Types	32 V or ± 16 V
DIFFERENTIAL INPUT VOLTAGE:	
CA2904	± 26 V
Other Types	± 32 V
INPUT VOLTAGE	–0.3 V to V^+ V
INPUT CURRENT ($V_I < -0.3$ V) + ...	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leqslant 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	630 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/^oC
AMBIENT TEMPERATURE RANGE:	
Operating	–55 to + 125^oC
Storage	–65 to + 150^oC
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 300 ^oC

+ This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than –0.3 V dc.

* The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

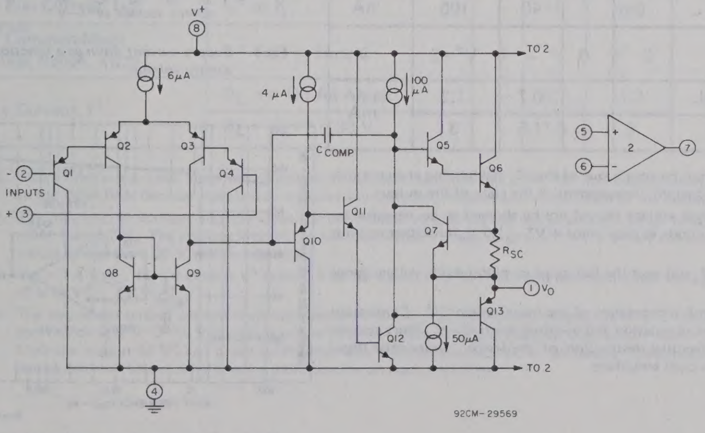


Fig. 1 – Schematic diagram – one of two operational amplifiers.

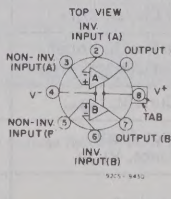


Fig.2 – Functional diagram for CA158, CA258, and CA358 S- and T-suffix types.

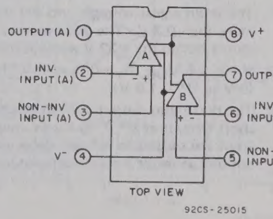


Fig.3 – Functional diagram for CA158, CA258, CA358, and CA2904 G-suffix types.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS Supply Voltage (V^+) = 5 V Unless Otherwise Specified	LIMITS CA158A (G, T, S)			UNITS
		Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	1	2	mV
Output Voltage Swing, V_{OPP}	$R_L = 2\ k\Omega$	0	–	$V^+ - 1.5$	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, $V^+ = 30$ V	0	–	$V^+ - 1.5$	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	10	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	20	50	nA
Output Current (Source), I_O	$V_I^+ = +1$ V, $V_I^- = 0$ V, $V^+ = 15$ V	20	40	–	mA
Output Current (Sink), I_O	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V^+ = 15$ V	10	20	–	mA
	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V_O = 200$ mV	12	50	–	μA
Short Circuit Output Current	$R_L = 0$ (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq 2\ k\Omega$, $V^+ = 15$ V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –55 to +125°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	$R_s = 0$	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	$V^+ = 30$ V, Note 2	0	–	$V^+ - 2$	V
Supply Current, I^+	$R_L = \infty$ On All Ampl.	–	0.7	1.2	mA
	$R_L = \infty$, $V^+ = 30$ V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: $V_O = 1.4\ V_{DC}$, $R_s = 0\ \Omega$ with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

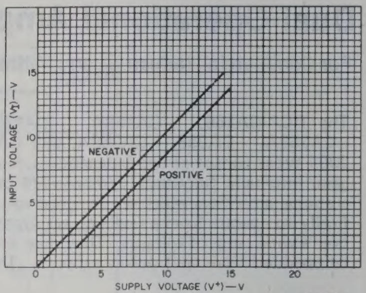


Fig.4 – Input voltage range as a function of supply voltage.

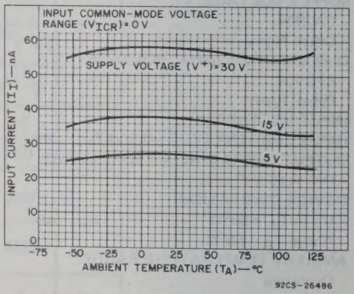


Fig.5 – Input current as a function of ambient temperature.

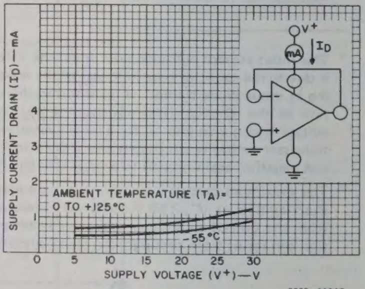


Fig.6 – Supply current drain as a function of supply voltage.

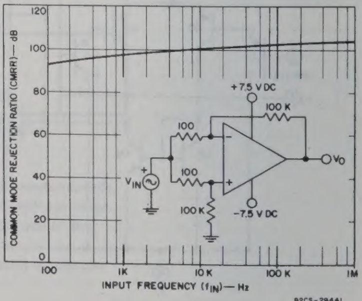


Fig.7 – Common mode rejection ratio as a function of input frequency.

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS Supply Voltage (V^+) = 5 V Unless Otherwise Specified	LIMITS CA258A (G, T, S) Min.	Typ.	Max.	UNITS
	$T_A = 25^oC$				
Input Offset Voltage, V_{IO}	Note 3	–	1	3	mV
Output Voltage Swing, V_{OPP}	$R_L = 2\ k\Omega$	0	–	$V^+ -1.5$	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, $V^+ = 30$ V	0	–	$V^+ -1.5$	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	15	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	40	80	nA
Output Current (Source), I_O	$V_I^+ = +1$ V, $V_I^- = 0$ V, $V^+ = 15$ V	20	40	–	mA
Output Current (Sink), I_O	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V^+ = 15$ V	10	20	–	mA
	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V_O = 200$ mV	12	50	–	μA
Short Circuit Output Current	$R_L = 0$ (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant 2\ k\Omega$, $V^+ = 15$ V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRP	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	$T_A = -25$ to $+85^oC$				
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	$R_s = 0$	–	7	15	$\mu V/^oC$
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	$pA/^oC$
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	$V^+ = 30$ V, Note 2	0	–	$V^+ - 2$	V
Supply Current, I^+	$R_L = \infty$ On All Ampl.	–	0.7	1.2	mA
	$R_L = \infty$, $V^+ = 30$ V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: $V_O = 1.4\ V_{DC}$, $R_s = 0\ \Omega$ with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

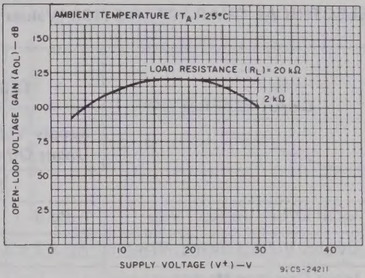


Fig.8 — Voltage gain as a function of supply voltage.

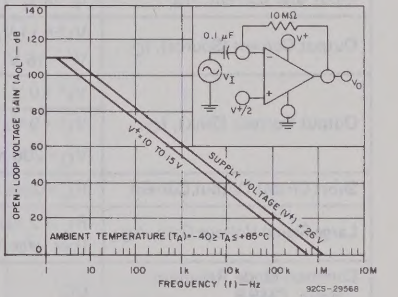


Fig.9 — Open-loop frequency response.

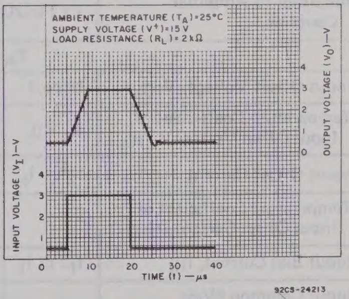


Fig.10 — Voltage follower pulse response.

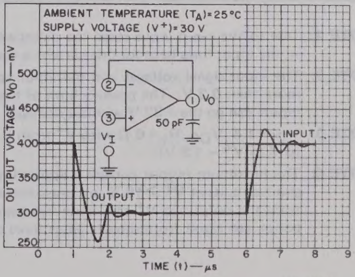


Fig.11 — Voltage follower pulse response (small signal).

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA358A (G, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
$T_A = 25^oC$					
Input Offset Voltage, V_{IO}	Note 3	–	2	3	mV
Output Voltage Swing, V_{OPP}	$R_L = 2\ k\Omega$	0	–	$V^+ -1.5$	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, $V^+ = 30$ V	0	–	$V^+ -1.5$	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	100	nA
Output Current (Source), I_O	$V_I^+ = +1$ V, $V_I^- = 0$ V, $V^+ = 15$ V	20	40	–	mA
Output Current (Sink), I_O	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V^+ = 15$ V	10	20	–	mA
	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V_O = 200$ mV	12	50	–	µA
Short Circuit Output Current	$R_L = 0$ (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant 2\ k\Omega$, $V^+ = 15$ V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
$T_A = 0$ to $+70^oC$					
Input Offset Voltage, V_{IO}	Note 3	–	–	5	mV
Temperature Coefficient of Input Offset Voltage, $\propto V_{IO}$	$R_s = 0$	–	7	20	µV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	75	nA
Temperature Coefficient of Input Offset Current, $\propto I_{IO}$		–	10	300	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	200	nA
Input Common-Mode Voltage Range, V_{ICR}	$V^+ = 30$ V, Note 2	0	–	V^+-2	V
Supply Current, I^+	$R_L = \infty$ On All Ampl.	–	0.7	1.2	mA
	$R_L = \infty$, $V^+ = 30$ V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: $V_O = 1.4\ V_{DC}$, $R_s = 0\ \Omega$ with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of thedevice. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

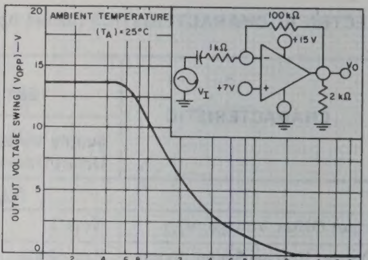


Fig. 12 – Large-signal frequency response.

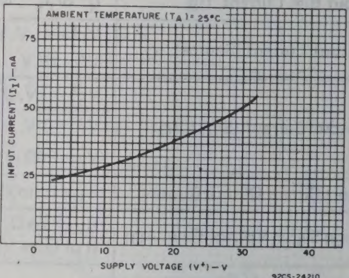


Fig. 13 – Input current as a function of supply voltage.

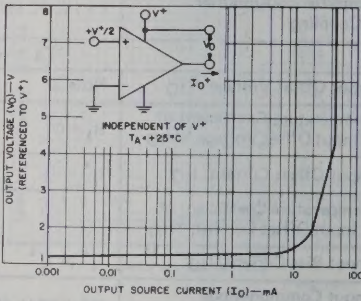


Fig. 14 – Output source current characteristics.

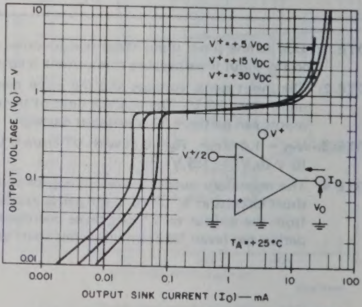


Fig. 15 – Output sink current characteristics.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS Supply Voltage (V^+) = 5 V Unless Otherwise Specified	LIMITS CA158 (G, T, S) CA258 (G, T, S) Min.	Typ.	Max.	UNITS
$T_A = 25^oC$					
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	$R_L = 2\ k\Omega$	0	–	$V^+ -1.5$	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, $V^+ = 30$ V	0	–	$V^+ -1.5$	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	$V_I^+ = +1$ V, $V_I^- = 0$ V, $V^+ = 15$ V	20	40	–	mA
Output Current (Sink), I_O	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V^+ = 15$ V	10	20	–	mA
	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V_O = 200$ mV	12	50	–	µA
Short Circuit Output Current	$R_L = 0$ (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant 2\ k\Omega$, $V^+ = 15$ V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
$T_A = -55$ to $+125^oC$ (CA158); $T_A = -25$ to $+85^oC$ (CA258)					
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, $\propto V_{IO}$	$R_s = 0$	–	7	–	$\mu V/^oC$
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, $\propto I_{IO}$		–	10	–	$pA/^oC$
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	300	nA
Input Common-Mode Voltage Range, V_{ICR}	$V^+ = 30$ V, Note 2	0	–	$V^+ -2$	V
Supply Current, I^+	$R_L = \infty$ On All Ampl.	–	0.7	1.2	mA
	$R_L = \infty$, $V^+ = 30$ V	–	1.5	3	

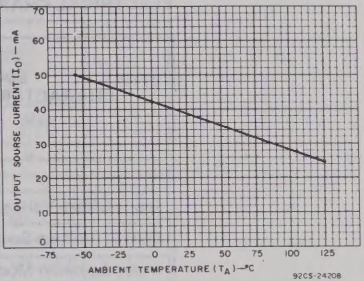


Fig. 16 – Output current as a function of ambient temperature.

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: $V_O = 1.4\ V_{DC}$, $R_s = 0\ \Omega$ with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS Supply Voltage (V^+) = 5 V Unless Otherwise Specified	LIMITS CA358 (G, T, S)			UNITS
		Min.	Typ.	Max.	
	$T_A = 25^\circ C$				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	$R_L = 2\ k\Omega$	0	–	$V^+ -1.5$	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, $V^+ = 30$ V	0	–	$V^+ -1.5$	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	$V_I^+ = +1$ V, $V_I^- = 0$ V, $V^+ = 15$ V	20	40	–	mA
Output Current (Sink), I_O	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V^+ = 15$ V	10	20	–	mA
	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V_O = 200$ mV	12	50	–	μA
Short Circuit Output Current	$R_L = 0$ (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant 2\ k\Omega$, $V^+ = 15$ V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	$T_A = 0$ to $+70^\circ C$				
Input Offset Voltage, V_{IO}	Note 3	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	$R_s = 0$	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	$V^+ = 30$ V, Note 2	0	–	$V^+ -2$	V
Supply Current, I^+	$R_L = \infty$ On All Ampl.	–	0.7	1.2	mA
	$R_L = \infty$, $V^+ = 30$ V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: $V_O = 1.4\ V_{DC}$, $R_s = 0\ \Omega$ with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA2904G			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	$T_A = 25^oC$				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	$R_L \geqslant 10\ k\Omega$	0	–	$V^+ - 1.5$	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, $V^+ = 30$ V	0	–	$V^+ - 1.5$	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	$V_I^+ = +1$ V, $V_I^- = 0$ V, $V^+ = 15$ V	20	40	–	mA
Output Current (Sink), I_O	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V^+ = 15$ V	10	20	–	mA
Short Circuit Output Current	$R_L = 0$ (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant 2\ k\Omega$, $V^+ = 15$ V (For large V_O swing)	–	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	50	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	50	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	$T_A = -40$ to $+85^oC$				
Input Offset Voltage, V_{IO}	Note 3	–	–	10	mV
Temperature Coefficient of Input Offset Voltage, $\propto V_{IO}$	$R_s = 0$	–	7	–	$\mu V/^oC$
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	45	200	nA
Temperature Coefficient of Input Offset Current, $\propto I_{IO}$		–	10	–	$pA/^oC$
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	$V^+ = 30$ V, Note 2	0	–	$V^+ - 2$	V
Supply Current, I^+	$R_L = \infty$ On All Ampl.	–	0.7	1.2	mA
	$R_L = \infty$, $V^+ = 30$ V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: $V_O = 1.4\ V_{DC}$, $R_s = 0\ \Omega$ with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA555, CA555C Types

Timers

For Timing Delays & Oscillator Applications in Commercial, Industrial, and Military Equipment

The RCA-CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the waveform signal, and the output of these circuits can source or sink up to a 200-milliampere current or drive TTL circuits.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	18	V
DEVICE DISSIPATION:		
Up to T_A = 55°C	600	mW
Above T_A = 55°C Derate linearly	5	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating		
CA555	–55 to +125	°C
CA555C	0 to 70	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

The CA555 and CA555C are supplied in hermetic IC Gold-CHIP 8-lead dual-in-line plastic packages (G Suffix), standard 8-lead TO-5 style packages (T suffix), 8-lead TO-5 style packages with dual-in-line formed leads (DIL-CAN, S suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), and in chip form (H suffix). These types are direct replacements for industry types in packages with similar terminal arrangements e.g.SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

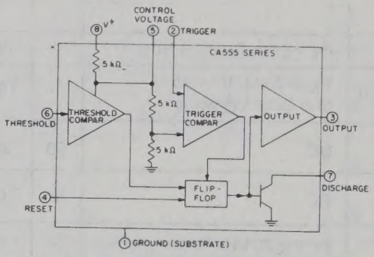


Fig. 1 – Functional diagram of the CA555 series.

CA555G, CA555CG:
Hermetic Gold-CHIP 8-Lead Dual-In-Line Plastic Package (MINI-DIP)

CA555T, CA555CT:
Standard 8-Lead TO-5 Style Package

CA555S, CA555CS:
Standard 8-Lead TO-5 Style Package With Formed Leads (DIL-CAN)

CA555E, CA555CE:
8-Lead Dual-In-Line Plastic Package (MINI-DIP)

Features:

- **Accurate timing from microseconds through hours**
- **Astable and monostable operation**
- **Adjustable duty cycle**
- **Output capable of sourcing or sinking up to 200 mA**
- **Output capable of driving TTL devices**
- **Normally ON and OFF outputs**
- **High-temperature stability –0.005%/°C**
- **Directly interchangeable with SE555, NE555, MC1555, and MC1455**

Applications:

- **Precision timing**
- **Sequential timing**
- **Time-delay generation**
- **Pulse generation**
- **Pulse-width and position modulation**
- **Pulse detector**

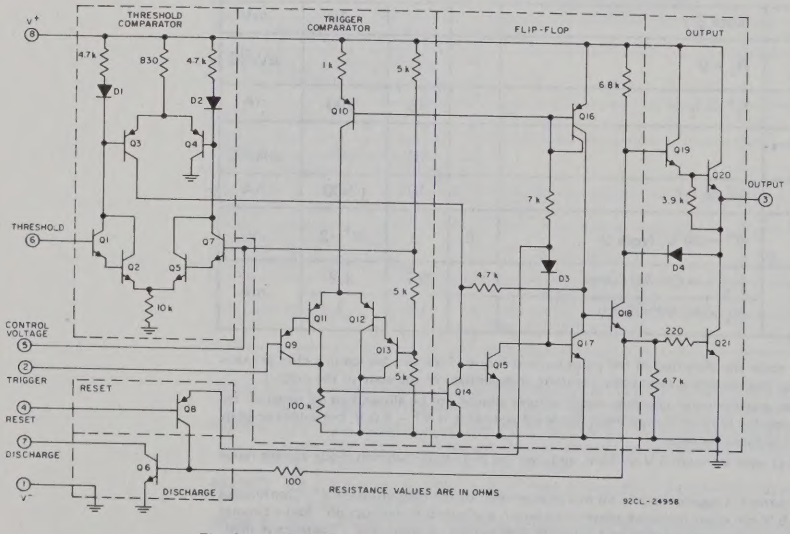
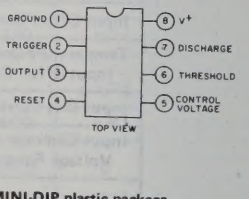
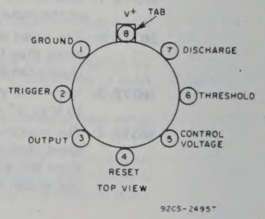


Fig. 2 – Schematic diagram of the CA555 and CA555C.



a. MINI-DIP plastic package
TO-5 style package with formed leads



b. TO-5 style package

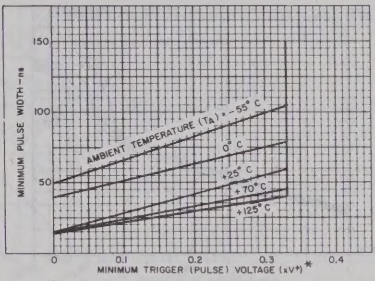
Fig. 3 – Terminal assignment diagrams.

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$, $V^+ = 5$ to 15 V unless otherwise specified*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA555			CA555C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
DC Supply Voltage, V^+		4.5	–	18	4.5	–	16	V
DC Supply Current (Low State)*, I^+	$V^+ = 5$ V, $R_L = \infty$	–	3	5	–	3	6	mA
	$V^+ = 15$ V, $R_L = \infty$	–	10	12	–	10	15	mA
Threshold Voltage, V_{TH}		–	$(2/3)V^+$	–	–	$(2/3)V^+$	–	V
Trigger Voltage	$V^+ = 5$ V	1.45	1.67	1.9	–	1.67	–	V
	$V^+ = 15$ V	4.8	5	5.2	–	5	–	
Trigger Current		–	0.5	–	–	0.5	–	μA
Threshold Current▲, I_{TH}		–	0.1	0.25	–	0.1	0.25	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		–	0.1	–	–	0.1	–	mA
Control Voltage Level	$V^+ = 5$ V	2.9	3.33	3.8	2.6	3.33	4	V
	$V^+ = 15$ V	9.6	10	10.4	9	10	11	V
Output Voltage Drop: Low State, V_{OL}	$V^+ = 5$ V $I_{SINK} = 5$ mA	–	–	–	–	0.25	0.35	V
	$I_{SINK} = 8$ mA	–	0.1	0.25	–	–	–	
	$V^+ = 15$ V $I_{SINK} = 10$ mA	–	0.1	0.15	–	0.1	0.25	V
	$I_{SINK} = 50$ mA	–	0.4	0.5	–	0.4	0.75	
	$I_{SINK} = 100$ mA	–	2.0	2.2	–	2.0	2.5	
	$I_{SINK} = 200$ mA	–	2.5	–	–	2.5	–	
High State, V_{OH}	$V^+ = 5$ V $I_{SOURCE} = 100$ mA	3.0	3.3	–	2.75	3.3	–	V
	$V^+ = 15$ V $I_{SOURCE} = 100$ mA	13.0	13.3	–	12.75	13.3	–	
	$I_{SOURCE} = 200$ mA	–	12.5	–	–	12.5	–	
Timing Error (Monostable): Initial Accuracy	R_1, R_2 = 1 to 100 kΩ C = 0.1 μF Tested at $V^+ = 5$ V, $V^+ = 15$ V	–	0.5	2	–	1	–	%
Frequency Drift with Temperature		–	30	100	–	50	–	p/m/°C
Drift with Supply Voltage		–	0.05	0.2	–	0.1	–	%/V
Output Rise Time, t_r		–	100	–	–	100	–	ns
Output Fall Time, t_f		–	100	–	–	100	–	ns

* When the output is in a high state, the dc supply current is typically 1 mA less than the low-state value.

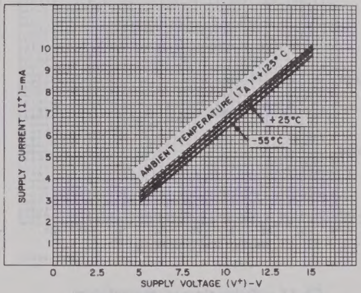
▲ The threshold current will determine the sum of the values of R_1 and R_2 to be used in Fig. 16 (astable operation): the maximum total $R_1 + R_2 = 20$ MΩ.



*WHERE x IS THE DECIMAL MULTIPLIER OF THE SUPPLY VOLTAGE

92CS-24960

Fig. 4 – Minimum pulse width vs. minimum trigger voltage.



92CS-24961

Fig. 5 – Supply current vs. supply voltage.

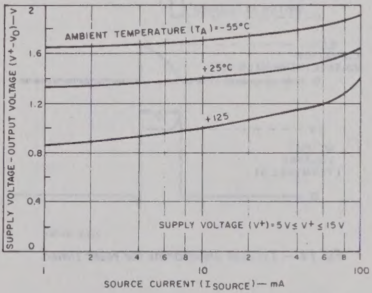


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Fig. 6 – Output voltage drop (high state) vs. source current.

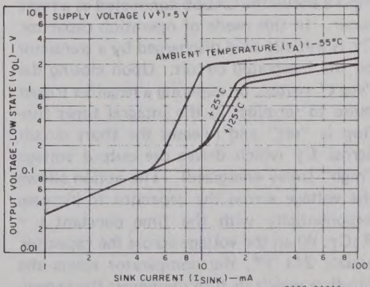

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Fig.7 – Output voltage-low state vs. sink current at $V^+ = 5$ V.

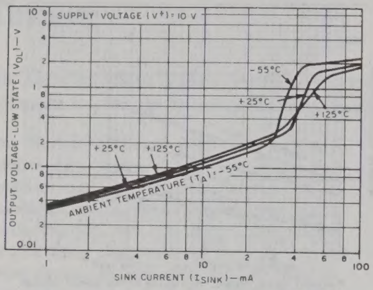


Fig.8 – Output voltage-low state vs. sink current at $V^+ = 10$ V.

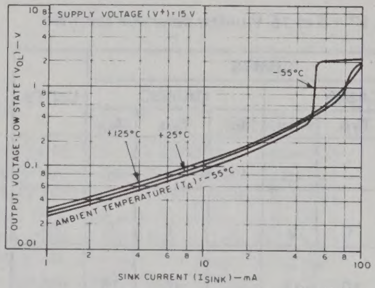


Fig.9 – Output voltage-low state vs. sink current at $V^+ = 15$ V.

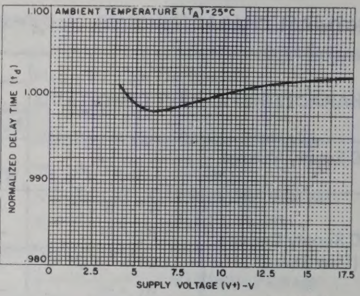


Fig.10 – Delay time vs. supply voltage.

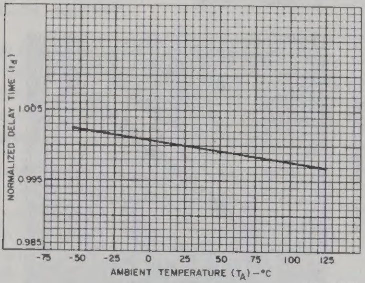


Fig.11 – Delay time vs. temperature.

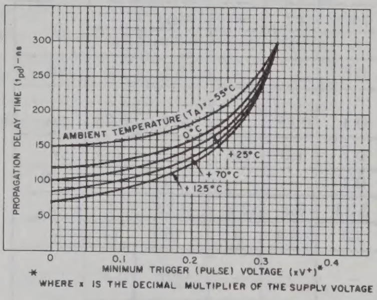


Fig.12 – Propagation delay time vs. trigger voltage.

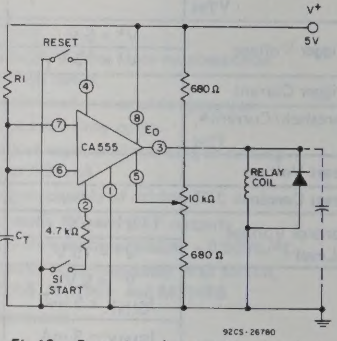


Fig.13 – Reset timer (monostable operation).

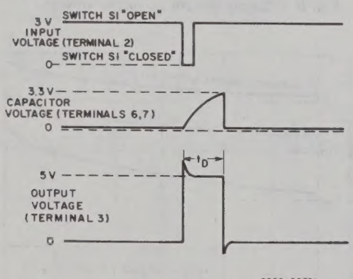


Fig.14 – Typical waveforms for reset timer.

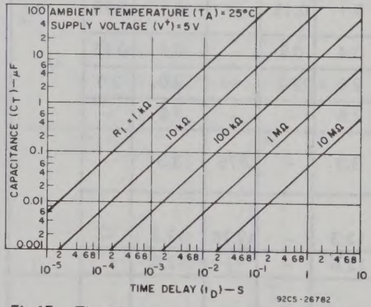


Fig.15 – Time delay vs. resistance and capacitance.

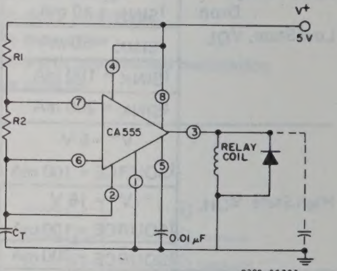


Fig.16 – Repeat cycle timer (astable operation).

TYPICAL APPLICATIONS

Reset Timer (Monostable Operation)

Fig.13 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the time constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.

Since the charge rate and threshold level of the comparator are both directly proportional to V^+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1 volt change in V^+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Fig.14 shows the typical waveforms generated during this mode of operation, and Fig.15 gives the family of time delay curves with variations in R_1 and C_T.

Repeat Cycle Timer (Astable Operation)

Fig.16 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R_1 and R_2;

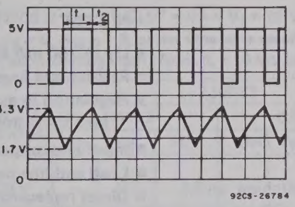
$$T = 0.693(R_1 + 2R_2)C_T = t_1 + t_2$$

where $t_1 = 0.693(R_1 + R_2)\,C_T$
and $t_2 = 0.693(R_2)C_T$

The duty cycle is:

$$\frac{t_2}{t_1 + t_2} = \frac{R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Fig. 17. Fig. 18 gives the family of curves of free running frequency with variations in the value of $(R_1 + 2R_2)$ and C_T.



Top Trace: Output voltage (2V/div. and 0.5 ms/div.)

Bottom Trace: Capacitor voltage (1 V/div. and 0.5 ms/div.)

Fig. 17 — Typical waveforms for repeat cycle timer.

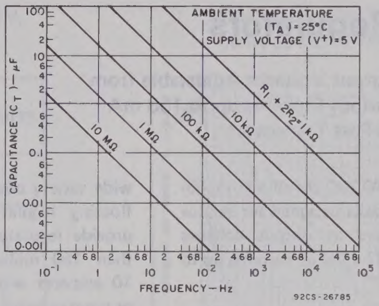


Fig. 18 — Free running frequency of repeat cycle timer with variation in capacitance and resistance.

CA723 Types
Voltage Regulators

For Regulated Output Voltages Adjustable from 2 V to 37 V at Output Currents up to 150 mA Without External Pass Transistors

RCA-CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2 to 37 volts at currents up to 150 milliamperes.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150 milliamperes and in excess of 10 amperes with the use of suitable n-p-n or p-n-p external pass transistors.

The CA723 and CA723C are supplied in the 10-lead TO-5-style ceramic package (T suffix), and the 14-lead dual-in-line plastic package (E suffix), and are direct replacements for industry types 723, 723C, μA723, and μA723C in packages with similar terminal arrangements. They are also available in chip form ("H" suffix).

All types are rated for operation over the full military-temperature range of −55°C to +125°C.

Features:

- **Up to 150 mA output current**
- **Positive and negative voltage regulation**
- **Regulation in excess of 10A with suitable pass transistors**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.03%**
- **Direct replacement for 723 and 723C industry types**
- **Adjustable output voltage: 2 to 37 V**

Applications:

- **Series and shunt voltage regulator**
- **Floating regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Temperature controller**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals)	40	V
PULSE VOLTAGE FOR 50-ms PULSE WIDTH (Between V^+ and V^- Terminals)	50	V
DIFFERENTIAL INPUT–OUTPUT VOLTAGE	40	V
DIFFERENTIAL INPUT VOLTAGE:		
Between Inverting and Non-Inverting Inputs	±5	V
Between Non-Inverting Input and V^-	8	V
CURRENT FROM ZENER DIODE TERMINAL (V_Z)	25	mA
CURRENT FROM VOLTAGE REFERENCE TERMINAL (V_{REF})	15	mA
DEVICE DISSIPATION:		
Up to T_A = 25°C –		
CA723T, CA723CT	800	mW
CA723E, CA723CE	1000	mW
Above T_A = 25°C –		
CA723T, CA723CT Derate linearly	6.3	mW/°C
CA723E, CA723CE Derate linearly	8.3	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering): At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

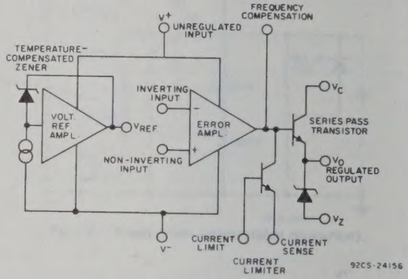


Fig. 1 – Functional diagram of the CA723 and CA723C.

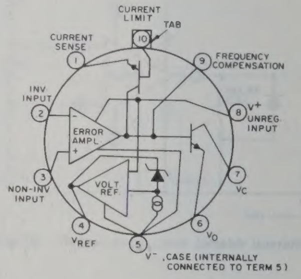


Fig. 2 – Terminal arrangement of the CA723T and CA723CT in the TO-5 style package.

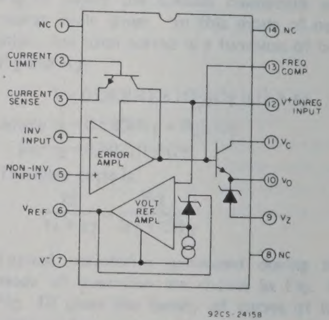


Fig. 3 – Terminal arrangement of the CA723E and CA723CE in the dual-in-line plastic package.

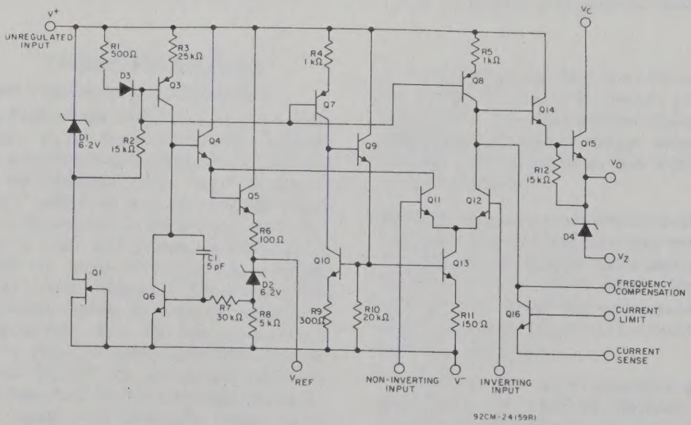


Fig. 4 – Equivalent schematic diagram of the CA723 and CA723C.

ELECTRICAL CHARACTERISTICS at T_A = 25 C, $V^+ = V_C = V_I$ = 12 V, V^- = 0, V_O = 5 V, I_L = 1 mA, C_1 = 100 pF, C_{REF} = 0, R_{SCP} = 0, unless otherwise specified. Divider impedance R_1R_2 R_1+R_2 at non-inverting input, Term. 5, = 10 kΩ (see Fig. 23).

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Regulator Current, I_Q	I_L = 0, V_I = 30 V	–	2.3	3.5	–	2.3	4	mA
Input Voltage Range, V_I		9.5	–	40	9.5	–	40	V
Output Voltage Range, V_O		2	–	37	2	–	37	V
Differential Input-Output Voltage, V_I-V_O		3	–	38	3	–	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (See Note 1)	V_I = 12 to 40 V	–	0.02	0.2	–	0.1	0.5	%V_O
	V_I = 12 to 15 V	–	0.01	0.1	–	0.01	0.1	
	V_I = 12 to 15 V, T_A = −55 to +125°C	–	–	0.3	–	–	–	
	V_I = 12 to 15 V, T_A = 0 to 70°C	–	–	–	–	–	0.3	
Load Regulation (See Note 1)	I_L = 1 to 50 mA	–	0.03	0.15	–	0.03	0.2	%V_O
	I_L = 1 to 50 mA, T_A = −55 to +125°C	–	–	0.6	–	–	–	
	I_L = 1 to 50 mA, T_A = 0 to 70°C	–	–	–	–	–	0.6	
Output-Voltage Temp. Coefficient, $\wedge V_O$	T_A = −55 to +125°C	–	0.002	0.015	–	–	–	%/°C
	T_A = 0 to 70°C	–	–	–	–	0.003	0.015	
Ripple Rejection (See Note 2)	f = 50 Hz to 10 kHz	–	74	–	–	74	–	dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF	–	86	–	–	86	–	
Short-Circuit Limiting Current, I_{LIM}	R_{SCP} = 10 Ω, V_O = 0	–	65	–	–	65	–	mA
Equivalent Noise RMS Output Voltage, V_N (See Note 2)	BW = 100 Hz to 10 kHz, C_{REF} = 0	–	20	–	–	20	–	μV
	BW = 100 Hz 10 kHz, C_{REF} = 5 μF	–	2.5	–	–	2.5	–	

Note 1: Line and load regulation specifications are given for condition of a constant chip temperature. For high-dissipation conditions, temperature drifts must be separately taken into account.

Note 2: For C_{REF}, see Fig. 23.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

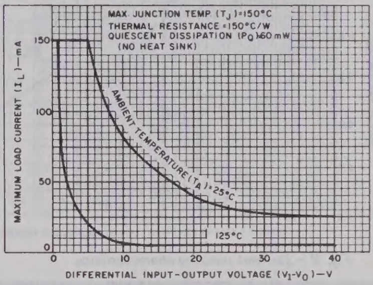


Fig. 5 – Max. load current vs differential input-output voltage.

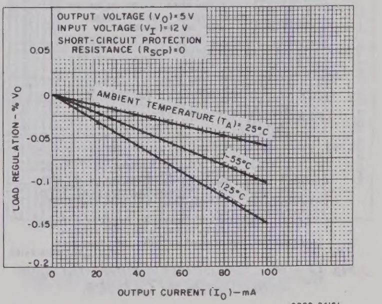


Fig. 6 – Load regulation without current limiting.

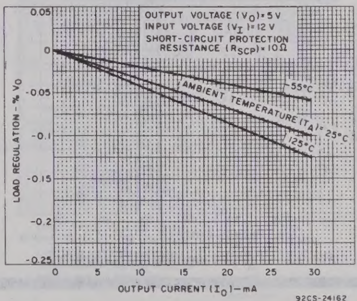


Fig. 7 – Load regulation with current limiting.

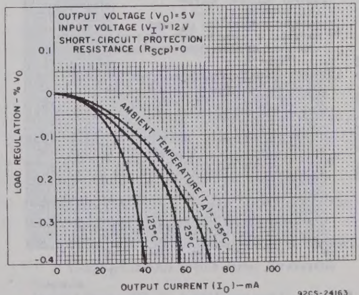


Fig. 8 – Load regulation with current limiting.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723 (Cont'd)

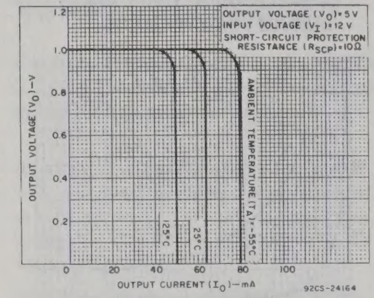


Fig. 9 – Current limiting characteristics.

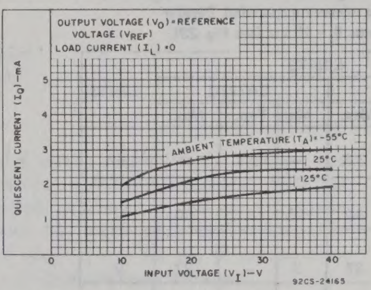


Fig. 10 – Quiescent current vs. input voltage.

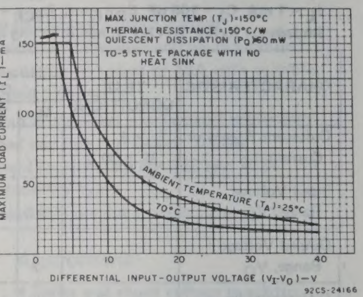


Fig. 11 – Max. load current vs differential input-output voltage CA723CT.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723C

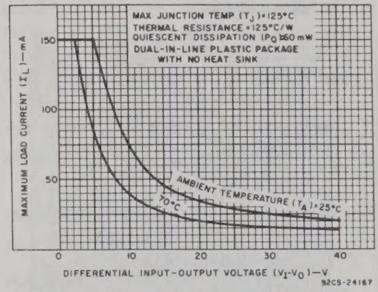


Fig. 12 – Max. load current vs differential input-output voltage for CA723CE.

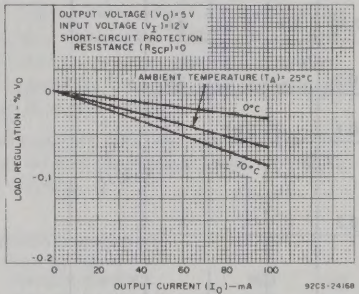


Fig. 13 – Load regulation without current limiting.

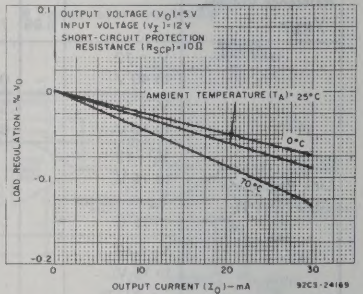


Fig. 14 – Load regulation with current limiting.

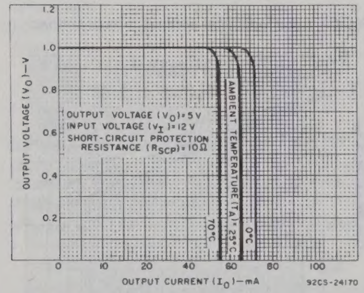


Fig. 15 – Current limiting characteristics.

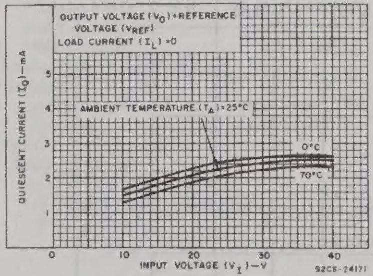


Fig. 16 – Quiescent current vs. input voltage.

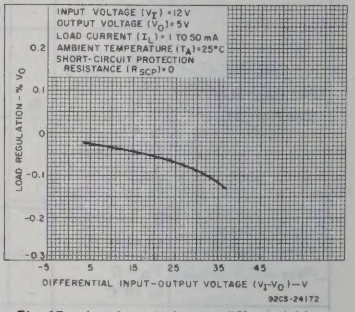


Fig. 17 – Load regulation vs. differential input-output voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPES CA723 AND CA723C

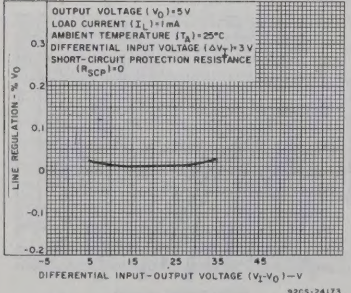


Fig. 18 – Line regulation vs. differential input-output voltage.

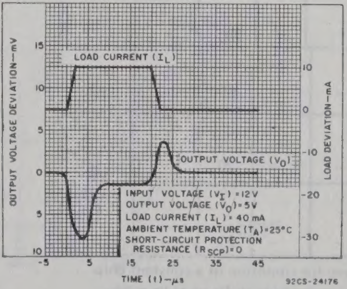


Fig. 19 – Line transient response.

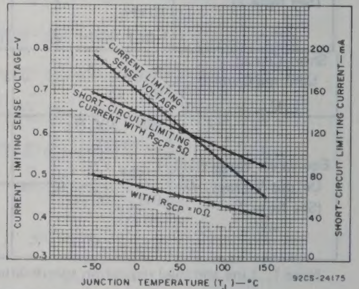


Fig. 20 – Current limiting characteristics vs. junction temperature.

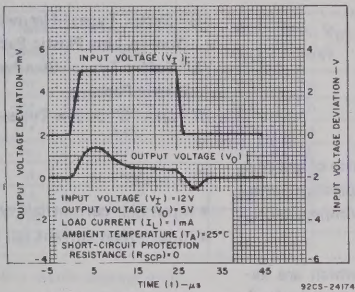


Fig. 21 – Load transient response.

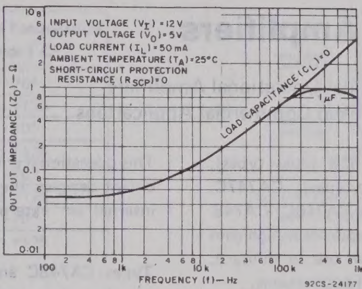
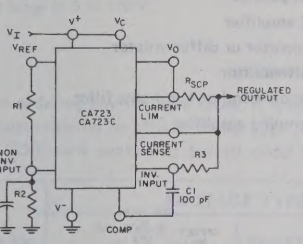


Fig. 22 – Output impedance vs. frequency.

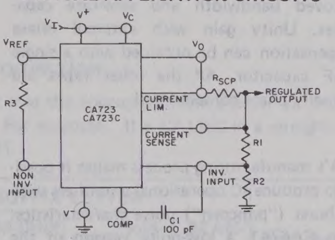
TYPICAL APPLICATION CIRCUITS



CIRCUIT PERFORMANCE DATA:
REGULATED OUTPUT VOLTAGE . . . . 5 V
LINE REGULATION (ΔV_I = 3 V) . . . . 0.5 mV
LOAD REGULATION (ΔI_L = 50 mA). . . 1.5 mV

Note: $R3 = \frac{R1\ R2}{R1+R2}$ for minimum temperature drift

Fig. 23 – Low-voltage regulator circuit (V_O = 2 to 7 volts).

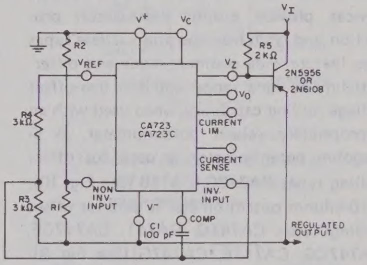


CIRCUIT PERFORMANCE DATA:
REGULATED OUTPUT VOLTAGE . . . 15 V
LINE REGULATION (ΔV_I = 3 V) . . . . 1.5 mV
LOAD REGULATION (ΔI_L = 50 mA) . . 4.5 mV

Note: $R3 = \frac{R1\ R2}{R1+R2}$ for minimum temperature drift

R3 may be eliminated for minimum component count.

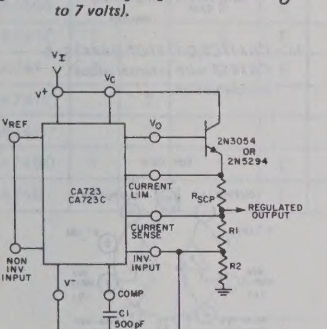
Fig. 24 – High-voltage regulator circuit (V_O = 7 to 37 volts).



CIRCUIT PERFORMANCE DATA:
REGULATED OUTPUT VOLTAGE . . . –15 V
LINE REGULATION (ΔV_I = 3 V) . . . . 1 mV
LOAD REGULATION (ΔI_L = 100 mA) . . 2 mV

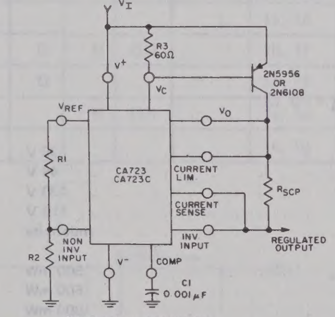
Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

Fig. 25 – Negative-voltage regulator circuit.



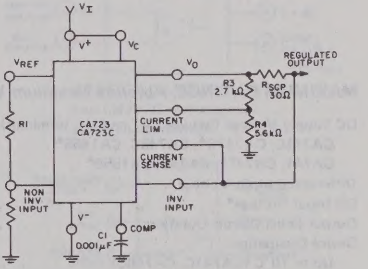
CIRCUIT PERFORMANCE DATA:
REGULATED OUTPUT VOLTAGE . . . 15 V
LINE REGULATION (ΔV_I = 3 V) . . . . 1.5 mV
LOAD REGULATION (ΔI_L = 1 A) . . . . 15 mV

Fig. 26 – Positive-voltage-regulator circuit (with external n-p-n pass transistor).



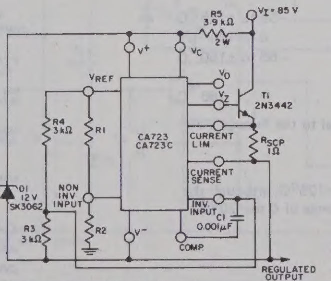
CIRCUIT PERFORMANCE DATA:
REGULATED OUTPUT VOLTAGE . . . 5 V
LINE REGULATION (ΔV_I = 3 V) . . . . 0.5 mV
LOAD REGULATION (ΔI_L = 1 A) . . . . 5 mV

Fig. 27 – Positive voltage-regulator circuit (with external p-n-p pass transistor).



CIRCUIT PERFORMANCE DATA:
REGULATED OUTPUT VOLTAGE . . . 5 V
LINE REGULATION (ΔV_I = 3 V) . . . 0.5 mV
LOAD REGULATION (ΔI_L = 10 mA). . . 1 mV
SHORT-CIRCUIT CURRENT . . . . 20 mA

Fig. 28 – Foldback current-limiting circuit.



Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

CIRCUIT PERFORMANCE DATA:
REGULATED OUTPUT VOLTAGE . . . 50 V
LINE REGULATION (ΔV_I = 20 V) . . . 15 mV
LOAD REGULATION (ΔI_L = 50 mA). . . 20 mV

Fig. 29 – Positive-floating regulator circuit.

CA741, CA747, CA748, CA1458, CA1558 Types

Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commercial Applications

"G" Suffix Types—Hermetic Gold-CHIP in Dual-In-Line Plastic Package
"E" Suffix Types—Standard Dual-In-Line Plastic Package
"T" and "S" Suffix Types—TO-5 Style Package

The RCA-CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 10); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747CG, CA747E, CA747G (See Fig. 9); and types CA1458, CA1558, CA747CT, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

RCA's manufacturing process makes it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your RCA Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

Features:

- **Input bias current (all types): 500 nA max.**
- **Input offset current (all types): 200 nA max.**

Applications:

- **Comparator**
- **DC amplifier**
- **Integrator or differentiator**
- **Multivibrator**
- **Narrow-band or band-pass filter**
- **Summing amplifier**

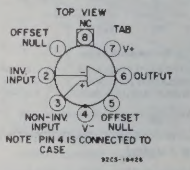
MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^\circ C$:*

DC Supply Voltage (between V$^+$ and V$^-$ terminals):	
CA741C, CA747C▲, CA748C, CA1458▲	36 V
CA741, CA747▲, CA748, CA1558▲	44 V
Differential Input Voltage	±30 V
DC Input Voltage*	±15 V
Output Short-Circuit Duration	Indefinite
Device Dissipation:	
Up to 70°C (CA741C, CA748C)	500 mW
Up to 75°C (CA741, CA748)	500 mW
Up to 30°C (CA747)	800 mW
Up to 25°C (CA747C)	800 mW
Up to 30°C (CA1558)	680 mW
Up to 25°C (CA1458)	680 mW
For Temperatures Indicated Above	Derate linearly 6.67 mW/°C
Voltage between Offset Null and V$^-$ (CA741C, CA741, CA747CE, CA747CG)	±0.5 V
Ambient Temperature Range:	
Operating – CA741, CA747E, CA748, CA1558	–55 to +125 °C
CA741C, CA747C, CA748C, CA1458	0 to +70 °C†
Storage	–65 to +150 °C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265 °C

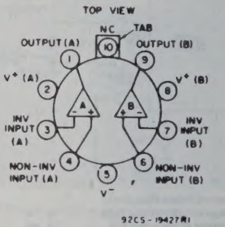
* If Supply Voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

▲ Voltage values apply for each of the dual operational amplifiers.

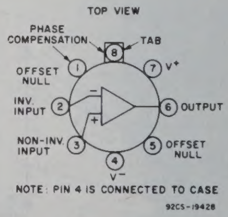
† All types in any package style can be operated over the temperature range of –55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.



1a.—CA741CS,CA741CT,CA741S, & CA741T with internal phase compensation.



1b.—CA747CT and CA747T with internal phase compensation.



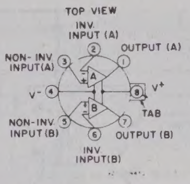
1c.—CA748CS, CA748CT,CA748S, and CA748T with external phase compensation.

Fig. 1 — Functional diagrams.

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)
CA1458	dual	int.	no	20k	6	0 to +70▲
CA1558	dual	int.	no	50k	5	−55 to +125
CA741C	single	int.	yes	20k	6	0 to +70▲
CA741	single	int.	yes	50k	5	−55 to +125
CA747C	dual	int.	yes*	20k	6	0 to +70▲
CA747	dual	int.	yes*	50k	5	−55 to +125
CA748C	single	ext.	yes	20k	6	0 to +70▲
CA748	single	ext.	yes	50k	5	−55 to +125

*In the 14-lead dual-in-line plastic package only.

▲All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

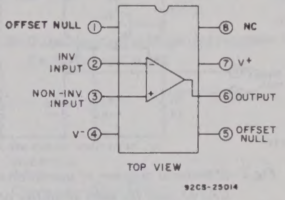


1d.—CA1458S,CA1458T,CA1558S, and CA1558T and internal phase compensation.

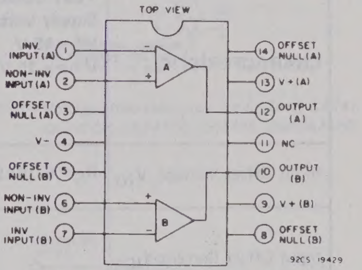
ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

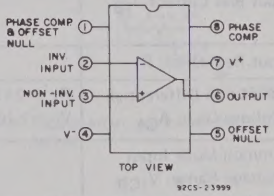
Type No.	PACKAGE TYPE AND SUFFIX LETTER										FIG. No.
	TO-5 STYLE			PLASTIC		Gold-CHIP PLASTIC		CHIP	Gold-CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L	8L	14L				
CA1458	T		S	E		G		H	GH		1d, 1h
CA1558	T		S	E		G					1d, 1h
CA741C	T		S	E		G		H	GH		1a, 1e
CA741	T		S	E		G				L	1a, 1e
CA747C		T			E		G	H	GH		1b, 1f
CA747		T			E		G				1b, 1f
CA748C	T		S	E		G		H	GH		1c, 1g
CA748	T		S	E		G					1c, 1g



1e.—CA741CE,CA741CG,CA741E, and CA741G with internal phase compensation.



1f.—CA747CE,CA747CG,CA747E, and CA747G with internal phase compensation.



1g.—CA748CE,CA748CG,CA748E, and CA748G with external phase compensation.

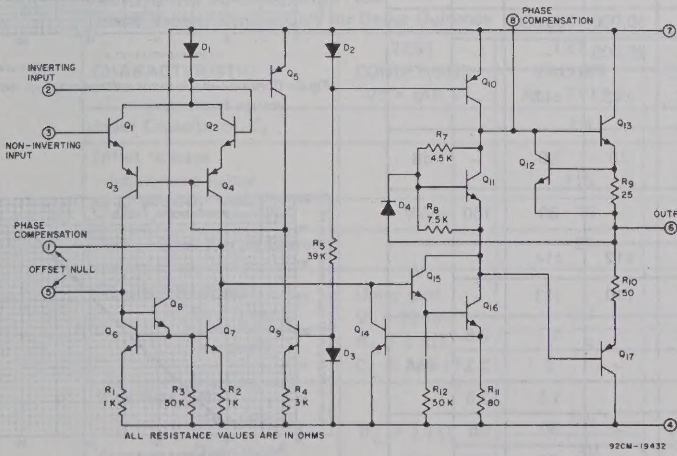
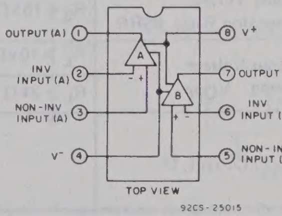


Fig.2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.



1h.—CA1458E,CA1458G,CA1558E, and CA1558G with internal phase compensation.

Fig. 1 — Functional Diagrams (Cont'd)

CA741, CA747, CA748, CA1458, CA1558 Types

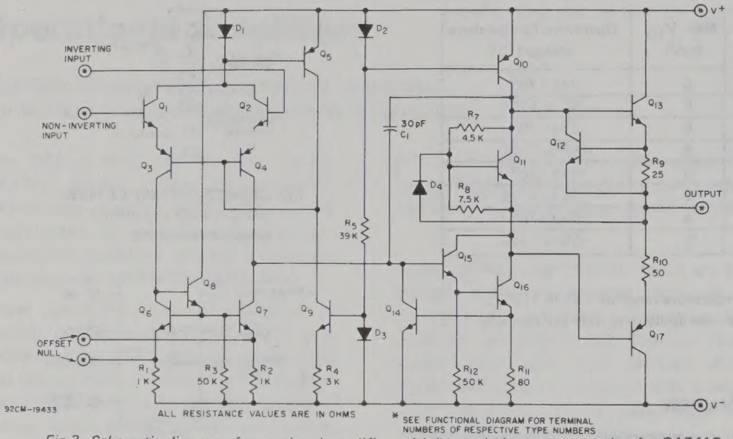


Fig.3–Schematic diagram of operational amplifiers with internal phase compensation for CA741C, CA741, and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

ELECTRICAL CHARACTERISTICS

For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, V^+ = 15 V, V^- = −15 V		LIMITS CA741 CA747* CA748 CA1558*			UNITS
		Ambient Temperature, T_A	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	R_S = ≤ 10 kΩ	25 °C	–	1	5	mV
		−55 to +125 °C	–	1	6	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		−55 °C	–	85	500	
		+125 °C	–	7	200	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		−55 °C	–	300	1500	
		+125 °C	–	30	500	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	R_L ≥ 2 kΩ V_O = ± 10 V	25 °C	50,000	200,000	–	
		−55 to +125 °C	25,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		−55 to +125 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	R_S ≤ 10 kΩ	−55 to +125 °C	70	90	–	dB
Supply Voltage Rejection Ratio, PSRR	R_S ≤ 10 kΩ	−55 to +125 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	R_L ≥ 10 kΩ	−55 to +125 °C	±12	±14	–	V
	R_L ≥ 2 kΩ	−55 to +125 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
		−55 °C	–	2	3.3	
		+125 °C	–	1.5	2.5	
Device Dissipation, P_D		25 °C	–	50	85	mW
		−55 °C	–	60	100	
		+125 °C	–	45	75	

* Values apply for each section of the dual amplifiers.

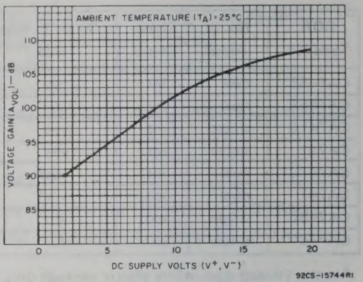


Fig.4–Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

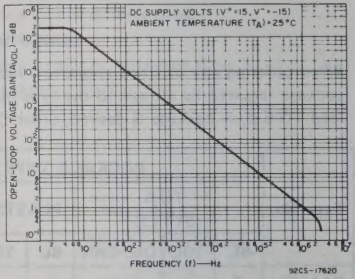


Fig.5–Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

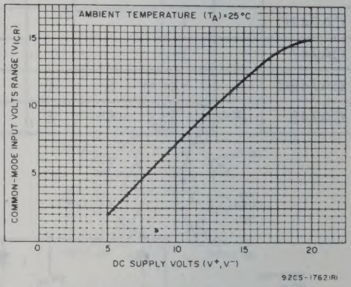


Fig.6–Common-mode input voltage range vs. supply voltage for all types.

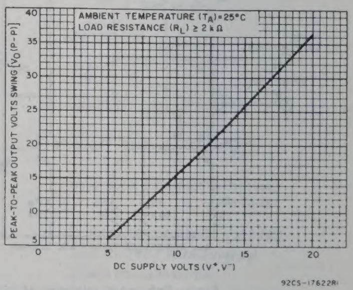


Fig.7–Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C.

CA741, CA747, CA748, CA1458, CA1558 Types

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V	Ambient Temperature, T_A	LIMITS CA741C CA747C* CA748C CA1458*			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	$R_S = \leqslant 10$ kΩ	25 °C	–	2	6	mV
		0 to 70 °C	–	–	7.5	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		0 to 70 °C	–	–	300	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		0 to 70 °C	–	–	800	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geqslant 2$ kΩ $V_O = \pm 10$ V	25 °C	20,000	200,000	–	
		0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leqslant 10$ kΩ	25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leqslant 10$ kΩ	25 °C	–	30	150	µV/V
Output Voltage Swing, V_{OPP}	$R_L \geqslant 10$ kΩ	25 °C	±12	±14	–	V
	$R_L \geqslant 2$ kΩ	25 °C	±10	±13	–	
		0 to 70 °C	±10	±13	–	
Supply Current, $I^\pm$		25 °C	–	1.7	2.8	mA
Device Dissipation, P_D		25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

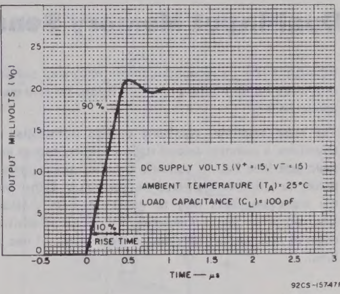


Fig.8—Output voltage vs. transient response time for CA741C and CA741.

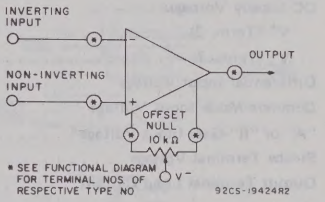


Fig.9—Voltage-offset null circuit for CA741C, CA741, CA747CE, CA747CG, CA747E, and CA747G.

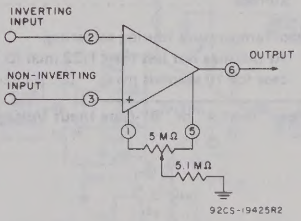


Fig.10—Voltage-offset null circuit for CA748C and CA748.

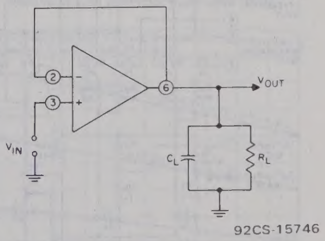


Fig.11—Transient response test circuit for all types.

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC		TEST CONDITIONS V± = ±15 V	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I			1.4	pF
Offset Voltage Adjustment Range			±15	mV
Output Resistance, R_O			75	Ω
Output Short-Circuit Current			25	mA
Transient Response:	Rise Time, t_r	Unity gain $V_I = 20$ mV $R_L = 2$ kΩ $C_L \leqslant 100$ pF	0.3	µs
	Overshoot		5	%
Slew Rate, SR:	Closed-loop	$R_L \geqslant 2$ kΩ	0.5	V/µs
	Open-loop▲		40	

▲ Open-loop slew rate applies only for types CA748C and CA748.

CA1541D

Dual-Input Memory Sense Amplifier

RCA-CA1541D , a monolithic silicon integrated circuit, is a dual-input memory sense amplifier intended for core memory applications.

The sense amplifier, consisting of two differential input amplifiers, a common second stage amplifier, and an output logic gate (See Fig. 1), converts low-level core-memory "1" pulses to saturated logic-level output pulses. Either one of the input amplifiers may be gated ON with a saturated logic signal so that an incoming "1" pulse of positive or negative polarity can be detected from either of two sense lines.

The CA1541D features an external switching threshold adjustment, plus its gate and strobe inputs are compatible with saturated logic levels. The sense amplifier is suitable for operation with core memories having cycle times equal to or greater than 0.4 μs and is unilaterally interchangeable with industry types 1541L and 1441.

The CA1541D is supplied in 14-lead dual-in-line ceramic package and is rated for operation over the full military temperature range of −55°C to +125°C.

Features

- **Complete dual input core memory sense amplifier**
- **Two available outputs: –Saturated logic output**
  –Linear output (positive output for either polarity input)
- **Nominal threshold voltage: 17 mV**
- **Adjustable threshold: 10 to 35 mV**
- **Low threshold uncertainty range: ±3 mV**
- **Fast overload recovery time: –Differential-Mode: 15 ns typ.**
  –Common-Mode: 30 ns typ.
- **Independent channel gate and strobe terminals compatible with saturated logic levels**
- **Suitable for core memories having cycle times ⩾ 0.4 μs**
- **Input offset voltage: 6 mV max.**

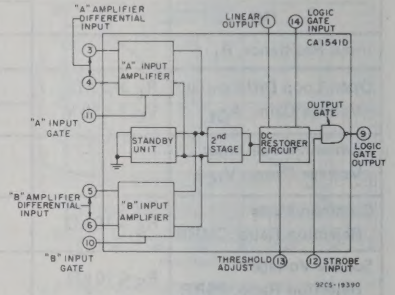


Fig. 1 – Functional block diagram of the CA1541D.

MAXIMUM RATINGS, Absolute Maximum Values, at T_A = 25°C

Except for Differential Input Voltage, all voltages are measured with respect to ground (Term. 8).

DC Supply Voltage:	
V^+ (Term. 2)	+10 V
V^- (Term. 7)	−10 V
Differential Input Voltage	±5 V
Common-Mode Input Voltage	±5 V
"A" or "B"-Gate Input Voltage*	V^- to V^+
Strobe Terminal Voltage	V^- to +6V
Output Terminal Load Current	±25 mA
Device Dissipation:	
Up to T_A = 75°C	750 mW
Above T_A = 75°C	Derate Linearly 8 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125 °C
Storage	−65 to +150 °C
Lead Temperature (during soldering): At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265°C

***Note:** The "A" or "B"-Gate Input Voltage is also referred to, as the Channel-Gate Input Voltage.

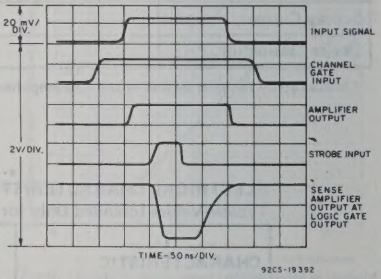


Fig. 3 – Typical operational wave forms.

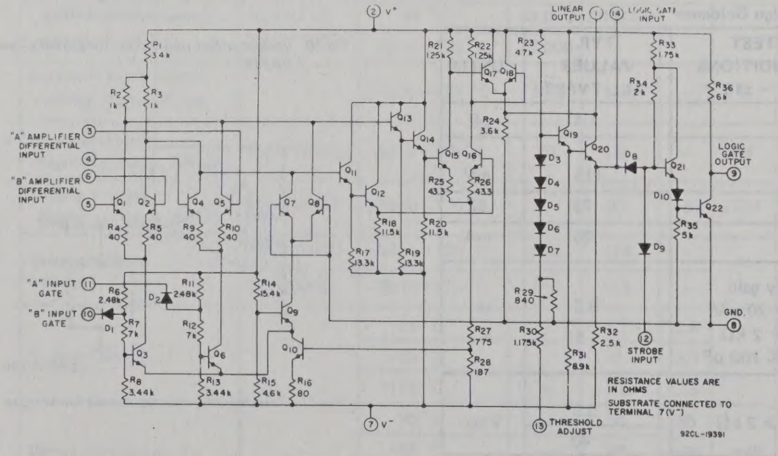


Fig. 2 – Schematic diagram of the CA1541D.

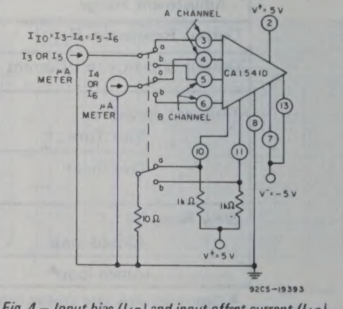


Fig. 4 – Input bias (I_{IB}) and input-offset current (I_{IO}) test circuit.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS $V^+ = 5V$, $V^- = -5V$ V_{TH} ADJ. = −5V ± 1%, (Term. 13) $C_{EXT} = 0.01\ \mu F$	$T_A = 25^oC$ (unless indicated otherwise)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Static (DC) Characteristics							
Power Dissipation	P_D			–	140	180	mW
Input Offset Current	I_{IO}			–	1	2	μA
Input Bias Current: $T_A = 25^oC$	I_{IB}		$V_5 = V_6 = V_3 = V_4 = 0$	–	5	25	μA
$T_A = -55^oC$				–	–	50	
Output Voltage: High	V_{OH}	$I_{OM} = 200\ \mu A$		3	–	–	V
Low – $T_A = 25^oC$	V_{OL}	$V_{14} = 5\ V$, $I_g = 10\ mA$		–	–	350	mV
$T_A = 125^oC$				–	–	400	
Strobe Load Current	I_S	$V_{12} = 0$		–	–	1.5	mA
Strobe Reverse Current: $T_A = 25^oC$	I_{SR}	$V_{12} = 5V$		–	–	2	μA
$T_A = 125^oC$				–	–	25	
Input Gate Load Current	I_G	$V_{10} = V_{11}$ 0		–	–	2.5	mA
Input Gate Reverse Current: $T_A = 25^oC$	I_{GR}	$V_{10} = V_{11} = 5V$		–	–	2	μA
$T_A = 125^oC$				–	–	25	
Switching Characteristics							
Input Threshold Voltage: $T_A = 25^oC$	V_{TH}			14	17	20	mV
$T_A = -55$ to 125^oC				12	17	22	
Input Offset Voltage	V_{IO}			–	1	6	mV
Input Gate Voltage: High	V_{GH}	$V_3 = V_5 = 25\ mV$,		–	1.6	—	V
Low	V_{GL}	$V_4 = V_6 = 0$		–	0.7	–	
Common-Mode Range: Input Gate High	V_{CM}			–	±1.5	–	V
Input Gate Low				–	±1.5	–	
Differential-Mode Range: Input Gate High	V_{DH}			–	±600	–	mV
Input Gate Low	V_{DL}			–	±1.5	–	V
Propagation Delay: Input to Amplifier Output	t_{IA}	$V_3 = 25\ mV$ (pulsed),		–	10	15	ns
Input to Output	t_{IO}	$V_{12} = 2V$		–	20	30	
Strobe to Output	t_{SO}	$V_3 = V_4 = V_5 = V_6 = 0$, $V_{12} = 2V$ (pulsed)		–	15	20	
Gate Input to Amplifier Output	t_{GA}	$V_{11} = 2V$ (pulsed)		–	10	15	
Gate Input to Amplifier Input	t_{GI}	$V_3 = 25\ mV$		–	30	35	
Common-Mode Recovery Time: Input Gate High	t_{CMR}	$V_3 = V_5 = 1.5\ V$		–	15	30	ns
Input Gate Low				–	15	30	
Differential-Mode Recovery Time: Input Gate High	t_{DR}	$V_3 = V_5 = 400\ mV$		–	30	–	ns
Input Gate Low				–	0	–	

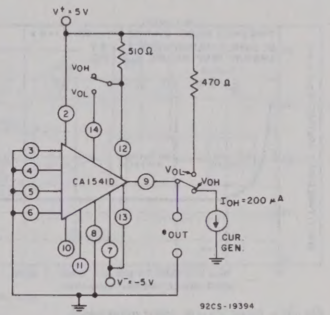


Fig. 5 – Test circuit for measurement of low (V_{OL}) and high (V_{OH}) output voltage levels.

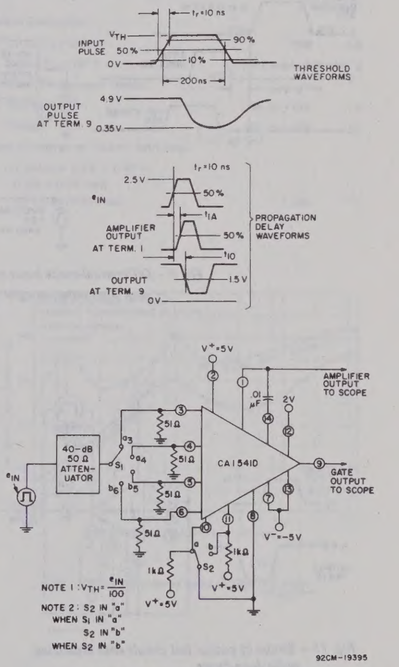


Fig. 6 – Threshold propagation delay, gate and input-offset test circuit with associated pulse wave forms.

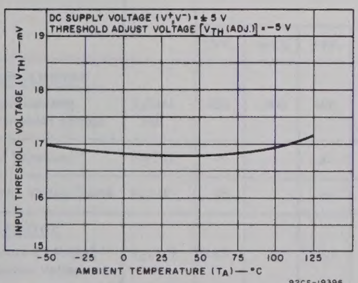


Fig. 7a – Input V_{TH} vs. T_A.

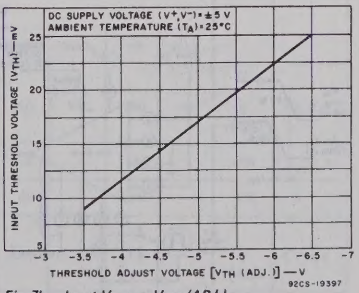


Fig. 7b – Input V_{TH} vs. V_{TH} (ADJ.).

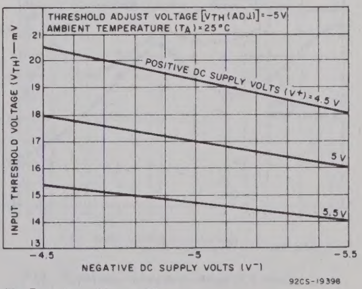


Fig. 7c – Input V_{TH} vs. V^-.

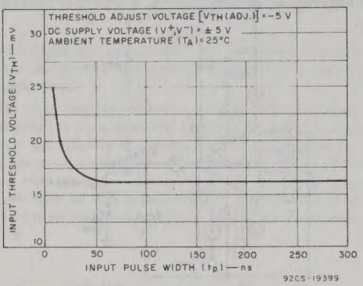


Fig. 7d – Input V_{TH} vs. input pulse width.

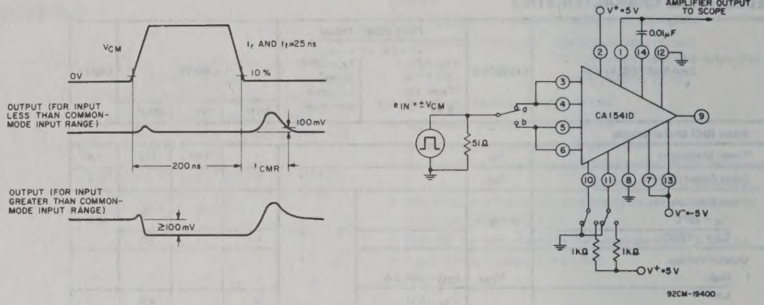

VCM
0V
tr AND tf = 25 ns
10 %
OUTPUT (FOR INPUT LESS THAN COMMON-MODE INPUT RANGE)
100mV
200 ns
tCMR
OUTPUT (FOR INPUT GREATER THAN COMMON-MODE INPUT RANGE)
≥100 mV
AMPLIFIER OUTPUT TO SCOPE
V+ = 5 V
0.01µF
eIN = ±VCM
a
b
51Ω
CA1541D
1KΩ
1KΩ
V− = −5 V
V+ = 5 V
92CM-19400

Fig. 8 – Common-mode input range test circuit with associated pulse wave forms.

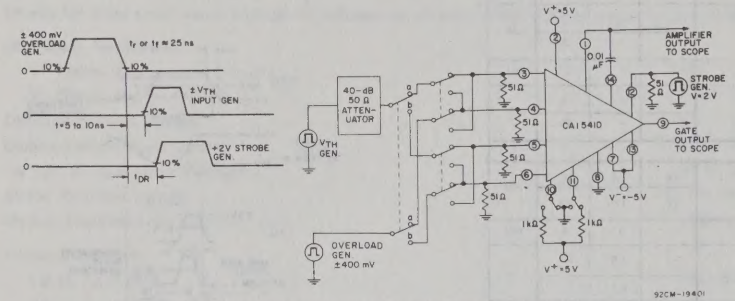


Fig. 9 – Differential-mode input range and recovery test circuit with associated pulse wave forms.

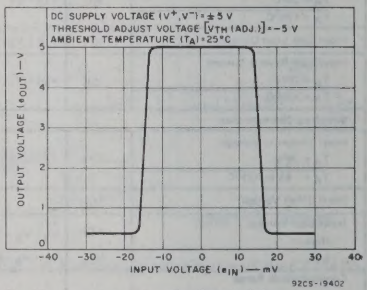


Fig. 10 – Input-output transfer characteristics.

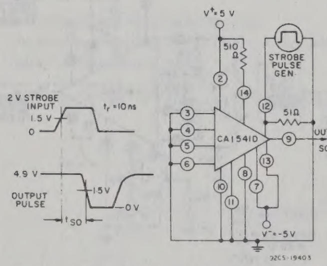
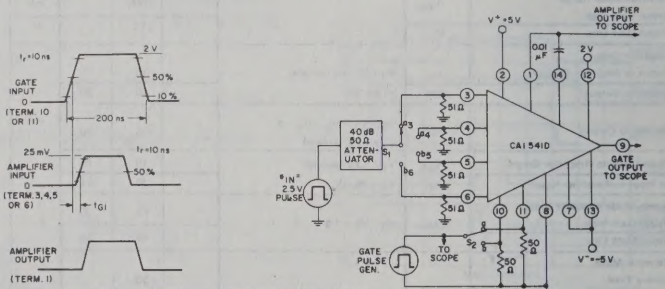


Fig. 11 – Strobe to output test circuit with associated pulse wave-forms.



NOTE: S2 IN "a" POSITION WHEN S1 IN EITHER "a" POSITION
S2 IN "b" POSITION WHEN S1 IN EITHER "b" POSITION

Fig. 12 – Gate input to amplifier input (t_{GI}) test circuit with associated pulse wave forms.

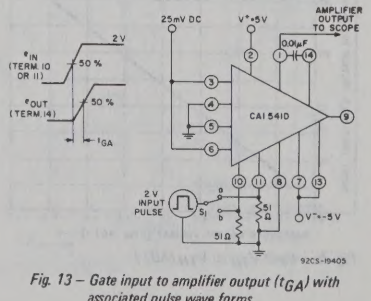


Fig. 13 – Gate input to amplifier output (t_{GA}) with associated pulse wave forms.

CA2111AE, CA2111AQ

FM IF Amplifier-Limiter and Quadrature Detector

For FM IF and TV Sound IF Applications

The CA2111A, on a single monolithic chip, provides a multistage wideband amplifier-limiter, a quadrature detector, and an emitter-follower output stage. This device is designed for use in FM receivers and in the sound IF sections of TV receivers. In addition, an output terminal is provided which allows the use of the amplifier-limiter as a straight 60-dB wideband amplifier.

The amplifier-limiter features the excellent limiting characteristics of 3 cascaded differential amplifiers.

The quadrature detector requires only one coil in the associated outboard circuit and therefore, tuning is a simple procedure.

A unique feature of the CA2111A is its exceptionally low AFC voltage drift over the full operating-temperature range.

This device can be supplied in either dual-in-line or quad-in-line 14-lead plastic packages (CA2111AE and CA2111AQ, respectively).

Features:

- **Direct replacement for ULN2111A and MC1357**
- **Good sensitivity: Input limiting voltage (knee) (400 μV typ. at 10.7 MHz; 250 μV typ. at 4.5 MHz and 5.5 MHz)**
- **Excellent AM rejection (45 dB typ. at 10.7 MHz)**
- **Provision for output from 3-stage IF amplifier section**
- **Low harmonic distortion**
- **Quadrature detection permits simplified single-coil tuning**
- **Extremely low AFC voltage drift over full operating-temperature range**
- **Minimum number of external parts required**

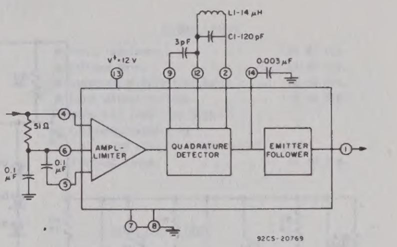


Fig. 1—Block diagram of CA2111A and associated outboard components.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC Supply Voltage [between terminals 13 (V^+) and 7 (V^-)]	16	V
Device Dissipation:		
Up to T_A = 60°C	600	mW
Above T_A = 60°C	derate linearly 6.7 mW/°C	
Ambient Temperature Range:		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for10s max.	+265	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
DC Voltage: At Terminal 1	V_1	V^+ = 12V	–	5.4	–	V
		= 8V	–	3.7	–	
At Terminals 4, 5, 6, 10	$V_{4,5,6,10}$	V^+ = 8V	–	1.35	–	
At Terminals 2, 12	$V_{2,12}$		–	3.5	–	
DC Current (into Terminal 13) At V^+ = 8V	I_{13}		–	14	–	mA
At V^+ = 12V			–	16	–	
Amplifier Input Resistance	R_4	f_o = 10.7 MHz	–	7	–	kΩ
Amplifier Input Capacitance	C_4		–	11	–	pF
Detector Input Resistance	R_{12}		–	70	–	kΩ
Detector Input Capacitance	C_{12}		–	2.7	–	pF
Amplifier Output Resistance	R_{10}		–	60	–	Ω
Detector Output Resistance	R_1		–	200	–	Ω
De-Emphasis Resistance	R_{14}		–	8.8	–	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
FM Modulation Frequency = 400 Hz, Source Resistance = 50Ω

CHARACTERISTIC	SYMBOL	TEST CONDITIONS								UNITS	TEST CIRCUIT OR CHARACTERISTIC CURVES FIG. NO.
		f_o = 10.7 MHz Δf = ± 75 KHz				f_o = 4.5 MHz Δf = ± 25 KHz		f_o = 5.5 MHz Δf = ± 50 KHz			
		V^+ = 12V		V^+ = 8V		V^+ = 12V		V^+ = 12V			
		LIMITS									
		TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.		
AMPL-LIMITER											
Input Limiting Threshold Voltage	V_i(lim) (4)	400	600	400	600	250	400	250	400	V (RMS)	7, 6, 8, 9
AM Rejection[‡][*]	AMR(1)	45	–	37	–	36	–	40	–	dB	2, 7, 5, 6
Ampl. Voltage Gain▲	A_V(10)	55	–	55	–	60	–	60	–	dB	7
DETECTOR											
Recovered Audio[‡] Output Voltage	V_o(AF) (1)	0.48	–	0.3	–	0.72	–	1.2	–	V (RMS)	6, 7, 8, 9
Total Harmonic[‡] Distortion	THD(1)	1	–	1	–	1.5	–	3	–	%	7

[‡] V_i = 10 mV (RMS)

▲ $V_i \leqslant 50$ μV (rms)

[*] 100% FM, 30% AM

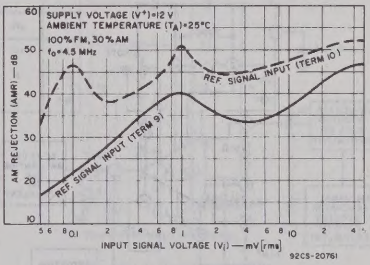


Fig. 2—AM rejection vs input voltage (4.5 MHz).

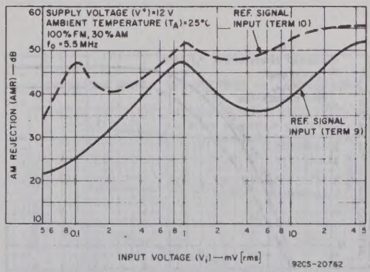


Fig. 3—AM rejection vs input voltage (5.5 MHz).

CA2111AE, CA2111AQ

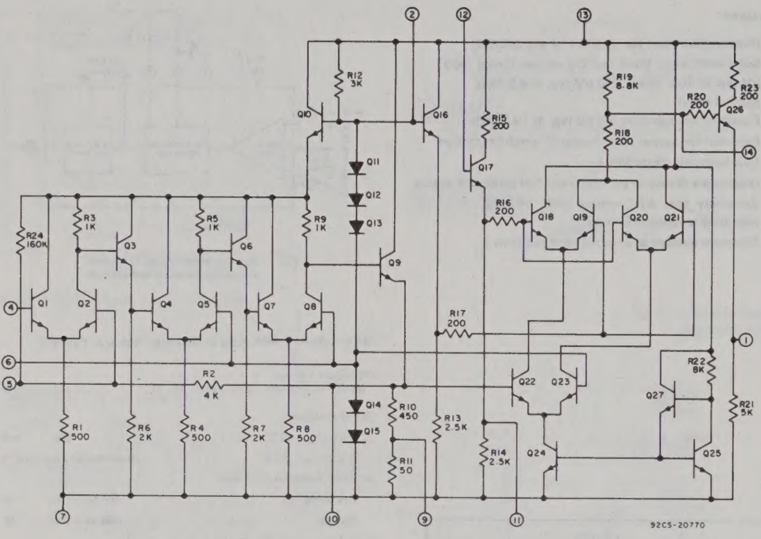


Fig. 4 –Circuit schematic–CA2111A

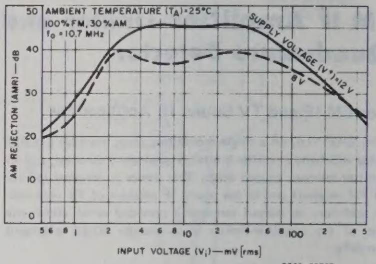


Fig. 5 –AM rejection vs input voltage (10.7 MHz).

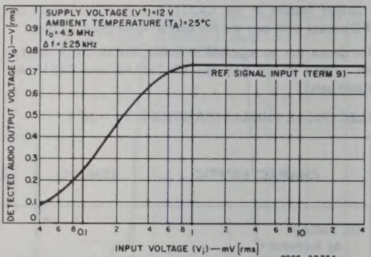
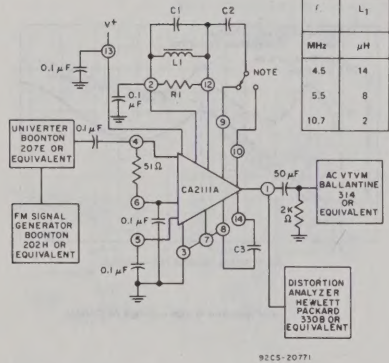


Fig. 6 –Detected audio output vs input voltage (4.5 MHz).

COMPONENT VALUES							DETECTOR TRANSFER CHARACTERISTICS	
f	L_1	C_1	R_1	Q	C_2	C_3	UPPER PEAK	LOWER PEAK
MHz	μH	pF	KΩ	–	pF	μF	MHz	MHz
4.5	14	120	20	30	3	0.003	4.58	4.42
5.5	8	100	20	30	3	0.003	5.63	5.37
10.7	2	120	3.9	20	4.7	0.01	10.9	10.5



V+
13
0.1 μF
C1
C2
L1
2
R1
12
NOTE
0.1 μF
9
UNIVERTER BOONTON 207E OR EQUIVALENT
0.1 μF
4
10
51 Ω
CA2111A
50 μF
1
AC VTVM BALLANTINE 314 OR EQUIVALENT
2K Ω
FM SIGNAL GENERATOR BOONTON 202H OR EQUIVALENT
6
14
0.1 μF
8
5
7
3
C3
0.1 μF
DISTORTION ANALYZER HEWLETT PACKARD 330B OR EQUIVALENT
92CS-20771

NOTE:

Input to the quadrature coil can be from either terminal 9 or terminal 10. Terminal 9 is normally used because it lessens the possibility of overloads during tuning. The use of terminal 10 increases the limiting sensitivity significantly and has been used successfully in these tests.

Fig. 7 –Test circuit.

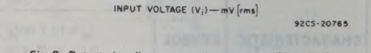


Fig. 8–Detected audio output vs input voltage (5.5 MHz).

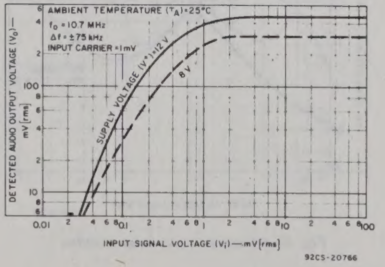


Fig. 9–Detected audio output voltage vs input voltage (10.7 MHz)

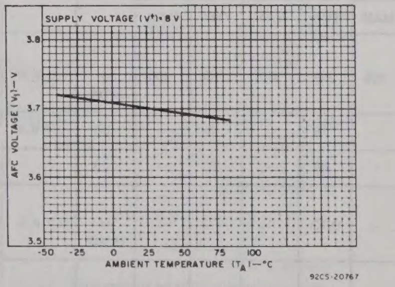


Fig. 10–AFC voltage vs ambient temp.

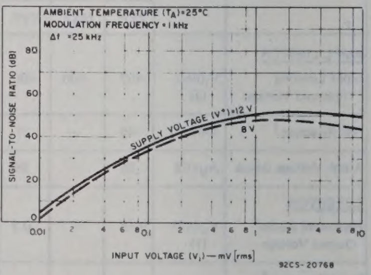


Fig. 11–Signal-to-noise ratio vs input voltage.

DC Amplifier

- Designed for use in Communication, Telemetry, Instrumentation, and Data-Processing Equipment
- Balanced differential-amplifier configuration with controlled constant-current source to provide outstanding versatility
- Built-in temperature stability for operation from $-55^{\circ}C$ to $+125^{\circ}C$
- Companion Application Note, ICAN 5030 "Applications of RCA CA3000 Integrated Circuit DC Amplifier" covers characteristics of different operating modes, frequency considerations, 10 MHz narrow band tuned amplifier design, crystal oscillator design, and many other application aids
- 10-Lead hermetic TO-5 style package

HIGHLIGHTS

Input Impedance	195 kΩ typ.
Voltage Gain	30 dB typ.
Common-Mode Rejection Ratio	98 dB typ.
Input Offset Voltage	1.4 mV typ.
Push-Pull Input and Output	
Frequency Capability DC to 30 MHz (with external C and R)	
Wide AGC Range	90 dB typ.

APPLICATIONS

- Schmitt Trigger
- RC-Coupled Feedback Amplifier
- Mixer
- Comparator
- Modulator
- Crystal Oscillator
- Sense Amplifier

ABSOLUTE-MAXIMUM VOLTAGE LIMITS

at $T_{FA} = 25^{\circ}C$

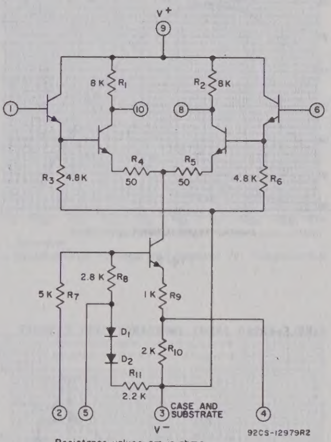
OPERATING-TEMPERATURE RANGE	$-55^{\circ}C$ to $+125^{\circ}C$
STORAGE-TEMPERATURE RANGE	$-65^{\circ}C$ to $+150^{\circ}C$
LEAD-TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	$+265^{\circ}C$

MAXIMUM POWER SUPPLY VOLTAGE -- 16 or ±8 V

MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	±2 V
MAXIMUM DEVICE DISSIPATION:	
From $-55^{\circ}C$ to $85^{\circ}C$	450 mW
Above $85^{\circ}C$	Derate 5 mW/°C

ELECTRICAL CHARACTERISTICS, at $T_{FA} = 25^{\circ}C$, $V_{CC} = +6V$, $V_{EE} = -6V$, unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified		TEST CIRCUITS	LIMITS TYPE CA3000				TYPICAL CHARAC-TERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}				-	1.4	5	mV	2
Input Offset Current	I_{IO}				-	1.2	10	μA	2
Input Bias Current	I_{IB}				-	23	36	μA	3
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS							
		4	5						
		NC	NC		-	2.6	-	V	4
		NC	VEE		-	4.2	-	V	4
		VEE	NC		-	-1.5	-	V	4
		VEE	VEE		-	0.6	-	V	4
Device Dissipation	P_D	NC	NC		-	30	-	mW	NONE
DYNAMIC CHARACTERISTICS									
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kHz		6	28	32	-	dB	5
		Double-Ended Output f = 1 kHz		6	-	38	-	dB	5
Bandwidth at -3 dB Point	BW	$V_I = 10$ mV, $R_s = 1$ kΩ			-	650	-	kHz	7
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kHz		6	-	6.4	-	V(P-P)	NONE
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		9	70	98	-	dB	8
Single-Ended Input Impedance	Z_{IN}	f = 1 kHz		11	70K	195K	-	Ω	10
Single-Ended Output Impedance	Z_{OUT}	f = 1 kHz		13	5.5K	8K	10.5K	Ω	12
Total Harmonic Distortion	THD	R_S=1kΩ f = 1 kHz V_O=42V_{p-p}			-	0.2	5	%	14
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kHz		15	80	90	-	dB	NONE



Resistance values are in ohms

Fig.1 SCHEMATIC DIAGRAM

STATIC CHARACTERISTICS FOR TYPE CA3000

INPUT OFFSET VOLTAGE AND CURRENT vs TEMPERATURE

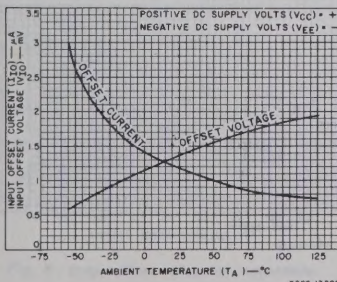


Fig.2

INPUT BIAS CURRENT vs TEMPERATURE

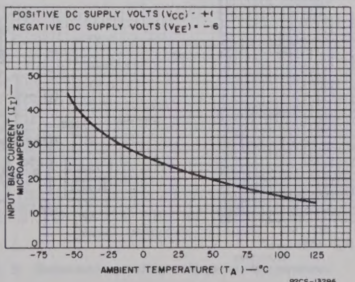


Fig.3

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

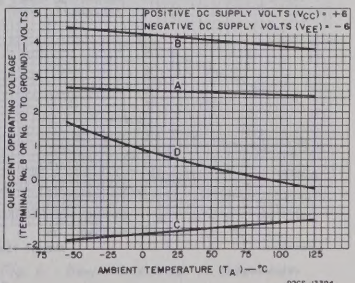


Fig.4

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT FOR TYPE CA3000

DIFFERENTIAL VOLTAGE GAIN vs TEMPERATURE

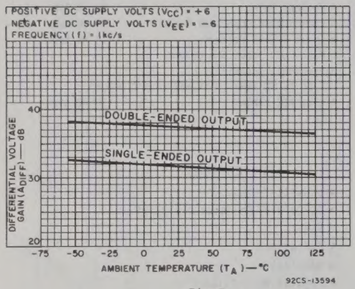


Fig.5

DIFFERENTIAL VOLTAGE GAIN AND MAXIMUM OUTPUT VOLTAGE SWING TEST CIRCUIT

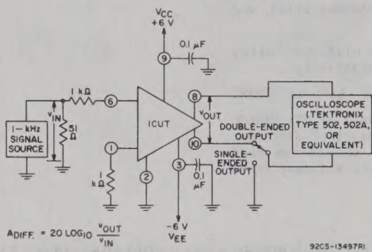


Fig.6

BANDWIDTH AT −3 dB POINT vs TEMPERATURE

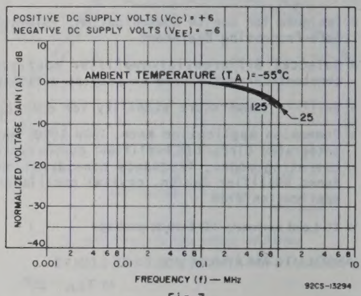


Fig.7

COMMON-MODE REJECTION RATIO vs TEMPERATURE

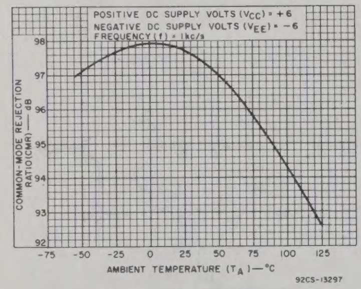


Fig.8

COMMON-MODE REJECTION RATIO TEST CIRCUIT

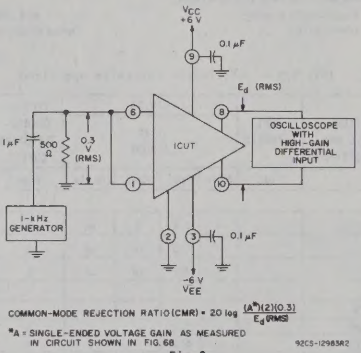

V_{CC} +6 V
0.1 μF
9
E_d (RMS)
6
8
1 μF
500 Ω
0.3 V (RMS)
ICUT
OSCILLOSCOPE WITH HIGH-GAIN DIFFERENTIAL INPUT
1
10
1-kHz GENERATOR
2
3
0.1 μF
−6 V V_{EE}
COMMON-MODE REJECTION RATIO (CMR) = $20 \log \frac{(A^*)(2)(0.3)}{E_d\,(RMS)}$
*A = SINGLE-ENDED VOLTAGE GAIN AS MEASURED IN CIRCUIT SHOWN IN FIG. 6B
92CS-12983R2

Fig.9

SINGLE-ENDED INPUT IMPEDANCE vs TEMPERATURE

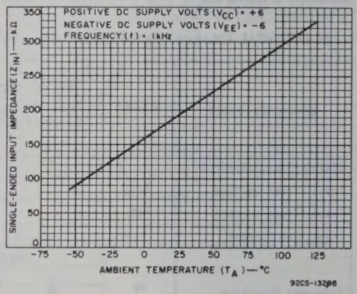


Fig.10

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

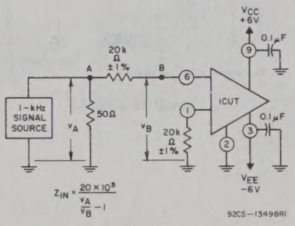


Fig.11

SINGLE-ENDED OUTPUT IMPEDANCE vs TEMPERATURE

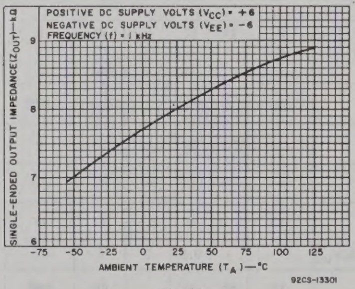


Fig.12

SINGLE-ENDED OUTPUT IMPEDANCE TEST CIRCUIT

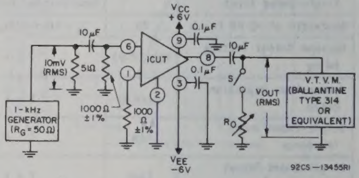


Fig.13

TOTAL HARMONIC DISTORTION vs TEMPERATURE

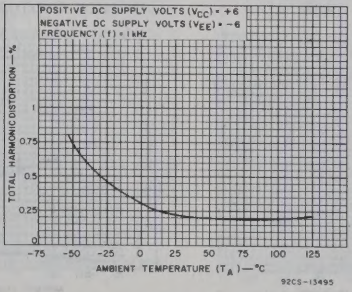


Fig.14

AGC RANGE TEST CIRCUIT

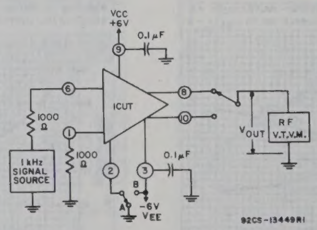


Fig.15

CA3001

Video and Wideband Amplifier

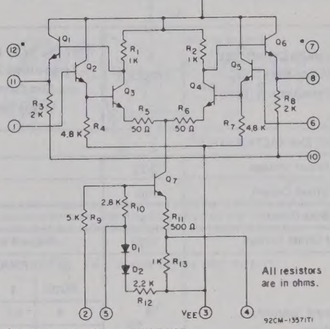
- **Designed for use in Video Systems and Communication Equipment**
- **Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility**
- **Built-in temperature stability for operation from -55°C to +125°C**
- **Emitter follower input & output**
- **Companion Application Note ICAN5038 "Application of the RCA-CA3001 Integrated-Circuit Video Amplifier", covers different operating modes, gain control, distortion, swing capability, 3 stage amplifier design, and a Schmitt trigger study.**
- 12-Lead Hermetic TO-5 Style Package

HIGHLIGHTS

Push-Pull Input & Output	
AGC Range	60 dB typ.
Bandwidth.	29 MHz
Input Resistance	150 kΩ typ.
Output Resistance	45 Ω typ.
Voltage Gain	19 dB typ.
Input Offset Voltage	1.5 mV typ.

APPLICATIONS

- Schmitt Trigger
- Mixer
- Modulator
- DC, IF, & Video Amplifier



* Internal Connection – DO NOT USE

Fig.1 - Schematic Diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS at T_A = 25°C

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals.
All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10	0 -6 +6
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10 & No.11	0 -6 +6
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

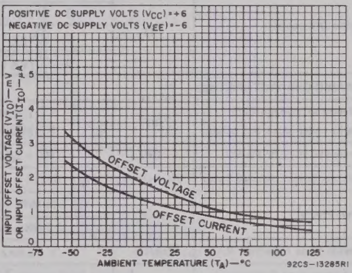


Fig.2 - Input offset voltage and current vs. temperature.

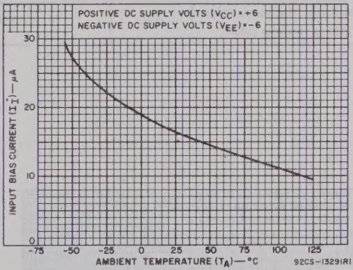


Fig.3 - Input bias current vs. temperature.

OPERATING TEMPERATURE RANGE	-55°C to +125°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	± 4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	± 2.5 V
MAXIMUM DEVICE DISSIPATION:	
-55 to 85°C	450 mW
Above 85°C	Derate linearly 5 mW/°C

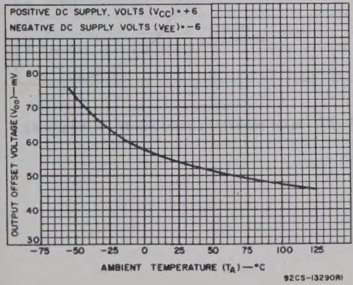


Fig. 4 - Output offset voltage vs. temperature.

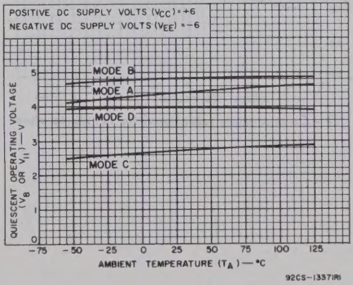


Fig. 5 - Quiescent operating voltage vs. temperature.

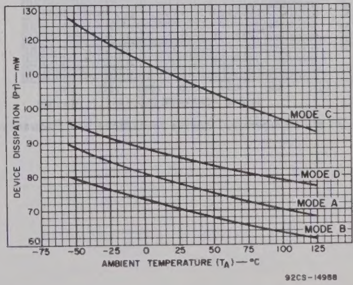


Fig. 6 - Device dissipation vs. temperature.

ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{CC} = +6 V, V_{EE} = −6 V

CHARACTERISTICS (See Page 2 for Definitions of Terms)	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Not Connected Unless Specified			TEST CIRCUITS	LIMITS				TYPICAL CHARAC-TERISTICS CURVES
						TYPE CA3001				
					Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:										
Input Offset Voltage	V_{IO}				12	-	1.5	-	mV	2
Input Offset Current	I_{IO}				13	-	1	10	μA	2
Input Bias Current	I_I				13	-	16	36	μA	3
Output Offset Voltage	V_{OO}	R_S = 1 kΩ				-	54	300	mV	4
Quiescent Operating Voltage	V_8 OR V_{11}	TERMINALS								
		MODE	4	5						
		A	NC	NC		3.8	4.4	5	V	5
		B	NC	V_{EE}		-	4.8	-	V	5
		C	V_{EE}	NC		-	2.7	-	V	5
		D	V_{EE}	V_{EE}		-	4	-	V	5
Device Dissipation	P_D	A	NC	NC		60	78	120	mW	6
		B	NC	V_{EE}		-	71	-	mW	6
		C	V_{EE}	NC		-	110	-	mW	6
		D	V_{EE}	V_{EE}		-	86	-	mW	6
DYNAMIC CHARACTERISTICS:										
Differential Voltage Gain (Single-ended input and output)	A_{DIFF}	f 1.75 MHz f 20 MHz				16 10	19 14	- -	dB dB	7, 8
Bandwidth at -3 dB Point	BW	R_S = 50Ω				16	29	-	MHz	NONE
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	R_S = 50Ω f = 1.75 MHz				-	5	-	V_{P-P}	NONE
Noise Figure	NF	f 1.75 MHz, R_S 1 KΩ			11	-	5	8	dB	
		f 11.7 MHz, R_S 1 KΩ			11	-	7.7	-	dB	9
Common-Mode Rejection Ratio	CMRR	f 1 KHz				70	88	-	dB	10
Input Impedance Components:										
Parallel Input Resistance	R_{IN}	f 1.75 MHz				50	140	-	KΩ	11
Parallel Input Capacitance	C_{IN}	f 1.75 MHz				-	3.4	7	pF	11
Output Resistance	R_{OUT}	f 1.75 MHz				-	45	70	Ω	NONE
AGC Range (Maximum voltage gain to complete cutoff)	AGC	f 1.75 MHz				55	60	-	dB	NONE

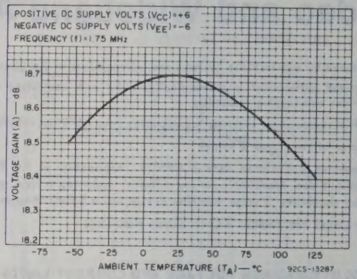


Fig. 7 - Differential voltage gain vs. temperature.

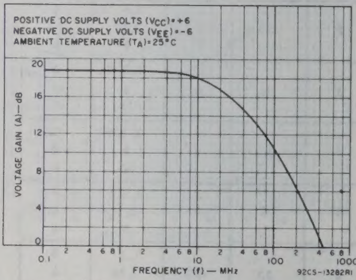


Fig. 8 - Differential voltage gain vs. frequency.

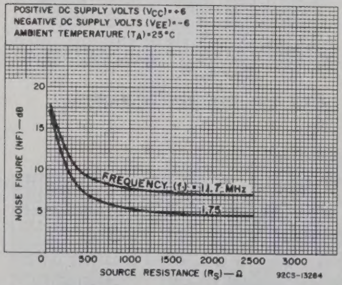


Fig. 9 - Noise figure vs. source resistance and frequency.

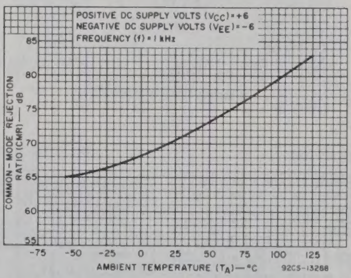


Fig. 10 - Common-mode rejection ratio vs. temperature.

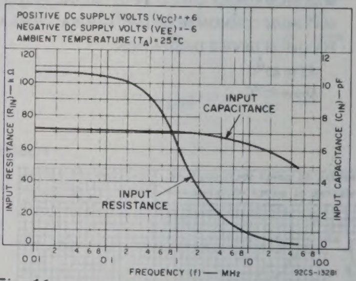
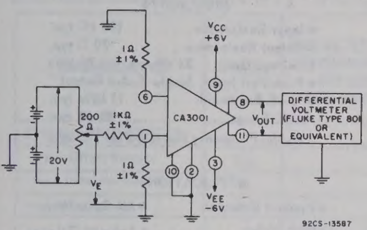
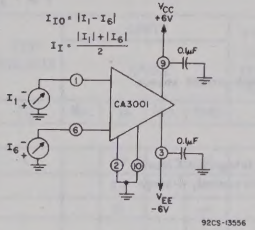


Fig. 11 - Input impedance components vs. frequency.



1. Adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ V 2. Measure V_E and record input offset voltage (V_{IO}) in mV as
$$V_{IO} = \frac{V_E}{1000}$$

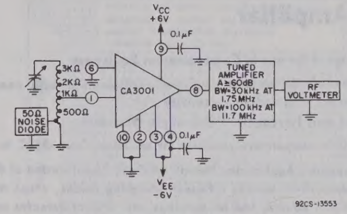
Fig. 12 - *Input offset voltage test circuit.*



$I_{IO} = |I_1 - I_6|$

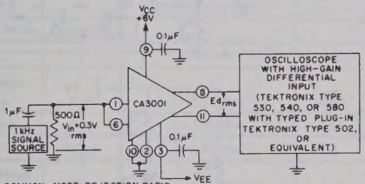
$I_I = \frac{|I_1| + |I_6|}{2}$

Fig. 13 - *Input offset current and input bias current test circuit.*



* Separate tuned input circuits are used for 1.75 MHz and 11.7 MHz. Source-resistance matching taps adjusted with circuit tuned to resonance and with 50-ohm resistor connected to simulate noise diode.

Fig. 14 . *Noise figure test circuit.*

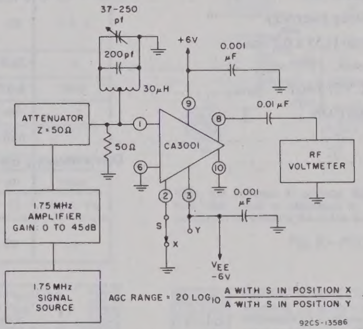

VCC
+6V
0.1µF
⑨
1µF
500Ω
Vin=0.3V rms
1kHz SIGNAL SOURCE
①
⑥
CA3001
⑧
⑪
Edrms
OSCILLOSCOPE WITH HIGH-GAIN DIFFERENTIAL INPUT (TEKTRONIX TYPE 530, 540, OR 580 WITH TYPED PLUG-IN TEKTRONIX TYPE 502, OR EQUIVALENT)
⑩ ② ③
0.1µF
VEE
-6V
92CS-13554

COMMON-MODE REJECTION RATIO

$$CMR = 20\ LOG_{10} \frac{(A^*)(2)(0.3)}{E_{d(rms)}}$$

*A = SINGLE-ENDED VOLTAGE GAIN

Fig. 15 - *Common-mode rejection ratio test circuit.*



$$AGC\ RANGE = 20\ LOG_{10} \frac{A \text{ WITH S IN POSITION X}}{A \text{ WITH S IN POSITION Y}}$$

Fig. 16 - *AGC range test circuit.*

CA3002

IF Amplifier

- **Designed for use in Communication Equipment**
- **Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility**
- **10-Lead hermetic TO-5 style package**
- **Built-in temperature stability for operation from -55°C to +125°C**
- **Companion Application Note ICAN-5036 "Application of the RCA-3002 Integrated-Circuit IF Amplifier" covers different operating modes, cross modulation, gain control, 4-stage amplifier design, and an envelope and product detector analysis.**

HIGHLIGHTS

- **Input Resistance . . . . . . 100 kΩ typ.**
- **Output Resistance . . . . . 70 Ω typ.**
- **Voltage Gain . . 24 dB typ. @ 1.75 MHz**
- **Push-Pull Input, Single-Ended Output**
- **-3 dB Bandwidth . . . . . . 11 MHz typ.**
- **AGC Range . . . . 80 dB typ.**
- **Useful Frequency Range DC to. . 15 MHz**

APPLICATIONS

- **Product Detector**
- **IF & Video Amplifier**
- **AM Detector**
- **Schmitt Trigger**

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, at T_A = 25°C

COMMON-MODE INPUT SIGNAL VOLTAGE	±2 V
MAXIMUM POWER SUPPLY VOLTAGE	16 V or ±8 V
OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM INPUT-SIGNAL VOLTAGE	± 4 V
MAXIMUM DEVICE DISSIPATION:	
-55 to 85°C	450 mW
Above 85°C	Derate linearly 5 mW/°C

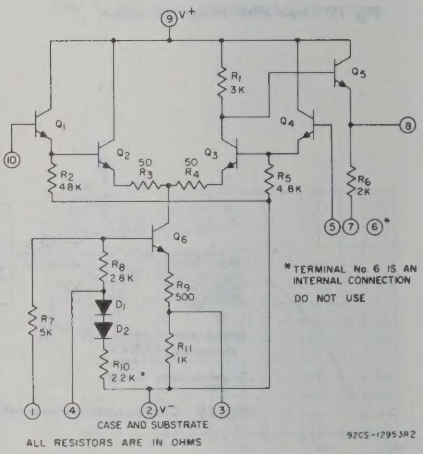


Fig. 1 — Schematic diagram.

STATIC CHARACTERISTICS AND TEST CIRCUITS

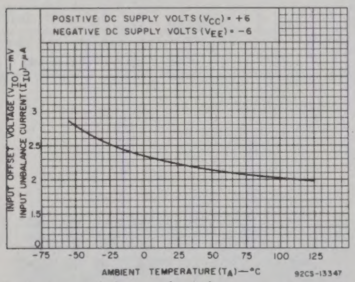


Fig.2 - Input unbalance voltage & current vs temperature.

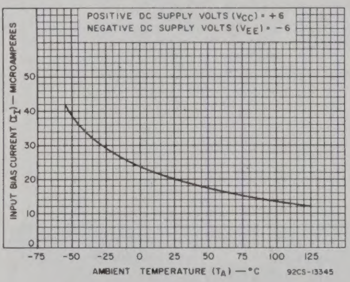


Fig.3 - Input bias current vs temperature.

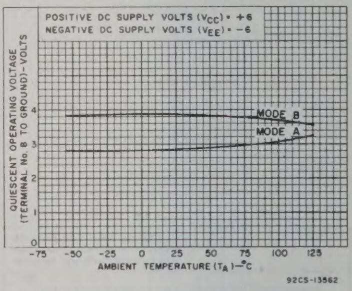


Fig.4 - Quiescent operating voltage vs temperature.

STATIC CHARACTERISTICS AND TEST CIRCUITS

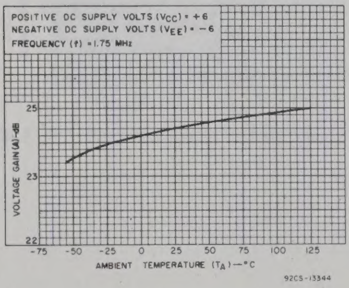


Fig. 5a - Differential voltage gain vs temperature.

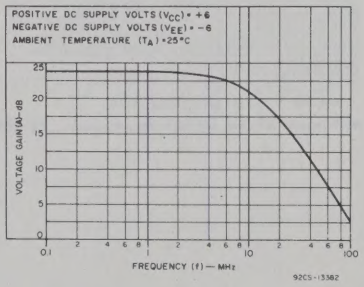


Fig. 5b - Differential voltage gain vs frequency.

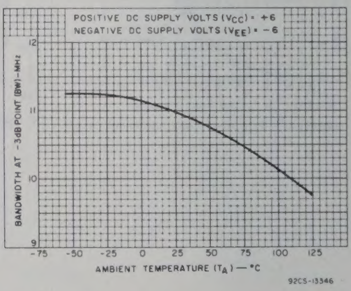


Fig. 6 - Bandwidth at -3 dB point vs temperature.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{CC} = +6 V, V_{EE} = -6 V

<table>
<tr><th rowspan="3">CHARACTERISTICS</th><th rowspan="3">SYMBOLS</th><th rowspan="3" colspan="3">SPECIAL TEST CONDITIONS TERMINALS No.3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED</th><th rowspan="2">TEST CIRCUITS</th><th colspan="4">LIMITS</th><th rowspan="2">TYPICAL CHARAC-TERISTICS CURVES</th></tr>
<tr><th colspan="4">CA3002</th></tr>
<tr><th>Fig.</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Units</th><th>Fig.</th></tr>
<tr><td>STATIC CHARACTERISTICS:</td><td></td><td colspan="3"></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Input Offset Voltage</td><td>V_{IO}</td><td colspan="3"></td><td>4</td><td>-</td><td>2.2</td><td>-</td><td>mV</td><td>2</td></tr>
<tr><td>Input Unbalance Current</td><td>I_{IU}</td><td colspan="3"></td><td></td><td>-</td><td>2.2</td><td>10</td><td>µA</td><td>2</td></tr>
<tr><td>Input Bias Current</td><td>I_I</td><td colspan="3"></td><td></td><td>-</td><td>20</td><td>36</td><td>µA</td><td>3</td></tr>
<tr><td rowspan="4">Quiescent Operating Voltage</td><td rowspan="4"></td><td>MODE</td><td colspan="2">TERMINAL</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td>2</td><td>4</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>A</td><td>V_{EE}</td><td>NC</td><td></td><td>-</td><td>2.8</td><td>-</td><td>V</td><td>4</td></tr>
<tr><td>B</td><td>V_{EE}</td><td>V_{EE}</td><td></td><td>-</td><td>3.9</td><td>-</td><td>V</td><td>4</td></tr>
<tr><td>Device Dissipation</td><td>P_T</td><td colspan="3"></td><td></td><td>-</td><td>55</td><td>-</td><td>mW</td><td>None</td></tr>
<tr><td>DYNAMIC CHARACTERISTICS:</td><td></td><td colspan="3"></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Differential Voltage Gain (Single-Ended Input and Output)</td><td>A_{DIFF}</td><td colspan="3">V_{IN} = 10 mV
f = 1.75 MHz
R_S = 50Ω</td><td></td><td>19</td><td>24</td><td>-</td><td>dB</td><td>5 & .5</td></tr>
<tr><td>Bandwidth at -3 dB Point</td><td>BW</td><td colspan="3">R_S = 50Ω, V_{IN} = 10 mV</td><td></td><td>-</td><td>11</td><td>-</td><td>MHz</td><td>6</td></tr>
<tr><td>Maximum Output Voltage Swing</td><td>$V_{OUT}(P-P)$</td><td colspan="3">-</td><td></td><td>-</td><td>5.5</td><td>-</td><td>V_{P-P}</td><td>None</td></tr>
<tr><td>Noise Figure</td><td>NF</td><td colspan="3">f = 1.75 MHz R_S = 1 kΩ</td><td>8</td><td>-</td><td>4</td><td>8</td><td>dB</td><td>7</td></tr>
<tr><td>Input Impedance Components:
Parallel Input Resistance</td><td>R_{IN}</td><td colspan="3">f = 1.75 MHz</td><td>None</td><td>-</td><td>100k</td><td>-</td><td>Ω</td><td>None</td></tr>
<tr><td>Parallel Input Capacitance</td><td>.C_{IN}</td><td colspan="3">f = 1.75 MHz</td><td>None</td><td>-</td><td>4</td><td>-</td><td>pF</td><td>None</td></tr>
<tr><td>Output Resistance</td><td>R_{OUT}</td><td colspan="3">f = 1.75 MHz</td><td>14</td><td>-</td><td>70</td><td>-</td><td>Ω</td><td>9a & 9b</td></tr>
<tr><td>AGC Range (Maximum Voltage Gain to Complete Cutoff</td><td>AGC</td><td colspan="3">f = 1.75 MHz</td><td>13</td><td>60</td><td>80</td><td>-</td><td>dB</td><td>12</td></tr>
</table>

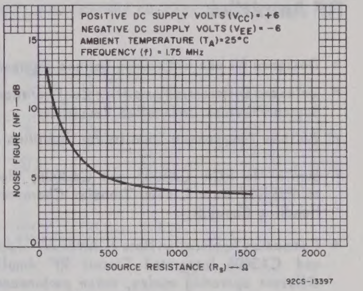
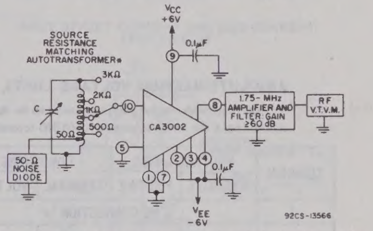


Fig. 7 - Noise figure vs source resistance.


VCC
+6V
SOURCE RESISTANCE MATCHING AUTOTRANSFORMER*
0.1µF
3KΩ
2KΩ
1KΩ
500Ω
50Ω
C
50-Ω NOISE DIODE
CA3002
1.75-MHz AMPLIFIER AND FILTER: GAIN ≥60 dB
RF V.T.V.M.
0.1µF
VEE
-6V
92CS-13566

* Taps are adjusted to provide indicated equivalent values of R_S with tank tuned to resonance at 1.75 MHz, and a 50-Ω resistor connected to simulate the noise diode.

Fig. 8 - Noise figure.

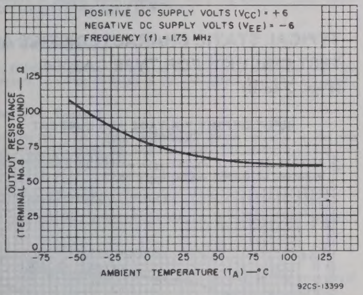


Fig. 9a - Output resistance vs temperature.

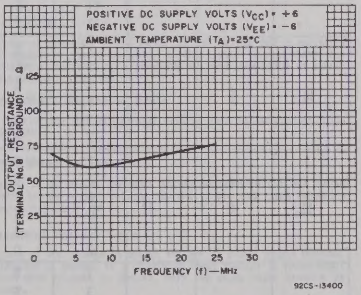


Fig. 9b - Output resistance vs frequency.

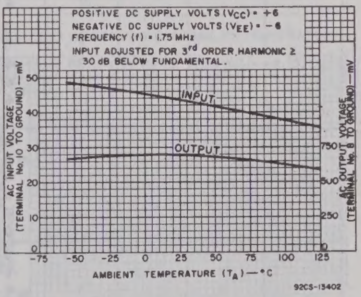
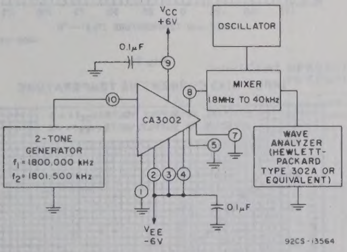


Fig. 10 - Input level for – 30 dB intermodulation vs. temperature



1) Increase both input-signal tones until the $2f_2$-f1 and $2f_1$-f2 output-signal voltages are 30 dB below the f_1 and f_2 output-signal voltages.
2) Measure rms values of the input and output signal voltages.
3) The measured input signal voltage is that value when the 3rd-harmonic intermodulation products are 30 dB below the fundamental outputs.

Fig. 11 - Intermodulation Test Circuit.

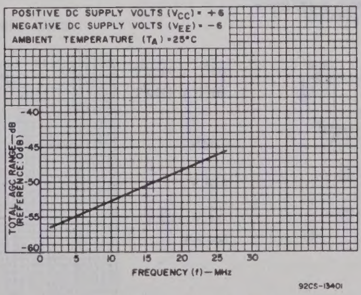
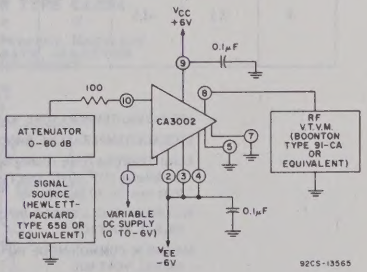


Fig. 12 - AGC range vs frequency.


VCC
+6V
0.1µF
100
CA3002
ATTENUATOR 0-80 dB
SIGNAL SOURCE (HEWLETT-PACKARD TYPE 658 OR EQUIVALENT)
VARIABLE DC SUPPLY (0 TO -6V)
RF V.T.V.M. (BOONTON TYPE 91-CA OR EQUIVALENT)
0.1µF
VEE
-6V
92CS-13565

1) Set attenuator at 80 dB attenuation.
2) Set variable dc supply voltage at 0 V.
3) Increase signal input voltage until RF V.T.V.M. indicates 5 mV output.
4) Set variable dc supply voltage at -6 V.
5) Adjust attenuator until RF V.T.V.M. again indicates 5 mV output.
6) Change in attenuator setting in dB is total AGC Range.

Fig. 13 - AGC range.

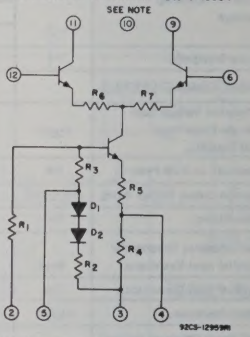
CA3004

RF Amplifier

- Designed for use in Communications Equipment
- Balanced Differential-Amplifier Configuration with Controlled Constant-Current Source Provides Unexcelled Versatility
- Built-in Temperature Stability for Operation from -55° C to +125° C
- Similar to RCA CA3005 and CA3006, plus Emitter-Degeneration Resistors to Provide More Linear Transfer Characteristic and Increased Input-Signal Handling Capability
- Companion Application Note ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC, limiter, detector, and amplifier design considerations.
- 12-Lead Hermetic TO-5 Style Package

- Push-Pull Input and Output
- Wide and Narrow-Band Amplifier
- AGC
- Detector
- Operation from DC to 100 Mc/s
- Mixer
- Limiter
- Modulator
- RF, IF, and Video Frequency Capability

SCHEMATIC DIAGRAM FOR CA3004



NOTE: Connect Terminal No. 10 to most positive dc supply voltage used for circuit.

Fig.1

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated circuit conditions for other terminals. All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	NO CONNECTION			
2	-9.5	0	6 12 3 9 10 11	0 0 -9.5 +6 +6 +6
3	-12	0	2 6 9 10 11 12	0 0 +6 +6 +6 0
4	-12	0	2 6 9 10 11 12	0 0 +6 +6 +6 0
5	-6	0	2,6,12 3 9 10 11	0 -6 +6 +6 +6
6	-3.5	+3.5	2 3 9 10 11 12	0 -6 +6 +6 +6 0
7	NO CONNECTION			
8	NO CONNECTION			
9	0	+12	2 3 6 10 11 12	0 -6 0 +6 +6 0
10	0	+12	2 3 6 9 11 12	0 -6 0 +6 +6 0
11	0	+12	2 3 6 10 11 12	0 -6 0 +6 +6 0
12	-3.5	+3.5	2 3 6 9 10 11	0 -6 0 +6 +6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL NO.3 (SUBSTRATE) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±3.5 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	-2.5 V, +3.5 V
MAXIMUM DEVICE DISSIPATION	300 mW

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004

(Figs. 2 to 8)

INPUT OFFSET VOLTAGE AND CURRENT VS TEMPERATURE

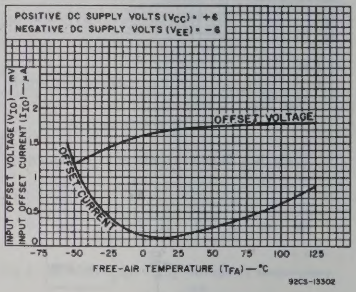


Fig.2

INPUT BIAS CURRENT VS TEMPERATURE

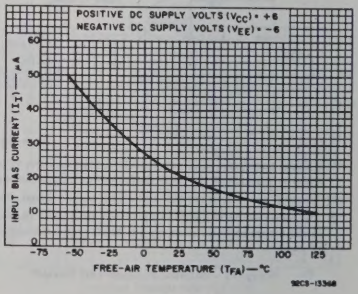


Fig.3

ELECTRICAL CHARACTERISTICS, at $T_{FA} = 25^{\circ}$ C, V_{CC} = +6V, V_{EE} = -6 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Open Unless Otherwise Specified		TEST CIRCUIT	LIMITS				TYPICAL CHARACTERISTICS CURVES
					TYPE CA3004				
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}			Fig.4	–	1.7	5	mV	Fig.2
Input Offset Current	I_{IO}			Fig.5	–	0.125	5	μA	Fig.2
Input Bias Current	I_I			Fig.5	–	21	40	μA	Fig.3
		TERMINALS							
		4	5						
Quiescent Operating Current	I_9 or I_{11}	NC	NC	Fig.8	–	1	–	mA	Fig.6
		V_{EE}	NC	Fig.8	–	2.7	–	mA	Fig.6
		NC	V_{EE}	Fig.8	–	0.45	–	mA	Fig.6
		V_{EE}	V_{EE}	Fig.8	–	1.25	–	mA	Fig.6
Quiescent Operating Current Ratio	I_9/I_{11}			Fig.8	–	1.1	–	–	Fig.7
Device Dissipation	P_T			Fig.8	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS									
Power Gain	G_P	f = 100 Mc/s		Fig.11	10	12	–	dB	Fig.9
Noise Figure	NF	f = 100 Mc/s		Fig.11	–	6.3	9	dB	Fig.10
Common Mode Rejection Ratio	CMR	f = 1 Kc/s		Fig.13	–	98	–	dB	Fig.12
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 Mc/s		Fig.14	-60	–	–	dB	NONE

DEFINITIONS OF TERMS

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Quiescent Operating Current Ratio

The ratio of the Quiescent operating currents in the two output terminals.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Common-Mode Voltage Gain

The ratio of the signal voltages developed between the two output terminals to the signal voltage applied to the two input terminals connected in parallel for ac.

Differential Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device

QUIESCENT OPERATING CURRENT RATIO VS TEMPERATURE

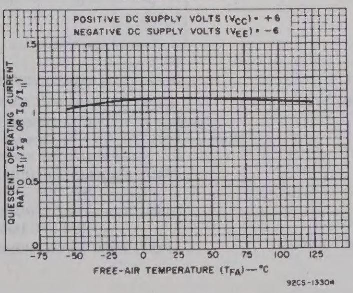


Fig.7

INPUT OFFSET VOLTAGE TEST CIRCUIT

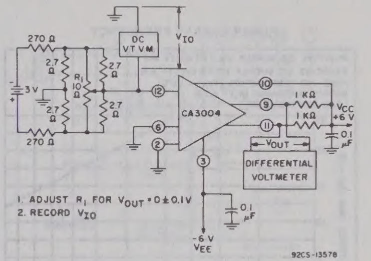
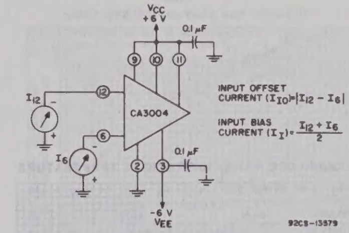


Fig.4

INPUT OFFSET CURRENT AND BIAS CURRENT TEST CIRCUIT



INPUT OFFSET CURRENT (I_{IO}) = $|I_{12} - I_6|$

INPUT BIAS CURRENT (I_I) = $\frac{I_{12} + I_6}{2}$

Fig.5

QUIESCENT OPERATING CURRENT VS TEMPERATURE

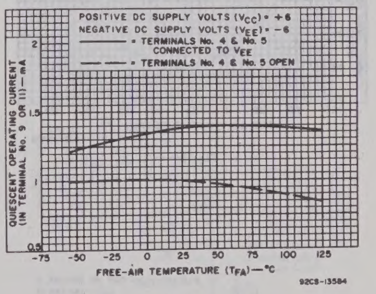
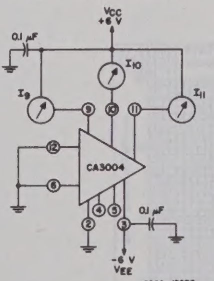


Fig.6

TEST CIRCUIT FOR TYPE CA3004

QUIESCENT OPERATING CURRENT, QUIESCENT OPERATING CURRENT RATIO, AND DEVICE DISSIPATION TEST CIRCUIT



$P_T = V_{CC}(I_9 + I_{10} + I_{11}) + V_{EE} I_3$

Fig.8

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004 (Figs. 9 to 14)

POWER GAIN VS FREQUENCY

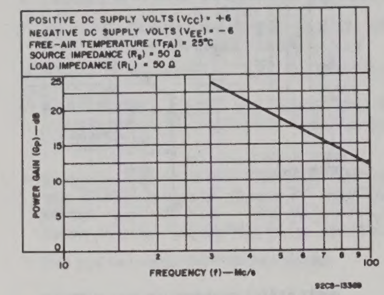


Fig. 9

NOISE FIGURE VS FREQUENCY

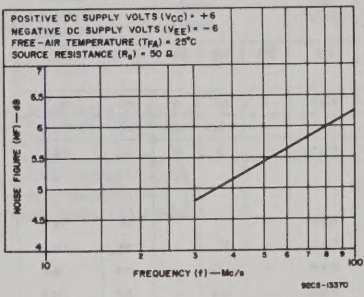


Fig. 10

100 Mc/s POWER GAIN AND NOISE FIGURE TEST CIRCUIT

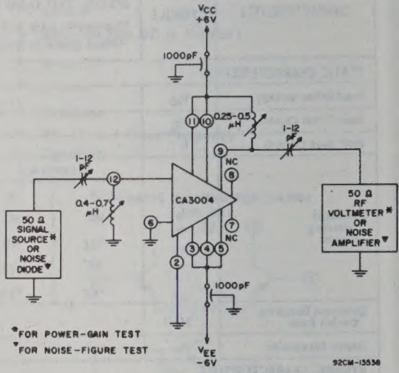


Fig. 11

COMMON-MODE REJECTION RATIO VS TEMPERATURE

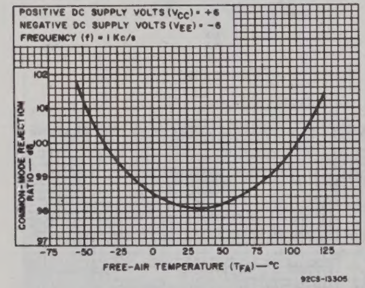


Fig. 12

COMMON-MODE REJECTION RATIO TEST CIRCUIT

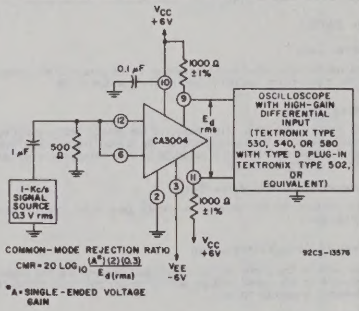

VCC
+6V
0.1 μF
10
1000 Ω ±1%
9
12
6
CA3004
Ed rms
OSCILLOSCOPE WITH HIGH-GAIN DIFFERENTIAL INPUT (TEKTRONIX TYPE 530, 540, OR 580 WITH TYPE D PLUG-IN TEKTRONIX TYPE 502, OR EQUIVALENT)
1 μF
500 Ω
1-Kc/s SIGNAL SOURCE 0.3 V rms
2
3
11
1000 Ω ±1%
VCC
+6V
VEE
-6V
COMMON-MODE REJECTION RATIO
CMR = 20 LOG10 (A*)(2)(0.3) / Ed(rms)
*A = SINGLE-ENDED VOLTAGE GAIN
92CS-13576

Fig. 13

AGC RANGE TEST CIRCUIT

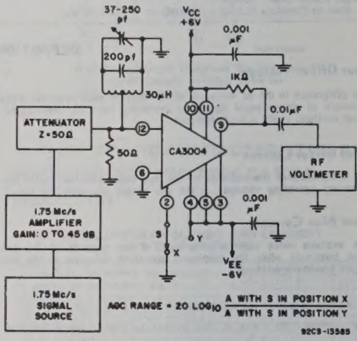


Fig. 14

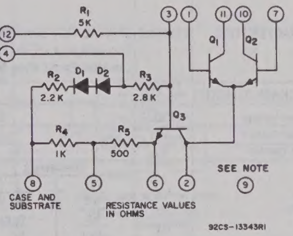
CA3005, CA3006

RF Amplifiers

- **Designed for use in Communications Equipment**
- **Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide Unexcelled Versatility**
- **Built-in Temperature Stability for Operation from -55° C to +125° C**
- **Companion Application Note, ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC limiter, detector, and amplifier design considerations.**
- 12-Lead Hermetic TO-5 Style Package.

- **Push-Pull Input and Output**
- **Wide and Narrow Band Amplifier**
- **AGC**
- **Detector**
- **RF, IF, and Video Frequency Capability**
- **Operation from DC to 100 MHz**
- **Mixer**
- **Limiter**
- **Modulator**
- **Cascode Amplifier**

SCHEMATIC DIAGRAM FOR CA3005 AND CA3006



NOTE: Connect Terminal No.9 to most positive dc supply voltage used for circuit.

Fig.1

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated voltage conditions for other terminals. All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3.5	+3.5	7 8 9 10 11 12	0 -6 +6 +6 +6 0
2	TEST POINT: DO NOT APPLY VOLTAGE FROM EXTERNAL SOURCE			
3	-9.5	0	1 7 8 9 10 11 12	0 0 -9.5 +6 +6 +6 0
4	-6	0	1 7 8 9 10 11 12	0 0 -6 +6 +6 +6 0
5	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
6	-6	0	1 7 9 10 11 12	0 0 +6 +6 +6 -6
7	-3.5	+3.5	1 8 9 10 11 12	0 -6 +6 +6 +6 0
8	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
9	0	+12	1 7 8 10 11 12	0 0 -6 +6 +6 0
10	0	+12	1 7 8 9 11 12	0 0 -6 +6 +6 0
11	0	+12	1 7 8 9 10 12	0 0 -6 +6 +6 0
12	-9.5	0	8 9 10 11	-9.5 +6 +6 +6
CASE	Internally connected to Terminal No.8 (substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±3.5 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	-2.5 V, +3.5 V
MAXIMUM DEVICE DISSIPATION	300 mW

INPUT OFFSET VOLTAGE AND CURRENT

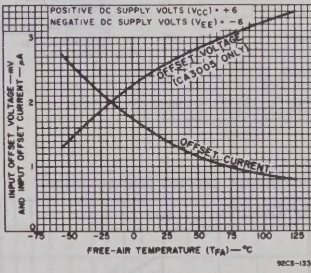
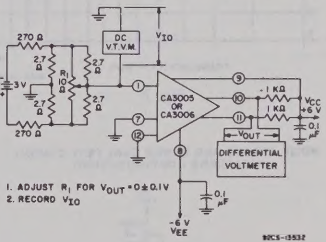


Fig.2

INPUT OFFSET VOLTAGE TEST CIRCUIT



1. ADJUST R_1 FOR V_{OUT} = 0 ± 0.1V
2. RECORD V_{IO}

Fig.3

INPUT BIAS CURRENT

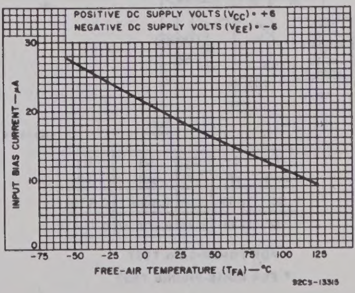


Fig.4

CA3005, CA3006

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, V_{CC} = +6V, V_{EE} = -6V

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.3,4,5, and 6 Not Connected Except Where Noted		TEST CIRCUITS	LIMITS							TYPICAL CHARAC-TERISTICS CURVES
					TYPE CA3005			TYPE CA3006				
				Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}			Fig.3	–	2.6	5	–	0.8	1	mV	Fig.2
Input Offset Current	I_{IO}			Fig.4	–	1.4	–	–	1.4	–	μA	Fig.2
Input Bias Current	I_{IB}			Fig.4	–	19	40	–	19	40	μA	Fig.5
Quiescent Operating Current	I_{10} or I_{11}	TERMINALS										
		4	5									
		NC	NC	Fig. 10	–	1	–	–	1	–	mA	Fig.6
		NC	$-V_{EE}$	Fig. 10	–	2.7	–	–	2.7	–	mA	NONE
		$-V_{EE}$	NC	Fig. 10	–	0.45	–	–	0.45	–	mA	NONE
		$-V_{EE}$	$-V_{EE}$	Fig. 10	–	1.25	–	–	1.25	–	mA	Fig.6
Quiescent Operating Current Ratio	$\frac{I_{10}}{I_{11}}$			Fig. 10	–	1.05	–	–	1.05	–	–	Fig.7
Device Dissipation	P_T			Fig. 10	–	26	–	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS												
Power Gain	G_p	f = 100 MHz	Cascode Configuration	Fig. 11	16	20	–	16	20	–	dB	Fig.9
			Differential-Ampl. Configuration	Fig.12	14	16	–	14	16	–	dB	Fig.11
Noise Figure	NF	f = 100 MHz	Cascode Configuration	Fig. 11	–	7.8	9	–	7.8	9	dB	Fig.13
			Differential Ampl. Configuration	Fig.12	–	7.8	9	–	7.8	9	dB	Fig.14
Common-Mode Rejection Ratio	CMR	f = 1 kHz			–	101	–	–	101	–	dB	Fig.15
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 MHz			-60	–	–	-60	–	–	dB	NONE

QUIESCENT OPERATING CURRENT

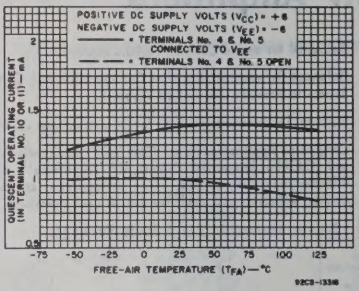


Fig. 5

QUIESCENT OPERATING CURRENT RATIO

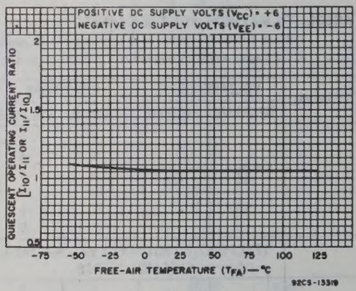


Fig. 6

POWER-GAIN (CASCODE CONFIGURATION)

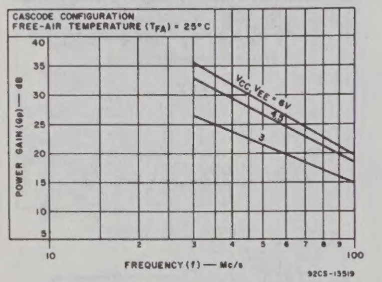


Fig. 7

POWER-GAIN (DIFFERENTIAL-AMPLIFIER CONFIGURATION)

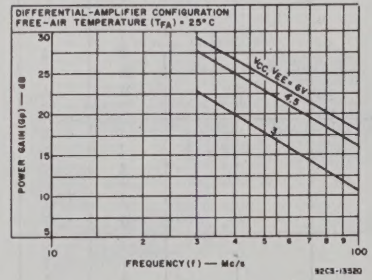


Fig. 8

100-Mc/s NOISE FIGURE VS. V_{EE} (CASCODE CONFIGURATION)

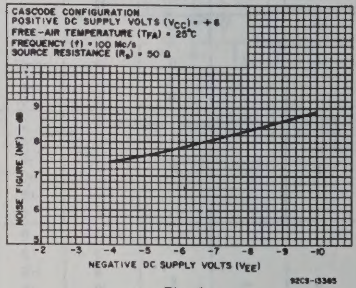
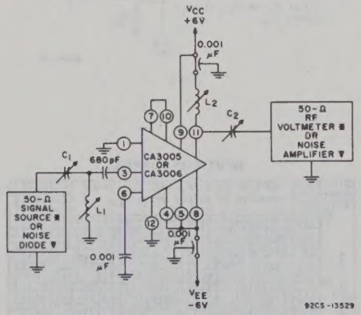


Fig. 9

NOISE FIGURE AND POWER GAIN TEST CIRCUIT (CASCODE CONFIGURATION)

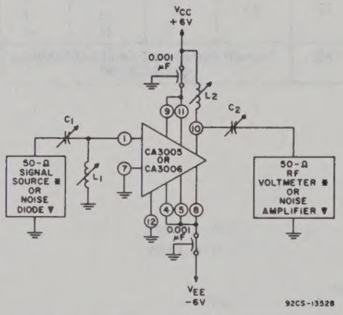


f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	14-150	5-40	0.3-0.6	0.8-1.4
100	5-40	5-40	0.07-0.12	0.15-0.3

- ■ FOR POWER-GAIN TEST
- ▼ FOR NOISE-FIGURE TEST

Fig. 10

NOISE FIGURE AND POWER-GAIN TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION)



f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	5-40	1.5-20	1.2-2	1.2-2
100	1-12	1-12	0.4-0.7	0.25-0.5

- ■ FOR POWER-GAIN TEST
- ▼ FOR NOISE-FIGURE TEST

Fig. 11

100 Mc/s NOISE FIGURE VS. V_{EE} (DIFFERENTIAL AMPLIFIER CONFIGURATION)

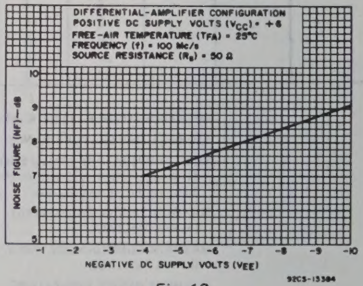


Fig. 12

COMMON-MODE-REJECTION RATIO

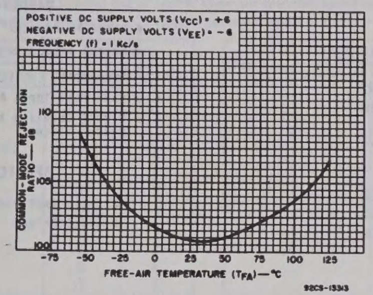


Fig. 13

COMMON–MODE-REJECTION RATIO
TEST CIRCUIT

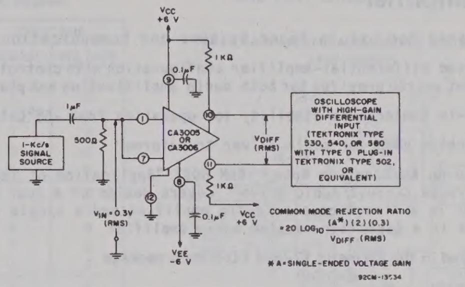

V_{CC} +6 V
1 KΩ
0.1μF
1μF
500Ω
1-Kc/s SIGNAL SOURCE
CA3005 OR CA3006
1
7
9
10
11
8
12
V_{DIFF} (RMS)
OSCILLOSCOPE WITH HIGH-GAIN DIFFERENTIAL INPUT (TEKTRONIX TYPE 530, 540, OR 580 WITH TYPE D PLUG-IN TEKTRONIX TYPE 502, OR EQUIVALENT)
1 KΩ
V_{IN} = 0.3V (RMS)
0.1μF
V_{CC} +6 V
V_{EE} −6 V
COMMON MODE REJECTION RATIO
$= 20 \log_{10} \frac{(A^*)(2)(0.3)}{V_{DIFF}\ (RMS)}$
* A = SINGLE-ENDED VOLTAGE GAIN
92CM-13534

Fig. 14

AGC RANGE TEST CIRCUIT

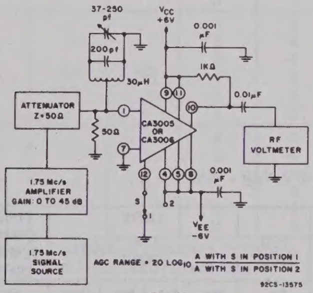


Fig. 15

CA3007

AF Amplifier

- Designed for use in Sound Systems and Communication Equipment
- Balanced differential-amplifier configuration with controlled constant-current source provides for both audio amplification and phase inversion
- Built-in temperature stability for operation from -55°C to +125°C
- Eliminates need for audio driver transformer
- Companion Application Note, ICAN 5037 "Application of the RCA-CA3007 Integrated Circuit Audio Driver" covers design of a dual supply audio driver in a direct-coupled audio amplifier, and a single supply audio driver in a capacitor-coupled audio amplifier
- **Supplied in the hermetic 12-lead TO-5 style package**

HIGHLIGHTS

Input Impedance. . . .	4 kΩ typ.
Output Impedance . . .	60 Ω typ.
Power Gain	22 dB typ.

- Push-Pull Input & Output
- Direct Coupling to Class B Audio Output Stage

APPLICATIONS

- Audio Amplifier
- Audio Driver

OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±2.5 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	±2.5 V
MAXIMUM DEVICE DISSIPATION	300 mW

ELECTRICAL CHARACTERISTICS, at $T_{FA} = 25°C$, $V_{CC} = +6$ V, $V_{EE} = -6$ V,

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Pin 4 Not Connected Unless Otherwise Noted	TEST CIRCUITS	LIMITS TYPE CA3007				TYPICAL CHARAC-TERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS								
Input Unbalance Voltage	V_{IU}		3	–	0.57	5	mV	2
Input Unbalance Current	I_{IU}		3	–	0.57	5	μA	2
Input Bias Current	I_I		3	–	11	34	μA	4
Quiescent Operating Voltage	V_8 or V_{10}		3	–	0.87	–	V	5
Device Dissipation	P_T		3	–	30	–	mW	NONE
DYNAMIC CHARACTERISTICS								
Power Gain	G_P	f = 1 Kc/s	6	20	22	–	dB	NONE
Total Harmonic Distortion	THD	f = 1 Kc/s	6	–	0.28	–	%	NONE
Input Impedance	Z_{IN}	f = 1 Kc/s	7	–	4K	–	Ω	NONE
Common-Mode Rejection Ratio	CMR	f = 1 Kc/s	9(A) 9(B)	–	77	–	dB	8

SCHEMATIC DIAGRAM

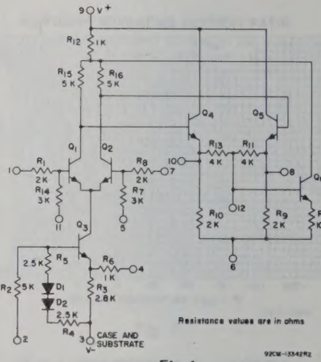


Fig.1

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUIT FOR CA3007

INPUT UNBALANCE VOLTAGE AND CURRENT vs TEMPERATURE

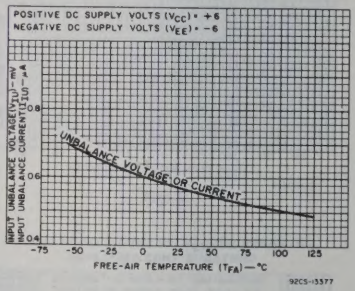
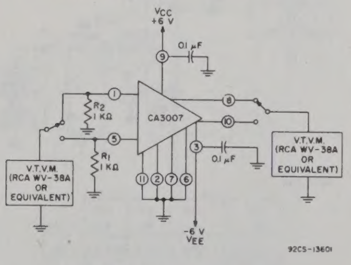


Fig.2

INPUT UNBALANCE VOLTAGE & CURRENT, INPUT BIAS CURRENT, QUIESCENT OPERATING VOLTAGE, AND DEVICE DISSIPATION TEST CIRCUIT


VCC +6 V
0.1 μF
9
R2 1 KΩ
1
5
R1 1 KΩ
CA3007
8
10
3
0.1 μF
11
2
7
6
V.T.V.M. (RCA WV-38A OR EQUIVALENT)
V.T.V.M. (RCA WV-38A OR EQUIVALENT)
-6 V VEE
92CS-13601

R_1 and R_2 matched to ± 1%.

$P_T = V_{CC}I_9 + V_{EE}I_3$

I_9 = Direct Current into Terminal No.9

I_3 = Direct Current out of Terminal No.3

Fig.3

INPUT BIAS CURRENT vs TEMPERATURE

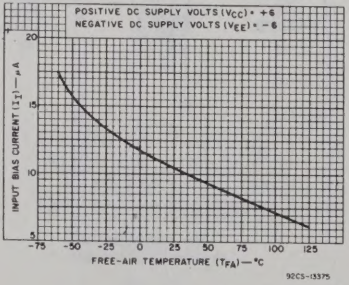


Fig.4

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

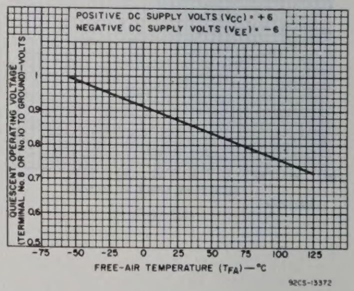


Fig.5

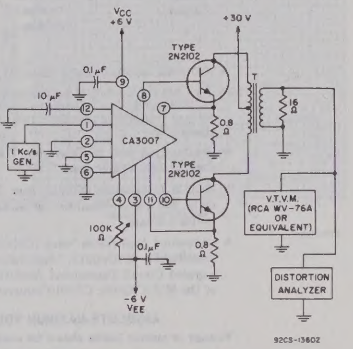
ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at $T_A = 25^\circ C$

Indicated voltage limits for each terminal can be applied under the specified operating conditions for other terminals. All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$, or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2 3 6 7 9 11	0 -6 0 0 +6 0
2	-8	0	3 6 7 9 11	-8 0 0 +6 0
3	-10	0	6 7 9 11	0 0 +6 0
4	-8.5	0	6 7 9 11	0 0 +6 0
5	-2.5	+2.5	2 3 6 7 9 11	0 -6 0 0 +6 0
6	-3	0	2 3 7 9 11	0 -6 0 +6 0
7	-2.5	+2.5	1 2 3 5 6 9	0 0 -6 0 0 +6
8	-2	0	2 3 6 7 9 11	0 -6 0 0 +6 0
9	0	+10	2 3 6 7 11	0 -6 0 0 0
10	-2	0	2 3 6 7 9 11	0 -6 0 0 +6 0
11	-2.5	+2.5	1 2 3 6 7 9	0 0 -6 0 0 +6
12	-2	0	2 3 6 7 9 11	0 -6 0 0 +6 0
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

TYPICAL DYNAMIC CHARACTERISTIC AND TEST CIRCUITS FOR CA3007

POWER GAIN AND TOTAL HARMONIC DISTORTION TEST CIRCUIT



T (Output Transformer):
Primary Impedance = 2000 Ω C.T.
Secondary Impedance = 16 Ω
Efficiency = 45% approx.
(STANCOR TYPE TA-10 OR EQUIVALENT)

Fig.6

INPUT IMPEDANCE TEST CIRCUIT

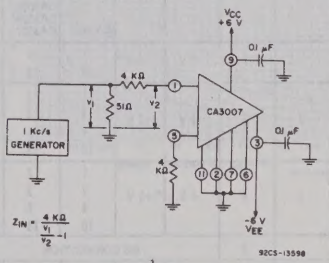


Fig.7

COMMON-MODE REJECTION RATIO vs TEMPERATURE

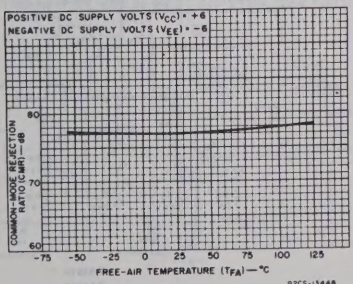
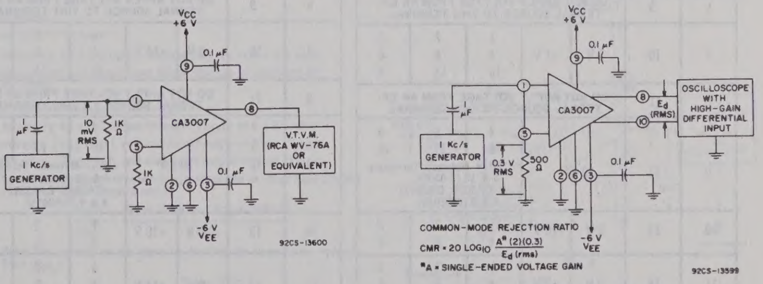


Fig.8

COMMON-MODE REJECTION-RATIO TEST CIRCUITS


VCC +6 V
0.1 µF
1 µF
10 mV RMS
1K Ω
CA3007
V.T.V.M. (RCA WV-76A OR EQUIVALENT)
1 Kc/s GENERATOR
1K Ω
0.1 µF
-6 V VEE
92CS-13600
VCC +6 V
0.1 µF
1 µF
CA3007
Ed (RMS)
OSCILLOSCOPE WITH HIGH-GAIN DIFFERENTIAL INPUT
1 Kc/s GENERATOR
0.3 V RMS
500 Ω
0.1 µF
-6 V VEE
COMMON-MODE REJECTION RATIO
CMR = 20 LOG10 A* (2)(0.3) / Ed (rms)
*A = SINGLE-ENDED VOLTAGE GAIN
92CS-13599

(A) Single-Ended Differential Voltage Gain

(B) Common-Mode Voltage Gain

Fig.9

CA3008, CA3010, CA3015, CA3016, CA3029,CA3030, CA3037, CA3038

Operational Amplifiers

6-VOLT TYPES	*12-VOLT TYPES*	*PACKAGE*
CA3008	CA3016	14-Lead Flat Pack
CA3010	CA3015	12-Lead TO-5 Style
CA3029	CA3015L	Beam-Lead Device
CA3037	CA3030	14-Lead Plastic Dual In-Line (TO-116)
	CA3038	14-Lead Ceramic Dual In-Line (TO-116)

- All types are electrically identical within their voltage groups
- The CA3105 is available in a sealed-junction Beam-Lead version (CA3015L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications.
- Designed for use in Telemetry, Data-Processing, Instrumentation, and Communication Equipment
- Built-in temperature stability from -55°C to +125°C for flatpack, TO-5 style, and ceramic dual in-line packages: 0°C to +70°C for plastic dual in-line package
- Companion Application Notes ICAN-5290, "Integrated Circuit Operational Amplifiers"; ICAN-5213, "Application of the RCA-CA3015, CA3016 Integrated Circuit Operational Amplifiers"; and ICAN-5015, "Application of the RCA-CA3008, CA3010 Integrated Circuit Operational Amplifiers";

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010	CA3008 CA3029 CA3037	Nega-tive	Posi-tive	Terminal		Voltage
				CA3010	CA3008 CA3029 CA3037	
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008, CA3029, CA3037) 4 & 9 (CA3010)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010 (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015	CA3016 CA3030 CA3038	Nega-tive	Posi-tive	Terminal		Voltage
				CA3015	CA3016 CA3030 CA3038	
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016, CA3030, CA3038) 4 & 9 (CA3015)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015 (Substrate) DO NOT GROUND				

	CA3008 CA3010 CA3016 CA3015 CA3037 CA3038	CA3029 CA3030
OPERATING TEMPERATURE RANGE . .	-55°C to +125°C	-40°C to +85°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C	-65°C to +150°C

	CA3016 CA3015 CA3030 CA3038	CA3008 CA3010 CA3029 CA3037
MAXIMUM SIGNAL VOLTAGE.	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

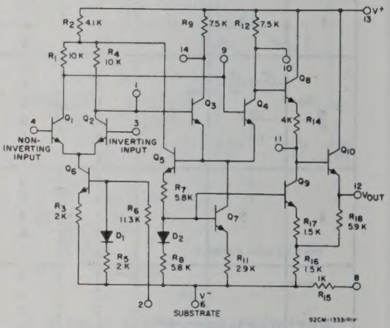
HIGHLIGHTS

	6 V Types	12 V Types	
• Open-Loop Voltage Gain	60	70	dB typ.
• Common-Mode Rejection Ratio	94	103	dB typ.
• Output Impedance	200	92	Ω typ.
• Input Offset Voltage	1	1	mV typ.
• Static Power Drain at ± 12 V	-	175	mW typ.
± 6 V	30	30	mW typ.
± 3 V	7	7	mW typ.

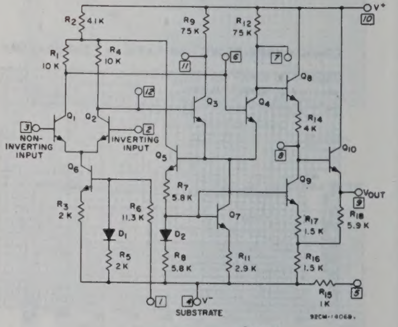
APPLICATIONS

- Narrow-Band and Band-pass Amplifier
- Operational Functions
- Feedback Amplifier
- DC and Video Amplifier
- Multivibrator
- Oscillator
- Comparator
- Servo Driver
- Scaling Adder
- Balanced Modulator-Driver

SCHEMATIC DIAGRAMS



CA3008 CA3016 CA3029 CA3030 CA3037 CA3038



CA3010 CA3015

Fig.1

CA3008, CA3010, CA3015, CA3016, CA3029,CA3030, CA3037, CA3038

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008, CA3016, CA3029, CA3030, CA3037, CA3038) Terminal No.5 (CA3010, CA3015) Not Connected Unless Otherwise Specified	Test Circuit	CA3008 CA3010 CA3029 CA3037			CA3016 CA3015 CA3030 CA3038			Units	Typical Characteristic Curves
			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	1.08 -	5 -	- -	- 1.37	- 5	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.54 -	5 -	- -	- 1.07	- 5	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	5.3 -	12 -	- -	- 9.6	- 24	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	30 -	- -	- -	- 175	- -	mW	none
		5 shorted to 9 V_{CC} = +6V V_{EE} = -6V		-	102	-	-	-	-		
		8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	500	-		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Common-Mode Rejection Ratio	CMRR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	10 -	14 -	- -	- 5	- 7.8	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	200 -	- -	- -	- 92	- -	Ω	15
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	0.5 to -4 -	- -	- -	- 0.65 to -8	- -	- -	V	none

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. .... +265°C

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

INPUT OFFSET VOLTAGE AND CURRENT

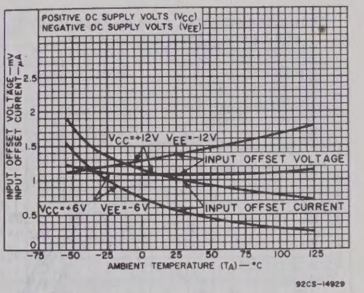


Fig.2

INPUT BIAS CURRENT

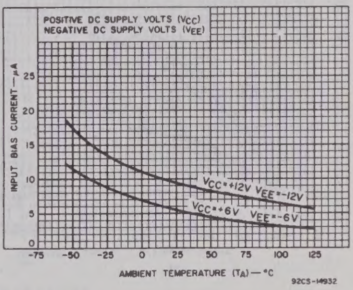


Fig.3

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

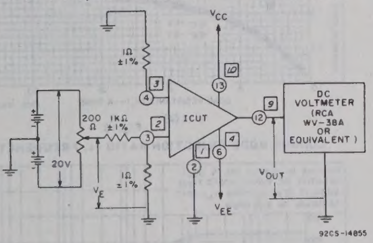


Fig.4

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference betwзen V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\text{ (Step 2) - }V_{OUT}\text{ (Step 3)}}{\text{2 volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$
I_C = Direct Current into Terminal ⑬ or *10*
I_E = Direct Current out of Terminal ⑥ or *4*

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

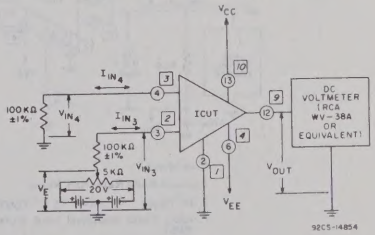


Fig.5

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}.
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038

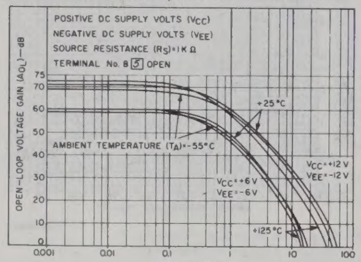


Fig.6

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029 AND CA3030

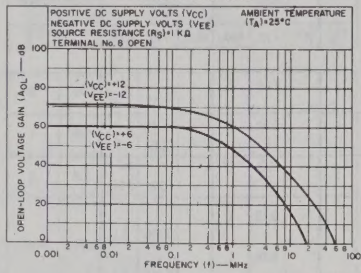
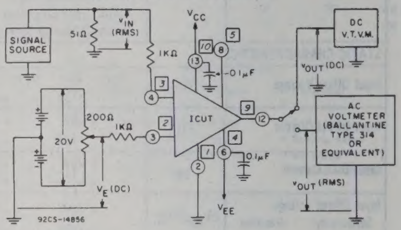


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, AND OPEN-LOOP BANDWIDTH AT −3 dB POINT TEST CIRCUIT



Procedure:

1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz.

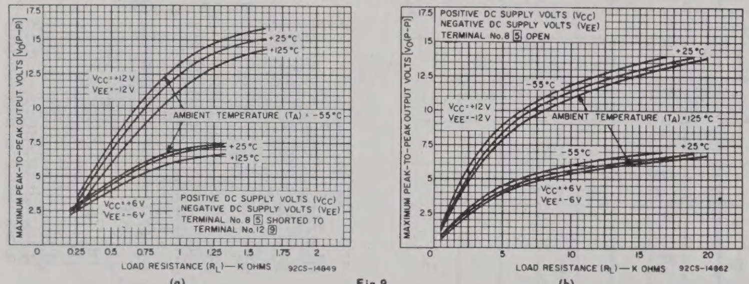
$$A_{OL} = 20\ \mathrm{Log}_{10}\frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz.
4. Measure Open-Loop Bandwidth at -3 dB Point.

Reference Level = A_{OL} at 1 kHz.

Fig.8

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038



(a) Fig.9 (b)

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029 AND CA3030

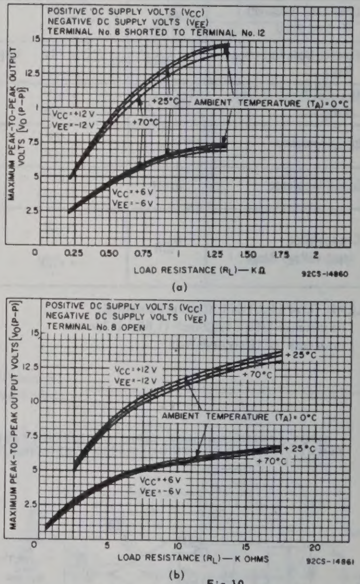
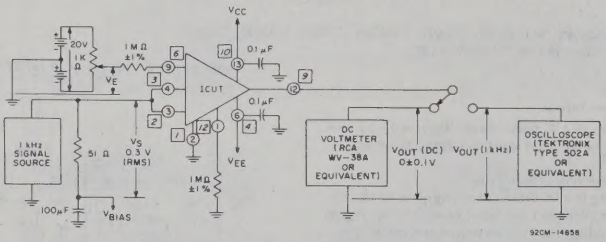


Fig.10

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for $V_{OUT}(DC)$ = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$
$$A_{CM} \text{ in dB} = -20\,\mathrm{LOG}_{10}\, V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$\text{CMR in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB.}$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig.11

COMMON-MODE REJECTION RATIO vs. FREQUENCY

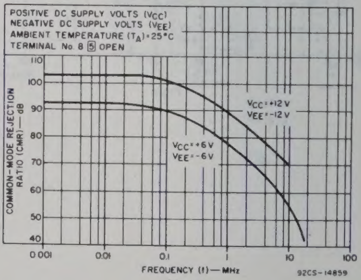


Fig.12

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

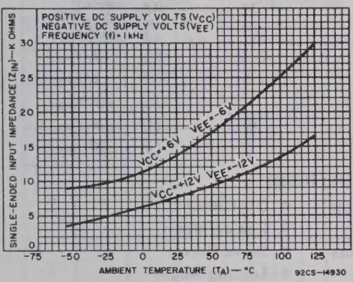


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

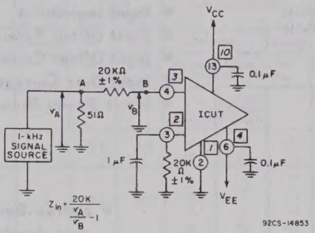


Fig.14

JTPUT IMPEDANCE vs. TEMPERATURE

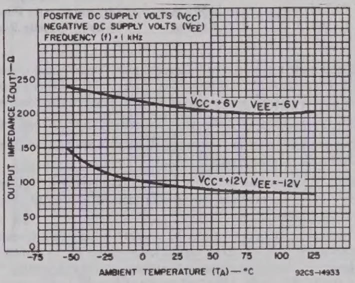
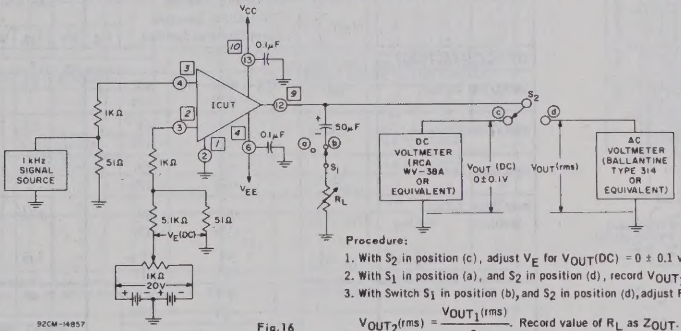


Fig.15

OUTPUT IMPEDANCE TEST CIRCUIT



Procedure:

1. With S_2 in position (c), adjust V_E for V_{OUT}(DC) = 0 ± 0.1 volt.
2. With S_1 in position (a), and S_2 in position (d), record V_{OUT_1}(rms).
3. With Switch S_1 in position (b), and S_2 in position (d), adjust R_L until

$$V_{OUT_2}(\text{rms}) = \frac{V_{OUT_1}(\text{rms})}{2}.$$ Record value of R_L as Z_{OUT}.

Fig.16

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

Operational Amplifiers

6-VOLT TYPES	12-VOLT TYPES	PACKAGE
CA3008A	CA3016A	14-Lead Flat Pack
CA3010A	CA3015A	12-Lead TO-5 Style
CA3029A	CA3030A	14-Lead Plastic Dual In-Line (TO-116)
CA3037A	CA3038A	14-Lead Ceramic Dual In-Line (TO-116)

- These new types have all the desirable features and characteristics of their prototypes plus lower noise figures and improved input characteristics for offset voltage, offset current, bias current, and impedance.
- All types are electrically identical within their voltage groups
- Designed for use in Telemetry, Data-Processing, Instrumentation, and Communication Equipment
- Built-in temperature stability from -55°C to +125°C for Flatpack, TO-5 style, and ceramic dual in-line packages; 0°C to +70°C for plastic dual in-line package
- Companion Application Notes ICAN-5290, "Integrated Circuit Operational Amplifiers"; ICAN-5213, "Application of the RCA-CA3015, CA3016 Integrated Circuit Operational Amplifiers"; and ICAN-5015, "Application of the RCA-CA3008, CA3010 Integrated Circuit Operational Amplifiers" cover Bode characteristics, phase compensation, frequency shaping, and amplifier design.

HIGHLIGHTS

	6 V Types	12 V Types	
• Open-Loop Voltage Gain	60	70	dB typ.
• Common-Mode Rejection Ratio	94	103	dB typ.
• Input Impedance	20	10	k typ.
• Input Offset Voltage	0.9	1	mV typ.
• Input Offset Current	0.3	0.5	A typ.
• Input Bias Current	2.5	4.7	A typ.
• Static Power Drain at 12 V	-	175	mW typ.
at 6 V	30	30	mW typ.
at 3 V	7	7	mW typ.

APPLICATIONS

- Narrow-Band and Band-pass Amplifier
- Operational Functions
- Feedback Amplifier
- DC and Video Amplifier
- Multivibrator
- Oscillator
- Comparator
- Servo Driver
- Scaling Adder
- Balanced Modulator-Driver

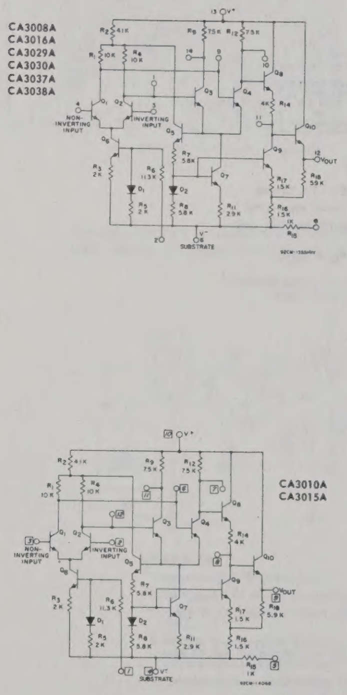


Fig.1

SCHEMATIC DIAGRAMS

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A), Terminal No.5 (CA3010A, CA3015A) Not Connected Unless Otherwise Specified	Test Circuit	CA3008A CA3010A CA3029A CA3037A			CA3016A CA3015A CA3030A CA3038A			Units	Typical Characteristic Curves
			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	0.9 -	2 -	- -	- 1	- 2	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.3 -	1.5 -	- -	- 0.5	- 1.6	µA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	2.5 -	4 -	- -	- 4.7	- 6	µA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	40 -	- -	- -	- 175	- -	mW	none
		5 shorted to 9 V_{CC} = +6V V_{EE} = -6V		-	102	-	-	-	-		
		8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	500	-		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Slew Rate	SR	V_{CC} = +6V V_{EE} = -6V = +12V = -12V; R_S = 1 kΩ	none	- -	3 -	- -	- -	- 7	- -	V/µs	none
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	15 -	20 -	- -	- 7.5	- 10	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	160 -	- -	- -	- 85	- -	Ω	16
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	+0.5 -4 -	- - -	- -	- +0.65 -8	- -	- -	V	none
Noise Figure	NF	V_{CC} = +3V, V_{EE} = -3V = +6V = -6V = +9V = -9V = +12V = -12V; R_S = 1 kΩ	18	- - - -	6.3 8.3 - -	9 12 - -	- - - -	6.3 8.3 10 11	9 12 14 16	dB	17

LEAD TEMPERATURE (During Soldering):	ALL TYPES
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010A	CA3008A CA3029A CA3037A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010A	CA3008A CA3029A CA3037A	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
-	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008A, CA3029A, CA3037A) 4 & 9 (CA3010A)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010A (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015A	CA3016A CA3030A CA3038A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015A	CA3016A CA3030A CA3038A	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
-	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016A, CA3030A, CA3038A) 4 & 9 (CA3015A)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015A (Substrate) DO NOT GROUND				

	CA3008A CA3010A CA3016A CA3015A CA3037A CA3038A	CA3029A CA3030A
OPERATING TEMPERATURE RANGE	-55°C to +125°C	-40°C to +80°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-65°C to +150°C

	CA3016A CA3015A CA3030A CA3038A	CA3008A CA3010A CA3029A CA3037A
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

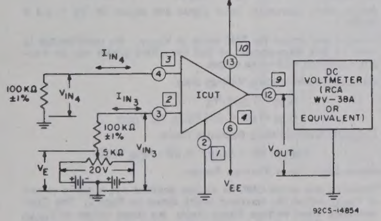


Fig.5

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}
3. Calculate the Input Bias Current using the following equation:

$$I_{14} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A;

Italic Numbers in Square Boxes are for CA3010A, CA3015A

INPUT OFFSET VOLTAGE AND CURRENT

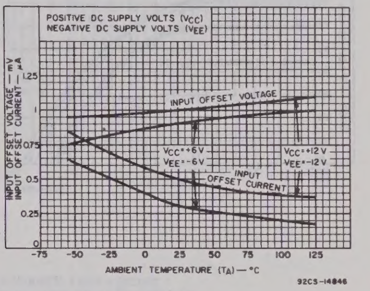


Fig.2

INPUT BIAS CURRENT

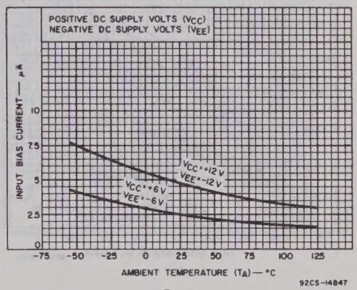


Fig.3

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

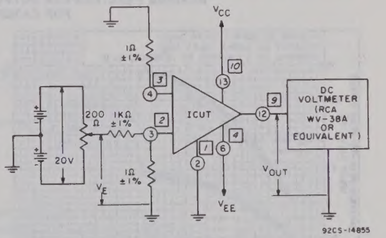


Fig.4

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\text{ (Step 2)} - V_{OUT}\text{ (Step 3)}}{2\text{ volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal 13 or $\boxed{10}$

I_E = Direct Current out of Terminal 6 or $\boxed{4}$

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A

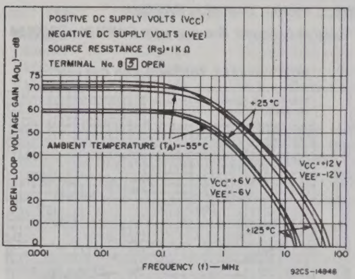


Fig.6

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029A AND CA3030A.

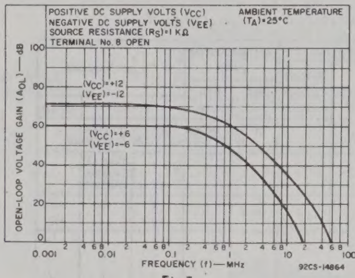
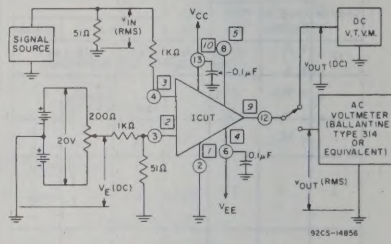


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, AND OPEN-LOOP BANDWIDTH AT −3 POINT TEST CIRCUIT



Procedure:

1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz

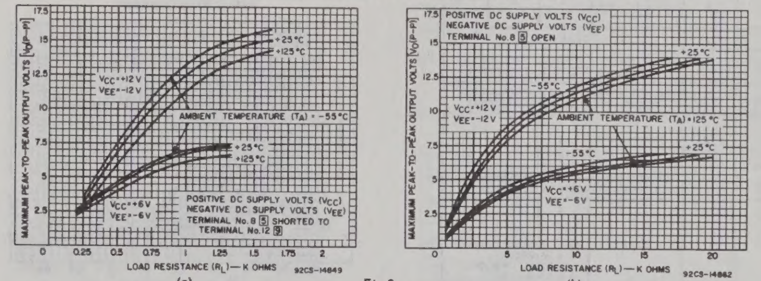
$$A_{OL} = 20 \text{ Log}_{10} \frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz
4. Measure Open-Loop Bandwidth at -3 dB Point

Reference Level = A_{OL} at 1 kHz

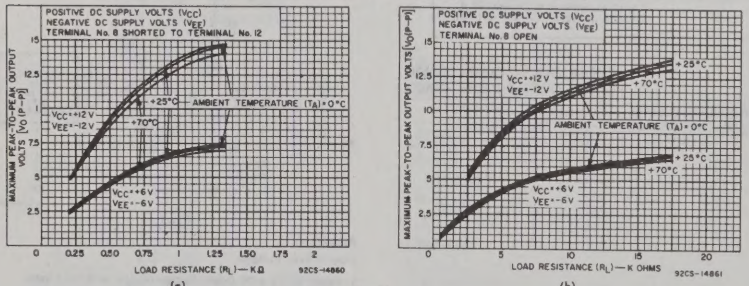
Fig.8

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A



(a) Fig.9 (b)

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029A AND CA3030A



(a) Fig.10 (b)

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT

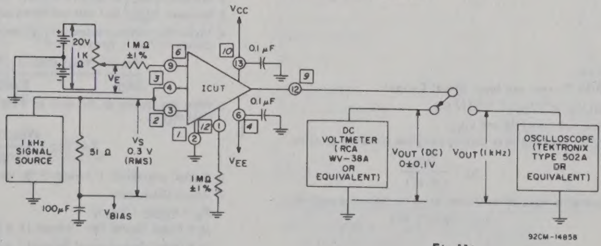


Fig.11

Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for $V_{OUT}(DC)$ = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated.from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$
$$A_{CM} \text{ in dB} = -20 \text{ LOG}_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$\text{CMR in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB.}$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

COMMON-MODE REJECTION RATIO vs. FREQUENCY

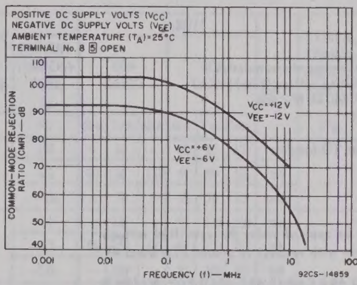


Fig.12

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

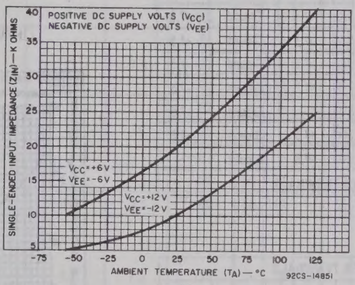


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

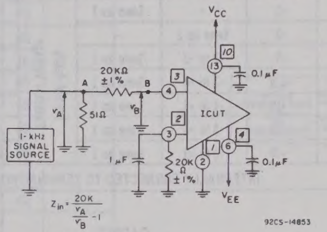
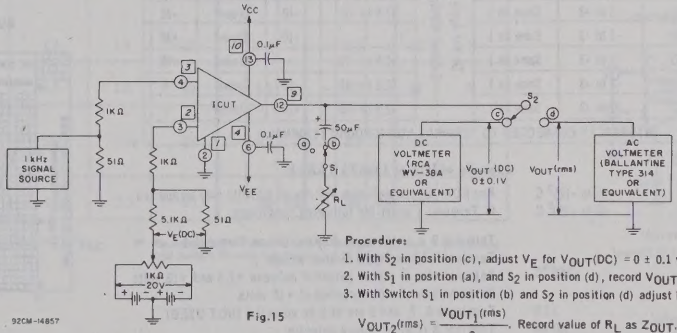


Fig.14

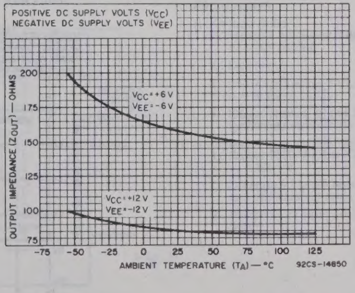
OUTPUT IMPEDANCE TEST CIRCUIT



Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b) and S_2 in position (d) adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.

Fig.15



OUTPUT IMPEDANCE vs. TEMPERATURE

Fig.16

NOISE FIGURE vs. FREQUENCY

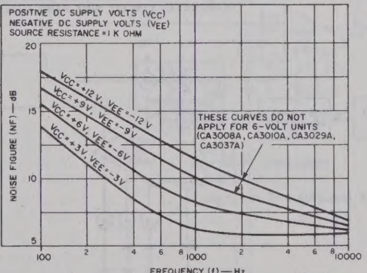


Fig.17

CA3011, CA3012

Wideband Amplifiers

FEATURES & APPLICATIONS

- exceptionally high amplifier gain:
  power gain at 4.5 MHz – 75 dB typ.
- excellent limiting characteristics –
  Input limiting voltage (knee) =
  600 μV typ. at 10.7 MHz
- wide frequency capability –
  100 kHz to > 20 MHz
- supplied in the hermetic 10-lead
  TO-5 style package

ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

NOTE: TERMINALS 6, 7, AND 9 OF RCA-CA3011 AND CA3012 ARE USED FOR INTERNAL CONNECTIONS. DO NOT APPLY VOLTAGES OR MAKE EXTERNAL CONNECTIONS TO THESE TERMINALS.

CA3011

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Ground	+7.5
2	-3	+3	Same as 2	–		+2.5 to +7.5	+7.5	Ground	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		–	+7.5	Ground	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	–	Ground	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

CA3012

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Ground	+10
2	-3	+3	Same as 2	–		+2.5 to +10	+10	Ground	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
4	+2.5	+10	-3 to +3	Same as 1		–	+10	Ground	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	–	Ground	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

OPERATING-TEMPERATURE RANGE	-55 to +125° C
STORAGE-TEMPERATURE RANGE	-65 to +150° C
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM INPUT-SIGNAL VOLTAGE: Between Terminals 1 and 2	±3 V
MAXIMUM DEVICE DISSIPATION	300 mW
RECOMMENDED MINIMUM DC SUPPLY VOLTAGE (V_{CC})	5.5 V

Example of Use of LIMITS TABLE:

For RCA-3012, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +10 volts
Terminal 5 is at a dc potential of +10 volts
Terminals 6, 7, and 9 are at 0 dc potential (NOT USED)
Terminal 8 is at dc ground potential
Terminal 10 is at a dc potential of +10 volts

BLOCK DIAGRAM OF TYPICAL FM RECEIVER USING RCA-CA3011 OR CA3012 INTEGRATED CIRCUIT WIDE-BAND AMPLIFIER

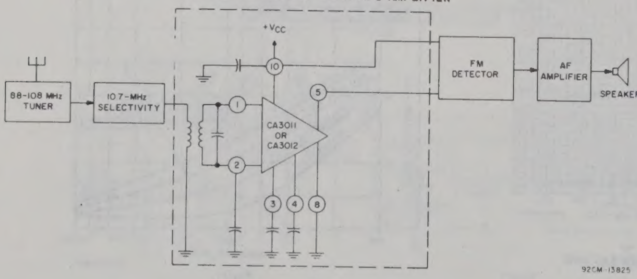


Fig. 4

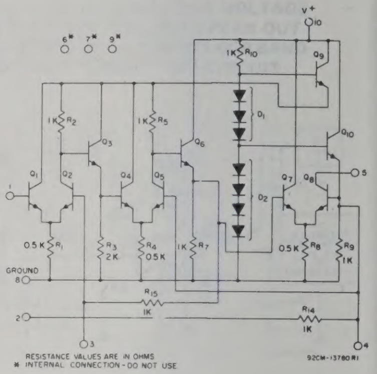


Fig. 1 – Schematic diagram for CA3011 and CA3012.

INPUT-IMPEDANCE COMPONENTS VS FREQUENCY

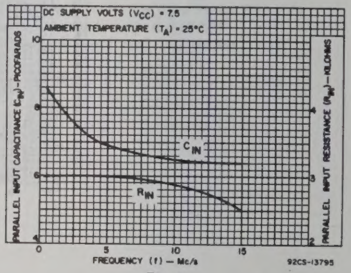


Fig. 2

OUTPUT-IMPEDANCE COMPONENTS VS FREQUENCY

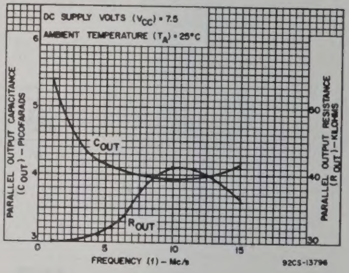


Fig. 3

VOLTAGE GAIN AND INPUT LIMITING VOLTAGE VS FREQUENCY

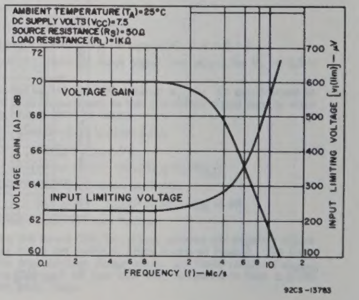


Fig. 5

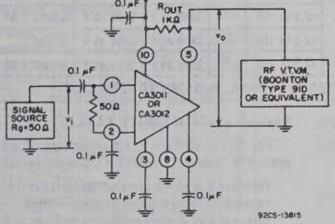
ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARAC-TERISTICS CURVES
		SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERA-TURE T_A	RCA CA3011			RCA CA3012				
		Fig.	Mc/s	Volts	°C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation *	P_T	6	–	6	-55	–	80	–	66	80	135	mW	
					+25	60	90	133	66	90	121	mW	
					+125	–	70	–	65	70	121	mW	
			–	7.5	-55	–	130	–	97	130	190	mW	
					+25	95	120	187	97	120	167	mW	
					+125	–	100	–	95	100	167	mW	
			–	10	-55	–	–	–	150	210	275	mW	
					+25	–	–	–	150	190	255	mW	
					+125	–	–	–	150	160	255	mW	
Voltage Gain**	A	9	1	6	-55	–	55	–	50	55	–	dB	
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
		9	1	7.5	-55	–	59	–	55	59	–	dB	
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
		9	1	10	-55	–	–	–	55	61	–	dB	
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
		9	4.5	7.5	+25	60	67	–	60	67	–	dB	5
			10.7	7.5	+25	55	61	–	55	61	–	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	7	4.5	7.5	+25	–	3	–	–	3	–	kΩ	2
Parallel Input Capacitance	C_{IN}	7	4.5	7.5	+25	–	7	–	–	7	–	pF	2
Output Impedance Components: Parallel Output Resistance	R_{OUT}	8	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	3
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	3
Noise Figure	NF	10	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	
Input Limiting Voltage (Knee)	$v_{i(lim)}$	9	4.5	7.5	+25	–	300	450	–	300	400	µV	

* The total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

VOLTAGE-GAIN TEST SETUP



PROCEDURES

A - Voltage Gain:
1) Set input frequency at desired value, v_i = 100 µV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

B - Input Limiting Voltage (Knee):
1) Repeat Steps A1 and A2, using v_i = 100 mV
2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.
3) Record v_i as Input Limiting Voltage (Knee).

Fig. 9

DISSIPATION TEST SETUP

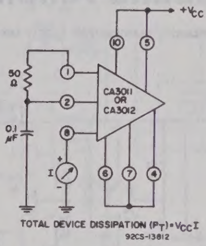


Fig. 6

INPUT-IMPEDANCE COMPONENTS TEST SETUP

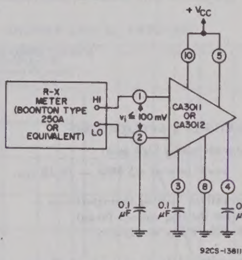


Fig. 7

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

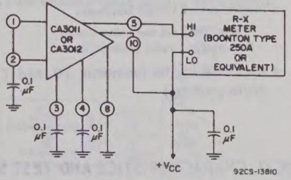
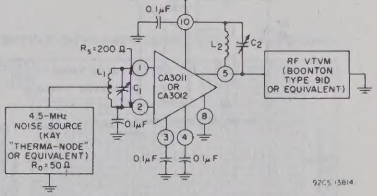


Fig. 8

NOISE FIGURE TEST SETUP


+VCC
0.1µF
10
Rs=200 Ω
L2
C2
L1
C1
1
2
CA3011 OR CA3012
5
RF VTVM (BOONTON TYPE 91D OR EQUIVALENT)
4.5-MHz NOISE SOURCE (KAY "THERMA-NODE" OR EQUIVALENT) Ro=50 Ω
0.1µF
8
3
4
0.1µF
0.1µF
92CS-13814

L_1 = 82 µH, center-tapped
L_2 = 2.36 µH
C_1,C_2 = Arco Type 423 padder, or equivalent

Fig. 10

CA3013, CA3014

Wideband Amplifier-Discriminators

SCHEMATIC DIAGRAM FOR CA3013 AND CA3014

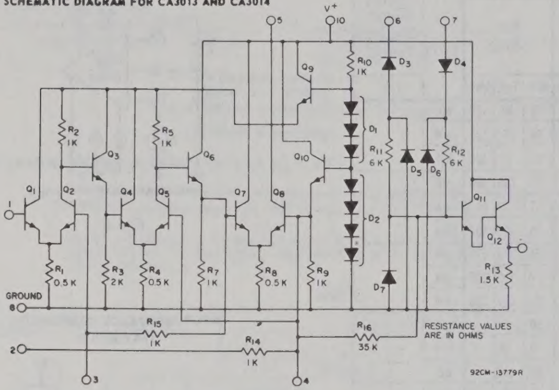


Fig. 1

BLOCK DIAGRAM OF TYPICAL TELEVISION RECEIVER USING RCA INTEGRATED-CIRCUIT SOUND-IF AMPLIFIER AND DETECTOR SECTION

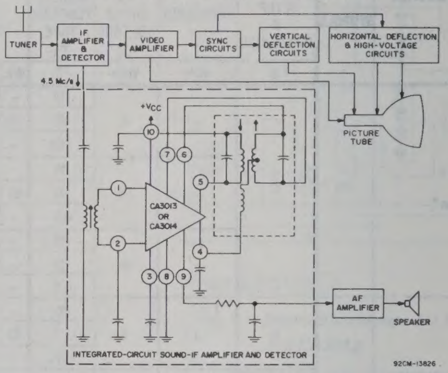


Fig. 2

FEATURES & APPLICATIONS:

- exceptionally high gain:
  power gain at 4.5 MHz — 75 dB typ.
- excellent limiting characteristics — input limiting voltage (knee) = 300 µV typ. at 4.5 MHz
- excellent AM rejection: > 50 dB at 4.5 MHz
- high audio-voltage recovery — 220 mV typ. at 4.5 MHz 25 kHz deviation
- wide frequency capability — 100 kHz to > 20 MHz
- comprehensive circuit functions:
  if amplifier, AM and noise limiter, FM detector, audio preamplifier
- supplied in the hermetic 10-lead TO-5 style package

TYPICAL CHARACTERISTICS AND TEST SETUPS

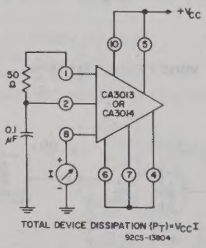


Fig.3

ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

CA3013

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
2	-3	+3	Same as 2	-		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		-	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	-	Same as 4	Same as 4	Ground	AF Output	+7.5
6	+2.5	+7.5	-3 to +3	Same as 1		Same as 6	+7.5	-	Same as 4	Ground	AF Output	+7.5
7	+2.5	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	-	Ground	AF Output	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
9	0	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	-	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

CA3014

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
2	-3	+3	Same as 2	-		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
4	+2.5	+10	-3 to +3	Same as 1		-	+10	Same as 4	Same as 4	Ground	AF Output	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	-	Same as 4	Same as 4	Ground	AF Output	+10
6	+2.5	+10	-3 to +3	Same as 1		Same as 6	+10	-	Same as 4	Ground	AF Output	+10
7	+2.5	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	-	Ground	AF Output	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
9	0	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	-	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

OPERATING-TEMPERATURE RANGE	-55 to +125°C
STORAGE-TEMPERATURE RANGE	-65 to +150°C
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max	+265°C
MAXIMUM INPUT-SIGNAL VOLTAGE: Between Terminals 1 and 2	± 3 V
MAXIMUM DEVICE DISSIPATION	300 mW
RECOMMENDED MINIMUM DC SUPPLY VOLTAGE (V_{CC})	5.5 V

Example of use of LIMITS TABLE:

For RCA-CA3013, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +7.5 volts
Terminal 5 is at a dc potential of +7.5 volts
Terminals 6 and 7 are at the same dc potential as Terminal 4
Terminal 8 is at dc ground potential
Terminal 9 is used as the af output terminal
Terminal 10 is at a dc potential of +7.5 volts

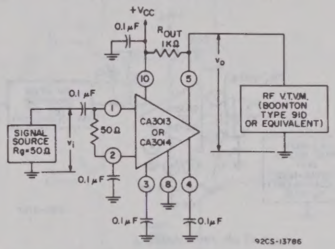
CA3013, CA3014

ELECTRICAL CHARACTERISTICS (See Page 8 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES
		SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERATURE T_A	RCA CA3013			RCA CA3014				
		Fig.	Mc/s	volts	^0C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation*	P_T	3	–	6	-55	–	80	–	73	80	120	mW	
					+25	60	90	133	73	90	110	mW	
					+125	–	70	–	60	70	110	mW	
		3	–	7.5	-55	–	130	–	106	130	170	mW	
					+25	87	120	187	106	120	150	mW	
					+125	–	100	–	90	100	150	mW	
		3	–	10	-55	–	–	–	165	210	250	mW	
					+25	–	–	–	165	190	230	mW	
					+125	–	–	–	150	160	230	mW	
Voltage Gain**	A	4	1	6	-55	–	55	–	50	55	–	dB	
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
		4	1	7.5	-55	–	59	–	55	59	–	dB	
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
		4	1	10	-55	–	–	–	55	61	–	dB	
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
		4	4.5	7.5	+25	60	67	–	60	67	–	dB	5
			10.7	7.5	+25	55	60	–	55	60	–	dB	
Input-Impedance Components:													
Parallel Input Resistance	R_{IN}	6	4.5	7.5	+25	–	3	–	–	3	–	kΩ	7
Parallel Input Capacitance	C_{IN}	6	4.5	7.5	+25	–	7	–	–	7	–	pF	7
Output-Impedance Components:													
Parallel Output Resistance	R_{OUT}	8	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	9
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	9
Noise Figure	NF	10	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	11
Input Limiting Voltage (Knee)	$v_i(lim)$	14	4.5	7.5	+25	–	300	450	–	300	400	μV	13
Recovered AF Voltage	$v_0(af)$	14	4.5	6	+25	–	155	–	–	155	–	mV	13
				7.5	+25	128	188	–	135	188	–	mV	
				10	+25	–	–	–	–	220	–	mV	
Amplitude-Modulation Rejection	AMR	15	4.5	7.5	+25	–	50	–	–	50	–	dB	–
Discriminator Output Resistance	$R_0(disc)$	–	4.5	7.5	+25	–	60	–	–	60	–	Ω	–
Total Harmonic Distortion	THD	14	4.5	7.5	+25	–	1.8	–	–	1.8	–	%	12

* Total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

VOLTAGE-GAIN TEST SETUP



PROCEDURE:

1) Set input frequency at desired value, $v_i = 100\ \mu V$ rms.
2) Record v_0.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_0/v_i$.
4) Repeat Steps 1, 2, and 3 for each frequency and/or temperature desired.

Fig. 4

VOLTAGE GAIN vs. FREQUENCY

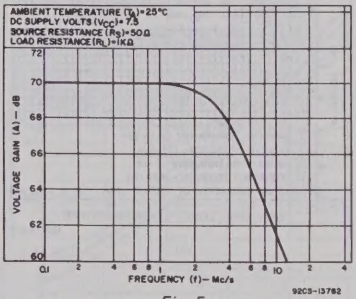


Fig. 5

INPUT-IMPEDANCE COMPONENTS TEST SETUP

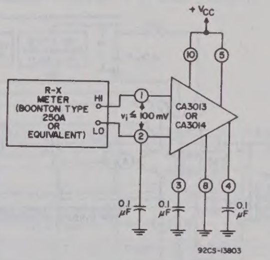


Fig. 6

INPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

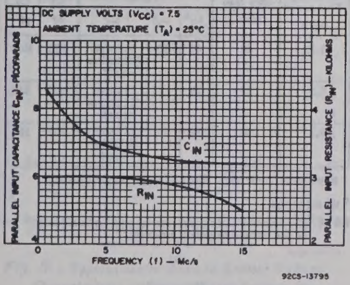


Fig. 7

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

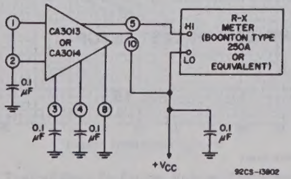


Fig. 8

OUTPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

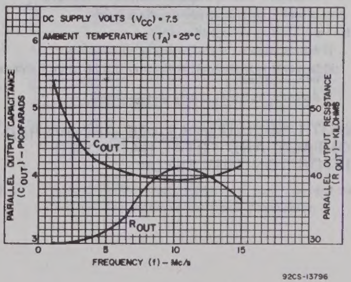
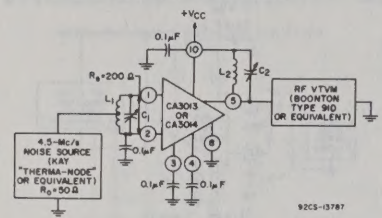


Fig. 9

NOISE FIGURE TEST SETUP


+Vcc
0.1μF
R_s=200 Ω
L_1
C_1
L_2
C_2
CA3013 OR CA3014
RF VTVM (BOONTON TYPE 910 OR EQUIVALENT)
4.5-Mc/s NOISE SOURCE (KAY "THERMA-NODE" OR EQUIVALENT) R_o=50 Ω
0.1μF
92CS-13787

L_1 = 82 μH, center-tapped

L_2 = 2.36 μH

C_1, C_2 = Arco Type 423 padder, or equivalent

Fig. 10

NOISE FIGURE vs. DC SUPPLY VOLTAGE

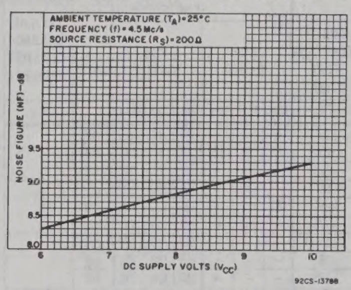


Fig. 11

TOTAL HARMONIC DISTORTION vs. DC SUPPLY VOLTAGE

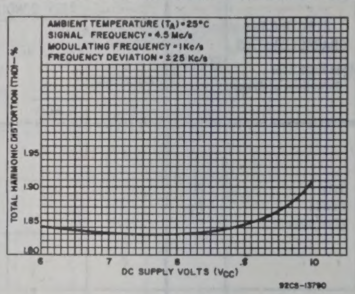


Fig. 12

INPUT LIMITING VOLTAGE (KNEE) AND RECOVERED AF VOLTAGE

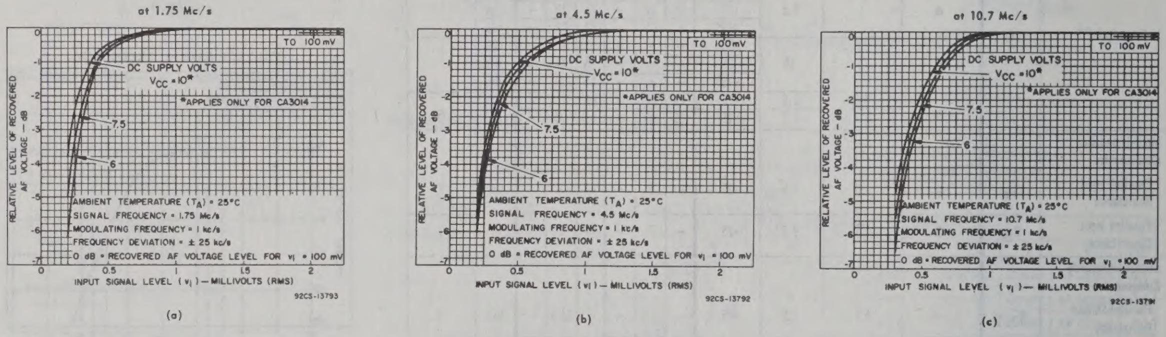
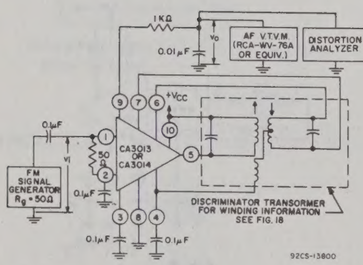


Fig. 13


1 KΩ
0.01μF
v_o
AF V.T.V.M. (RCA-WV-76A OR EQUIV.)
DISTORTION ANALYZER
+Vcc
0.1μF
FM SIGNAL GENERATOR R_g=50Ω
v_i
50 Ω
CA3013 OR CA3014
DISCRIMINATOR TRANSORMER FOR WINDING INFORMATION SEE FIG.18
0.1μF
92CS-13800

PROCEDURE:

A - Recovered-AF Voltage Output:

1) Set input frequency = 4.5 Mc/s, v_i = 100 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.

2) Record v_o as Recovered-AF Voltage Output.

B - Input Limiting Voltage (Knee):

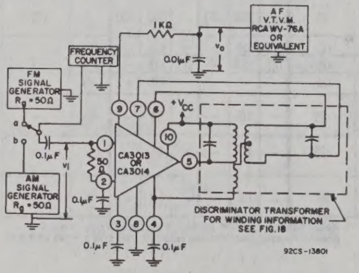
1) Repeat Steps A1 and A2, using v_i = 100 mV rms.

2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.

3) Record v_i as Input Limiting Voltage (Knee).

INPUT LIMITING VOLTAGE, RECOVERED AF VOLTAGE, AND TOTAL HARMONIC DISTORTION TEST SETUP

Fig. 14


AF V.T.V.M. RCA WV-76A OR EQUIVALENT
1 KΩ
0.01μF
v_o
FREQUENCY COUNTER
FM SIGNAL GENERATOR R_g=50Ω
AM SIGNAL GENERATOR R_g=50Ω
a
b
S
+Vcc
0.1μF
v_i
50 Ω
CA3013 OR CA3014
DISCRIMINATOR TRANSFORMER FOR WINDING INFORMATION SEE FIG.18
0.1μF
92CS-13801

PROCEDURE:

1) With Switch S in position "a", set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.

2) Record v_o.

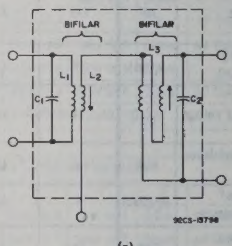
3) Place Switch S in position "b", and set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, % modulation = 50.

4) Measure v_o, and record value in dB below value in Step 2 as AM Rejection.

AM-REJECTION TEST SETUP

Fig. 15

DISCRIMINATOR TRANSFORMER SCHEMATIC



(a)

CONSTRUCTION DETAILS OF DISCRIMINATOR TRANSFORMERS SHOWN IN FIGS. 2, 14 AND 15

Coil-Form Outside Diameter = 7/32 inch

Slugs: Radio Industries, Inc. Type "E" Material, or equivalent

Wire Type: "GRIPEZE"*, or equivalent

Operating Frequency Mc/s	Wire Size (AWG #)	Turns			C_1 pF	C_2 pF
		L_1▲	L_2▲	L_3		
1.75	40	44	20	44 total (22 bifilar wound)	820	820
4.5	36	18	7	22 total (11 bifilar wound)	560	330
10.7	36	18	18	18 total (9 bifilar wound)	100	100

* Registered Trade Mark, Phelps-Dodge Copper Products.

▲ wound bifilar.

NOTE: The mutual coupling between L_1 and L_3 is adjusted for the desired degree of linearity.

(b)

Fig. 16

CA3018, CA3018A

General-Purpose Transistor Arrays

TWO ISOLATED TRANSISTORS AND A DARLINGTON-CONNECTED TRANSISTOR PAIR

For Low-Power Applications at Frequencies from DC Through the VHF Range

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

APPLICATIONS

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array" for suggested Applications.

FEATURES

- Matched monolithic general purpose transistors
- H_{FE} matched ± 10%
- V_{BE} matched ± 2 mV CA3018A (± 5mV CA3018)
- Operation from DC to 120 MHz
- Wide operating current range
- CA3018A performance characteristics controlled from 10μ A to 10mA
- Low noise figure - - 3.2 dB typical at 1KHz
- Full military temperature range capability (-55 to + 125°C)
- The CA3018 is available in a sealed-junction Beam Lead version (CA3018L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".
- Supplied in the hermetic 12-lead TO-5 style package.

Maximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	450	450	mW
Derate at 5 mW/°C for T_A > 85°C			
Temperature Range:			
Operating	-55 to + 125	-55 to + 125	°C
Storage.	-65 to + 150	-65 to + 150	°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO} ·	15	15	V
Collector-to-Base Voltage, V_{CBO} · ·	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO} · · ·	5	5	V
Collector Current, I_C	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

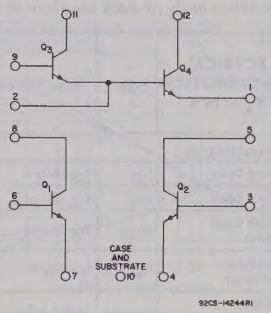


Fig. 1 - Schematic Diagram for CA3018 and CA3018A

STATIC CHARACTERISTICS

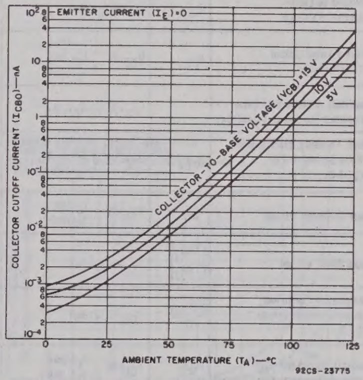


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

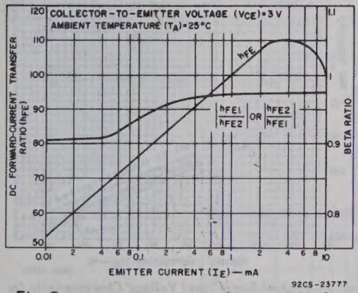


Fig. 3 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q, and Q_2 vs Emitter Current.

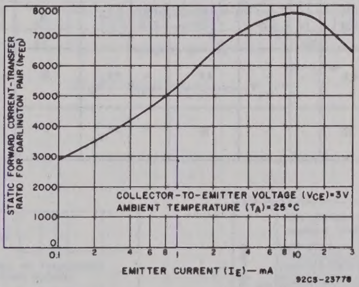


Fig. 4 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transistors Q_3 and Q_4 vs Emitter Current.

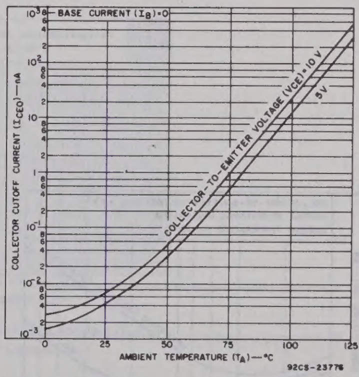


Fig. 7 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

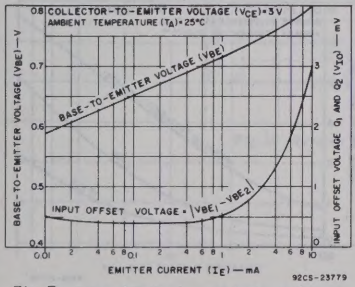


Fig. 5 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q_1 and Q_2 vs Emitter Current.

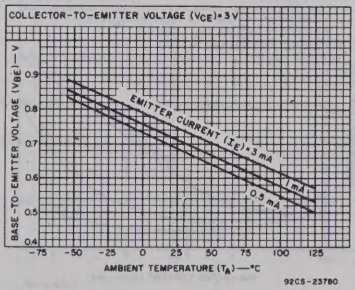


Fig. 6 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

CA3018, CA3018A

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

ELECTRICAL CHARACTERISTICS at T_A = 25°C	SYMBOLS	SPECIAL TEST CONDITIONS	CA3018 LIMITS			CA3018A LIMITS			Units	CHARAC-TERISTICS CURVES
			Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS										
Collector-Cutoff Current	I_{CBO}	V_{CB}=10V, I_E=0	–	0.002	100	–	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE}=10V, I_B=0	–	See Curve	5	–	See Curve	0.5	μA	7
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE}=10V, I_B=0	–	–	–	–	–	5	μA	–
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	15	24	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0	20	60	–	30	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0	5	7	–	5	7	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_{CI}=0	20	60	–	40	60	–	V	–
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B=1mA, I_C=10mA	–	0.23	–	–	0.23	0.5	V	–
Static Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V, I_C=10mA I_C= 1mA I_C=10μA	– 30 –	100 100 54	– 200 –	50 60 30	100 100 54	– 200 –	– – –	3
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE}=3V, I_{C1}=I_{C2}=1mA	0.9	0.97	–	0.9	0.97	–	–	3
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE}=3V I_C= 1mA I_C=100μA	1500 –	5400 –	– –	2000 1000	5400 2800	– –	–	4
Base-to-Emitter Voltage	V_{BE}	V_{CE}=3V I_E=1mA I_E=10mA	– –	0.715 0.800	– –	0.600 –	0.715 0.800	0.800 0.900	V	5
Input Offset Voltage	$\left\|V_{BE_1} - V_{BE_2}\right\|$	V_{CE}=3V, I_E=1mA	–	0.48	5	–	0.48	2	mV	5,8
Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	$\frac{\left\|\Delta V_{BE}\right\|}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	1.9	–	–	1.9	–	mV/°C	6
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} (V_{9-1})	V_{CE}=3V I_E=10mA I_E= 1mA	– –	1.46 1.32	– –	– 1.10	1.46 1.32	1.60 1.50	V	9
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3, Q_4	$\frac{\left\|\Delta V_{BED}\right\|}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	4.4	–	–	4.4	–	mV/°C	10
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\left\|V_{BE_1} - V_{BE_2}\right\|}{\Delta T}$	V_{CC}=+6V, V_{EE}=-6V, I_{C1}=I_{C2}=1mA	–	10	–	–	10	–	μV/°C	–

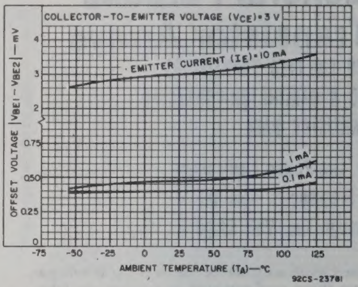


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

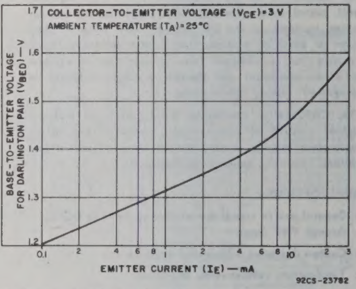


Fig.9 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Emitter Current

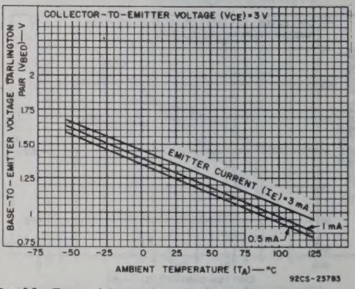


Fig.10 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Ambient Temperature.

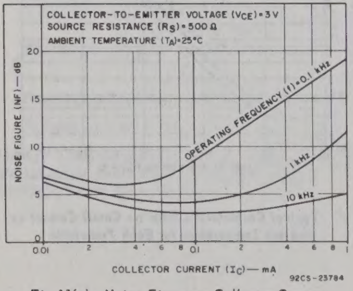


Fig.11(a) - Noise Figure vs Collector Current, R_S = 500 Ω.

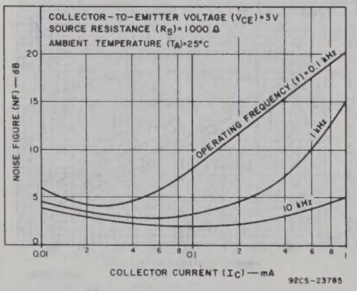


Fig.11(b) - Noise Figure vs Collector Current, R_S = 1 KΩ.

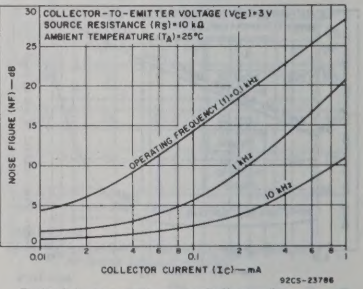


Fig.11(c) - Noise Figure vs Collector Current, R_S = 10 KΩ.

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS			CA3018			CA3018A				
Low Frequency Noise Figure	NF	f=1 KHz, V_{CE}=3V, I_C=100μA Source resistance=1 KΩ	–	3.25	–	–	3.25	–	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	–	110	–	–	110	–	–	12
Short-Circuit Input Impedance	h_{ie}		–	3.5	–	–	3.5	–	KΩ	12
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	1.8×10^{-4}	–	–	1.8×10^{-4}	–	–	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	–	31-j1.5	–	–	31-j1.5	–	mmho	13
Input Admittance	Y_{ie}		–	0.3+j0.04	–	–	0.3+j0.04	–	mmho	14
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA	300	500	–	300	500	–	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	–	0.6	–	–	0.6	–	pF	–
Collector-to-Base Capacitance	C_{CB}	V_{CB}=3V, I_C=0	–	0.58	–	–	0.58	–	pF	–
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	–	2.8	–	–	2.8	–	pF	–

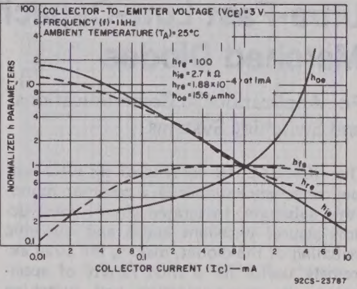


Fig.12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

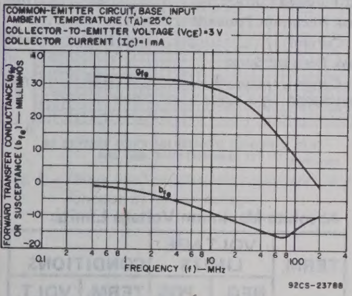


Fig.13 - Forward Transfer Admittance (Y_{fe})

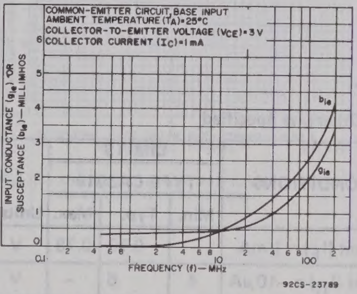


Fig.14 - Input Admittance (Y_{ie})

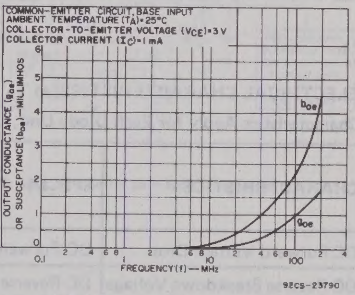


Fig.15 - Output Admittance (Y_{oe})

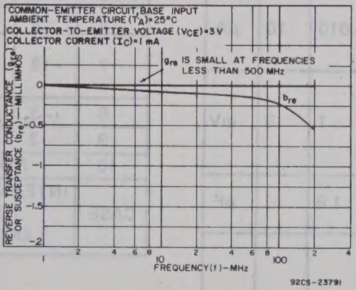


Fig.16 - Reverse Transfer Admittance (Y_{re})

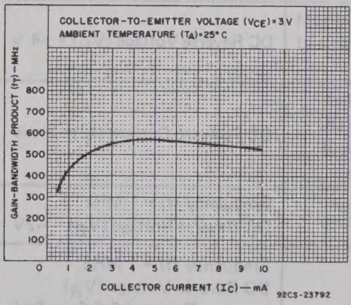


Fig.17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

CA3019

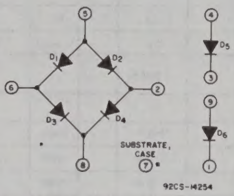
Ultra-Fast Low-Capacitance Matched Diodes

For Applications in Communications and Switching Systems

The RCA-CA3019 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Four of the diodes are internally connected as a "quad" and two are independently accessible. The substrate is internally connected to the 10-lead TO-5-style case.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.



*Connect to most negative circuit potential.

Fig. 1 — Schematic Diagram.

Features:

- Excellent Diode Match
- Low Leakage Current
- Low Pedestal Voltage when Gating
- Companion Application Note, ICAN-5299: "Application of the RCA-CA3019 Integrated-Circuit Diode Array"

Applications:

- Modulator
- Mixer
- Balanced Modulator
- Analog Switch
- Diode Gate for Chopper-Modulator Applications

Absolute-Maximum Ratings:

DISSIPATION:		
Any one diode unit . . .	20 max.	mW
Total for device	120 max.	mW
TEMPERATURE RANGE:		
Storage	−65 to +200	°C
Operating	−55 to +125	°C
DC Forward Current, I_F . .	25	mA
Peak Recurrent Forward Current, I_f	100	mA
Peak Forward Surge Current, I_f (surge) . . .	100	mA
VOLTAGE: See Table		

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics Apply for Each Diode Unit, Unless Otherwise Specified

CHARACTERISTICS	SPECIAL TEST CONDITIONS	LIMITS TYPE CA3019 Min.	 Typ.	 Max.	Units
DC Forward Voltage Drop	DC Forward Current (I_F) = 1 mA	—	0.73	0.78	V
DC Reverse Breakdown Voltage	DC Reverse Current (I_R) = −10 μA	4	6	—	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	DC Reverse Current (I_R) = −10 μA	25	80	—	V
DC Reverse (Leakage) Current	DC Reverse Voltage (V_R) = −4 V	—	0.0055	10	μA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	DC Reverse Voltage (V_R) = −4 V	—	0.010	10	μA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	DC Forward Current (I_F) = 1 mA	—	1	5	mV
Single Diode Capacitance	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) = −2V	—	1.8	—	pF
Diode Quad-to-Substrate Capacitance	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) between Terminal 2,5,6, or 8 of Diode Quad and Terminal 7 (Substrate) = −2 V				
	Terminal 2 or 6 to Terminal 7	—	4.4	—	pF
	Terminal 5 or 8 to Terminal 7	—	2.7	—	pF
Series Gate Switching Pedestal Voltage		—	10	—	mV

Absolute-Maximum Voltage Limits:

TERM.	VOLTAGE LIMITS NEG.	 POS.	CONDITIONS TERM.	 VOLT.
1	−3	+12	7	−6
2	−3	+12	7	−6
3	−3	+12	7	−6
4	−3	+12	7	−6
5	−3	+12	7	−6
6	−3	+12	7	−6
7	−18	0	1,2, 3,6, 8	0
8	−3	+12	7	−6
9	−3	+12	7	−6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 DO NOT GROUND			

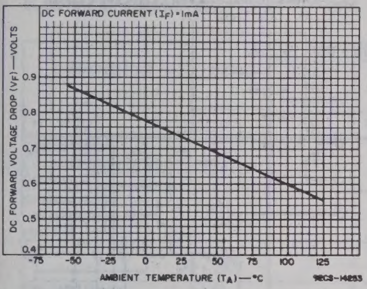


Fig. 2 — DC forward voltage drop (any diode) as a function of temperature.

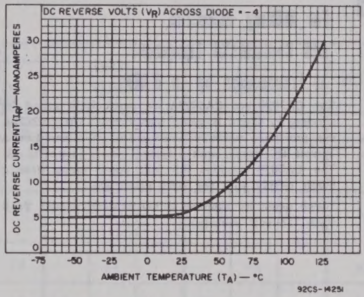


Fig. 3 — Reverse (leakage) current (any diode) as a function of temperature.

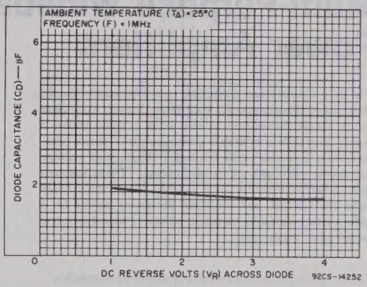


Fig. 4 — Diode capacitance (any diode) as a function of reverse voltage.

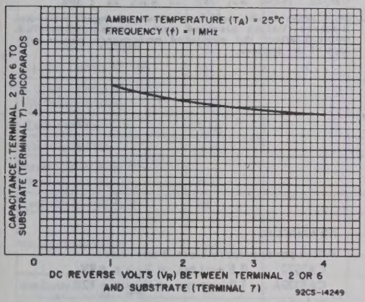


Fig. 5 — Diode quad-to-substrate capacitance as a function of reverse voltage.

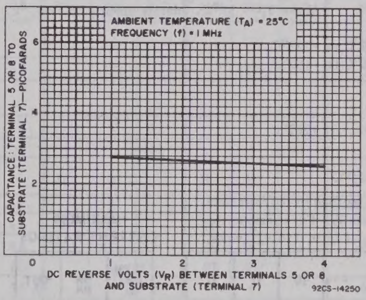


Fig. 6 — Diode quad-to-substrate capacitance as a function of reverse voltage.

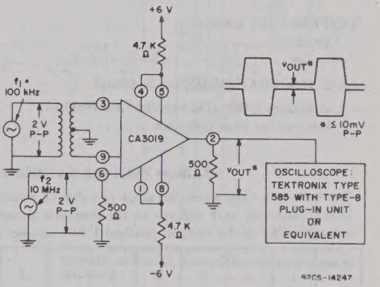


Fig. 7 — Series gate switching test setup.

CA3020, CA3020A
Multi-Purpose Wideband Power Amplifiers

For, Military, Industrial, and Commercial Equipment at Frequencies up to 8 MHz

The RCA-CA3020 and CA3020A are Integrated-Circuit, Multistage, Multipurpose, Wide-Band Power Amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct-coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as Class B power amplifiers. The CA3020A can provide a maximum power output of 1 watt from a 12-volt DC supply with a typical power gain of 75 dB. The CA3020 provides 0.5 watt power output from a 9-volt supply with the same power gain.

These types are supplied in hermetically sealed, TO-5 style 12-lead packages.

SCHEMATIC DIAGRAM FOR CA3020 AND CA3020A

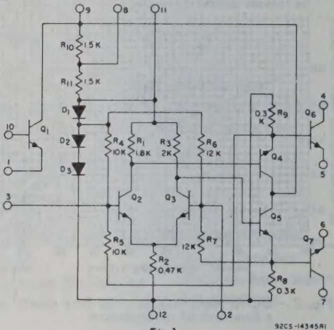


Fig.1

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:

WITHOUT HEAT SINK		WITH HEAT SINK	
At T_A = 25°C	1 W	At T_C = 25°C	2 W
Above T_A = 25°C	derate linearly 6.7 mW/°C	At T_C = 25°C to T_C = 55°C	2 W
		Above T_C = 55°C	derate linearly 16.7 mW/°C

TEMPERATURE RANGE:

Operating	-55°C to +125°C
Storage	-65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	▲ 0 -10/-12	+3 Note 1	*	+10 0
2			*	*	*	*	*	*	*	*	*	+2 -2
3				*	*	*	*	*	*	*	*	+2 -2
4					▲ +18/+25 0	*	*	*	*	*	*	▲ +18/+25 0
5						*	*	*	*	*	*	+3 Note 2
6							▲ 0 -18/-25	*	*	*	*	+3 Note 2
7								*	*	*	*	▲ +18/+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+10/+12 0
10											*	+10 0
11												*
12												REF. SUB-STRATE

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ Higher value is for CA3020A.

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	20
2	-	-
3	-	-
4	300	-
5	-	300
6	-	300
7	300	-
8	-	-
9	20	-
10	1	-
11	20	-
12	-	-

FEATURES

- **High power output - class B amplifier --**
  CA3020 .... 0.5 watt typ. at V_{CC} = +9V
  CA3020A ... 1.0 watt typ. at V_{CC} = + 12V
- **Wide frequency range --**
  Up to 8 MHZ with resistive loads
- **High power gain .... 75db typ.**
- **Single power supply for class B operation with transformer --**
  CA3020 .... 3 to 9V
  CA3020A ....3 to 12V
- **Built-in temperature-tracking voltage regulator provides stable operation over -55°C to +125°C temperature range**

APPLICATIONS

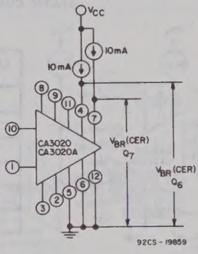
- **AF power amplifiers for portable and fixed sound and communications systems**
- **Servo-control amplifiers**
- **Wide-band linear mixers**
- **Video power amplifiers**
- **Transmission-line driver amplifiers (balanced and unbalanced)**
- **Fan-in and fan-out amplifiers for computer logic circuits**
- **Lamp-control amplifiers**
- **Motor-control amplifiers**
- **Power multivibrator**
- **Power switches**
- **Companion Application Note, ICAN 5766 "Application of CA3020 and CA3020A Integrated Circuit Multi-purpose Wide-Band Power Amplifiers".**

ELECTRICAL CHARACTERISTICS AT $T_A = 25°C$

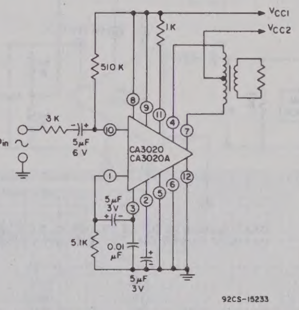
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS CA3020			LIMITS CA3020A			UNITS
		CIRCUIT AND PROCEDURE	DC SUPPLY VOLTAGE								
		FIG.	V_{CC1}	V_{CC2}	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CER}$	2_a	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 & Q_7	I_4 IDLE I_7 IDLE	4	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	4	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 & Q_7	I_4 CUTOFF I_7 CUTOFF	4	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differetial Amplifier Current Drain	I_{CC1}	4	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	4	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	4	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	4	9.0	2.0	-	2.35	-	-	2.35	-	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA
Emitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	
Collector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3 dB Point	BW		6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output	$P_{O(MAX)}$	6	6.0	6.0	200	300^a	-	200	300^a	-	mW
			9.0	9.0	400	550^a	-	400	550^a	-	
			9.0	12.0	-	-	-	800	1000^b	-	
Sensitivity for P_{OUT} = 400 mW	e_{IN}	6	9.0	9.0	-	35^a	55	-	-	-	mV
Sensitivity for P_{OUT} = 800 mW	e_{IN}	6	9.0	12.0	-	-	-	-	50^b	100	mV
Input Resistance---- Terminal 3 to Ground	R_{IN3}	9	6.0	6.0	-	1000	-	-	1000	-	Ω
Junction-to-Case Thermal Resistance	θ_{J-C}	-	-	-	-	-	60	-	-	60	°C/W

a R_{CC} = 130 Ω

b R_{CC} = 200 Ω



a. Collector-to-emitter breakdown voltage (Q_6 & Q_7) circuit



b. Typical audio amplifier circuit utilizing the CA3020 or CA3020A as an audio preamplifier and class B power amplifier

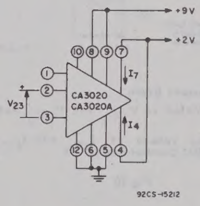
Fig.2

TYPICAL PERFORMANCE DATA

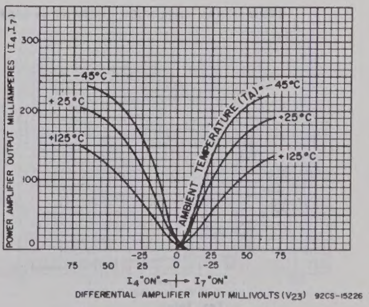
An External Radiator is Recommended for High Ambient Temperature Operation

CHARACTERISTICS		SYMBOLS	CA3020	CA3020A	UNITS
Power Supply Voltage		V_{CC_1}	9.0	9.0	V
		V_{CC_2}	9.0	12.0	
Zero Signal Current	Diff. Ampl.	I_{CC_1}	15	15	mA
	Output Ampl.	I_{CC_2}	24	24	
Maximum Signal Current	Diff. Ampl.	I_{CC_1}	16	16.6	mA
	Output Ampl.	I_{CC_2}	125	140	
Maximum Power Output at THD = 10%		Po	550	1000	mW
Sensitivity		e_{IN}	35	45	mV
Power Gain		G_P	75	75	dB
Input Resistance		R_{IN}	55	55	kΩ
Efficiency		η	45	55	%
Signal-to-Noise Ratio		S/N	70	66	dB
THD at 150 mW level			3.1	3.3	%
Test Signal Frequency from 600Ω Generator			1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance		R_{CC}	130	200	Ω

TYPICAL TRANSFER CHARACTERISTICS



a. Test Setup

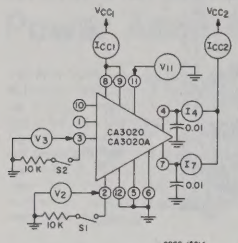


b. Characteristics with R_{10} shorted out

Fig.3

CA3020, CA3020A

STATIC CURRENT AND VOLTAGE TEST CIRCUIT

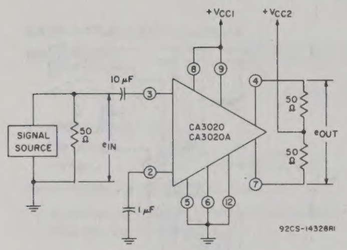


CURRENTS OR VOLTAGES	S1	S2
I_{4-IDLE}	open	open
I_{7-IDLE}	open	open
I_{4-PEAK}	open	close
I_{7-PEAK}	close	open
$I_{4-CUTOFF}$	close	open
$I_{7-CUTOFF}$	open	close

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	open	open
I_{CC2}	open	open
V_2	open	open
V_3	open	open
V_{11}	open	open

Fig.4

MEASUREMENT OF BANDWIDTH AT -3 dB POINTS

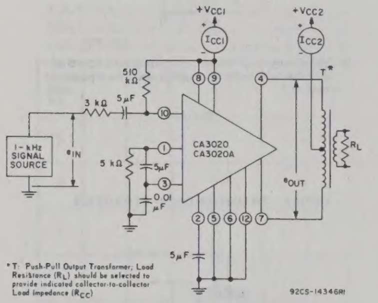


PROCEDURES:

1. Apply desired value of V_{CC_1} and V_{CC_2}
2. Apply 1 kHz input signal and adjust for e_{IN} = 5 mV (rms)
3. Record the resulting value of e_{OUT} in dB (reference value)
4. Vary input-signal frequency, keeping e_{IN} constant at 5 mV, and record frequencies above and below 1 kHz at which e_{OUT} decreases 3 dB below reference value.
5. Record bandwidth as frequency range between -3 dB points.

Fig.5

MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN



*T: Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load impedance (R_{CC})

PROCEDURES:

Zero-Signal DC Current Drain

1. Apply desired Value of V_{CC_1} and V_{CC_2} and reduce e_{IN} to 0V
2. Record resulting values of I_{CC_1} and I_{CC_2} in mA as Zero-Signal DC Current Drain.

Fig.10

Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of V_{CC_1} and V_{CC_2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of I_{CC_1} and I_{CC_2} in mA as Maximum-Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT})
4. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100 \frac{P_{OUT}}{V_{CC_1} I_{CC_1} + V_{CC_2} I_{CC_2}}$$

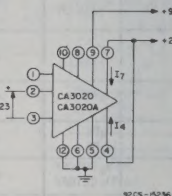
where P_{OUT} is in watts, V_{CC_1} and V_{CC_2} are in volts, and I_{CC_1} and I_{CC_2} are in amperes.

5. Record value of e_{IN} in mV (rms) required in Step 1 as Sensitivity (e_{IN})
6. Calculate Transducer Power Gain (G_p) in dB as follows:

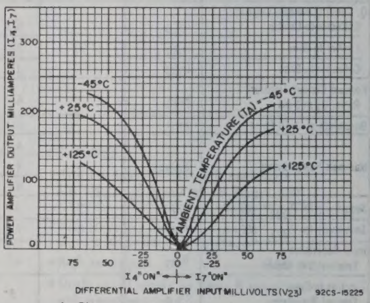
$$G_p = 10 \log_{10} \frac{P_{OUT}}{P_{IN}}$$

where P_{IN} (in mW) $= \dfrac{e_{IN}^2}{3000 + R_{IN(10)}}$

Fig.6



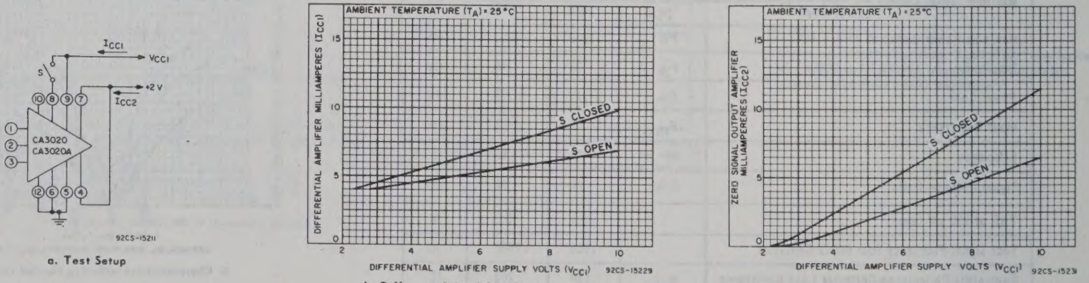
a. Test Setup



b. Characteristics with R_{10} in circuit

Fig.7

ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE



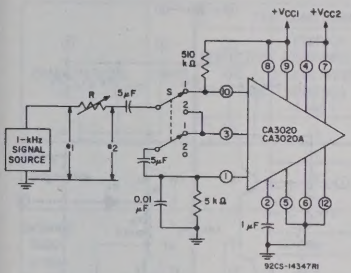
a. Test Setup

b. Differential Amplifier Characteristics

c. Output Amplifier Characteristics

Fig.8

MEASUREMENT OF INPUT RESISTANCE



PROCEDURES:

Input Resistance Terminal 10 to Ground ($R_{IN_{10}}$)

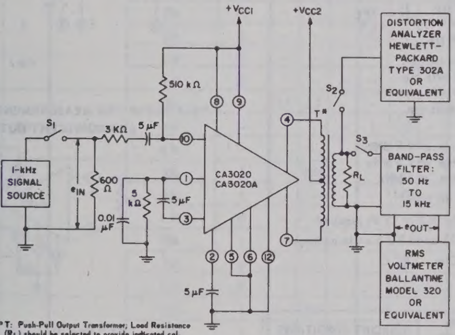
1. Apply desired value of V_{CC_1} and V_{CC_2} and set S in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as $R_{IN_{10}}$

Input Resistance Terminal 3 to Ground (R_{IN_3})

1. Apply desired value of V_{CC_1} and V_{CC_2} set S in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN_3}

Fig.9

MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION


+VCC1
+VCC2
S1
3 KΩ
5 μF
510 kΩ
⑧ ⑨
⑩
①
③
④
⑦
② ⑤ ⑥ ⑫
1-kHz SIGNAL SOURCE
eIN
600 Ω
5 kΩ
5μF
0.01 μF
5 μF
CA3020 CA3020A
T*
S2
S3
RL
DISTORTION ANALYZER HEWLETT-PACKARD TYPE 302A OR EQUIVALENT
BAND-PASS FILTER: 50 Hz TO 15 kHz
eOUT
RMS VOLTMETER BALLANTINE MODEL 320 OR EQUIVALENT
92CM-14329RI

*T: Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load Impedance (R_{CC})

PROCEDURES:

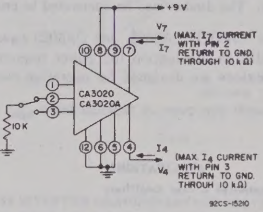
Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as $e_{OUT\,1}$ (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT_2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10}\dfrac{e_{OUT_1}}{e_{OUT_2}}$.

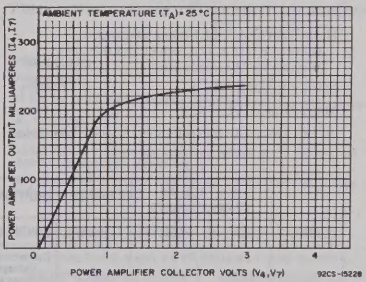
Total Harmonic Distortion

1. Close S_1 and S_2; open S_3
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

Fig.10


+9 V
V7
I7
(MAX. I7 CURRENT WITH PIN 2 RETURN TO GND. THROUGH 10 kΩ)
⑩ ⑧ ⑨ ⑦
①
②
③
⑫ ⑥ ⑤ ④
10 K
CA3020 CA3020A
I4
V4
(MAX. I4 CURRENT WITH PIN 3 RETURN TO GND. THROUH 10 kΩ)
92CS-15210

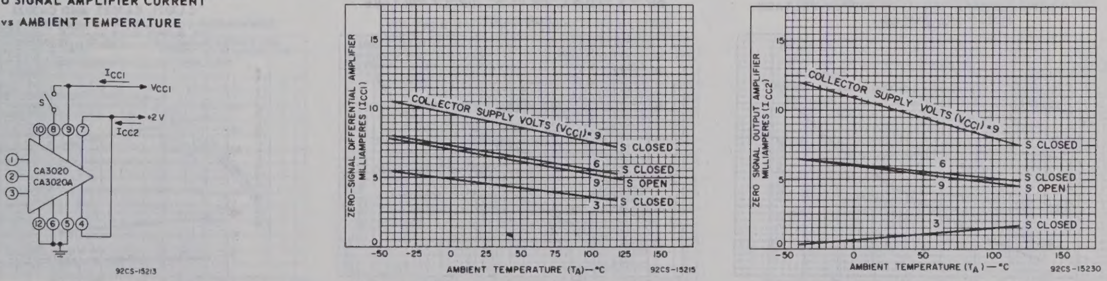
a. Test Setup



b. Characteristic

Fig.11

ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE



a. Test Setup

b. Differential Amplifier Characteristics

c. Output Amplifier Characteristics

Fig.12

CA3021, CA2022, CA2023

Low-Power Video and Wideband Amplifiers

RCA-CA3021, CA3022, and CA3023 are low-power integrated-circuit wideband amplifiers with a wide range of applications in industrial, military, and commercial communications equipment. Each consists of a multistage amplifier circuit and unconnected diodes on a single chip, hermetically sealed in a 12-lead TO-5 style package. The diodes may be connected to provide limiting in FM applications.

The CA3021, CA3022, and CA3023 have the same maximum ratings, and differ principally in dissipation (dc power requirements) and bandwidth capability. All three devices are designed for operation over the temperature range from -55° C to +125° C.

APPLICATIONS

- **Gain-Controlled Linear Amplifiers**
- **AM/FM IF Amplifiers** • **Video Amplifiers** • **Limiters**

HIGHLIGHTS

- **Low DC Power Drain:**

$$P_D \begin{cases} \text{CA3021} = 4 \text{ mW typ.} \\ \text{CA3022} = 12.5 \text{ mW typ.} \\ \text{CA3023} = 35 \text{ mW typ.} \end{cases} \text{at } V_{CC} = 6 \text{ V}$$

- **Excellent frequency response:**

$$\text{-3 dB BW} \begin{cases} \text{CA3021} = 2.4 \text{ MHz typ.} \\ \text{CA3022} = 7.5 \text{ MHz typ.} \\ \text{CA3023} = 16 \text{ MHz typ.} \end{cases}$$

- **High Voltage Gain:**

$$A \begin{cases} \text{CA3021} = 56 \text{ dB typ. at } 0.5 \text{ MHz} \\ \text{CA3022} = 57 \text{ dB typ. at } 2.5 \text{ MHz} \\ \text{CA3023} = 53 \text{ dB typ. at } 5 \text{ MHz} \end{cases}$$

- **Wide AGC Range: 33 dB typ.**
- **Only one power supply (4.5 to 12 V) required**
- **Hermetically Sealed 12-Lead TO-5-style package**
- **Operation from -55° C to +125° C**

SCHEMATIC DIAGRAM FOR CA3021, CA3022, AND CA3023

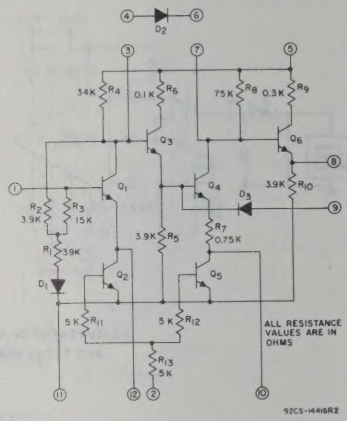


Fig.1

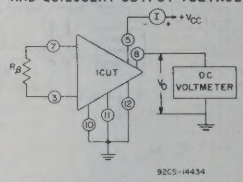
ABSOLUTE-MAXIMUM RATINGS:

OPERATING-TEMPERATURE RANGE	-55°C to +125°C	
STORAGE-TEMPERATURE RANGE	-65°C to +150°C	
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C	
DEVICE DISSIPATION, P_T	120 max.	mW
INPUT-SIGNAL VOLTAGE	-3, +3 max.	V
DC VOLTAGES AND CURRENTS	See Table Below	

	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
1	-3V	+3V	1	Connected to Voltage Source through 100Ω Resistor
			5	+12V
			10, 11, 12	Ground
2	-3V	+12V	5	+12V
			10, 11, 12	Ground
3	0V	+12V	5	+12V
			10, 11, 12	Ground
4	-12V 10 max. mA	+12V	6, 11	Ground
5	0V	+18V	10, 11, 12	Ground
6	-12V 10 max. mA	+12V	5, 11	Ground

	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
7	0V	+12V	5	+12V
			10, 11, 12	Ground
8	20 max. mA		5	+12V
			10, 11, 12	Ground
9	-0.5V	+3V	5	+12V
			10, 11, 12	Ground
10	0V	+4V	2,5	+12V
			11	Ground
11	-6V	+12V	2	Ground
			5	+12V
12	0V	+4V	2,5	+12V
			11	Ground

TEST SETUP FOR MEASUREMENT OF DEVICE DISSIPATIO AND QUIESCENT OUTPUT VOLTAGE



$P_T = V_{CC}\,(I)$

Fig.2

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3021

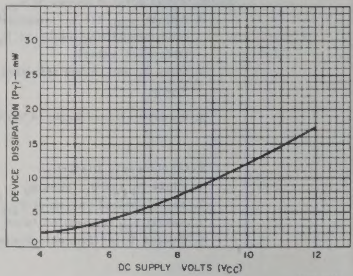


Fig.3(a)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3022

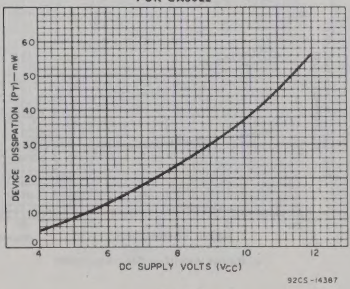


Fig.3(b)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3023

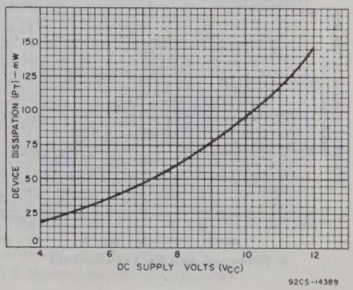


Fig.3(c)

DEVICE DISSIPATION VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

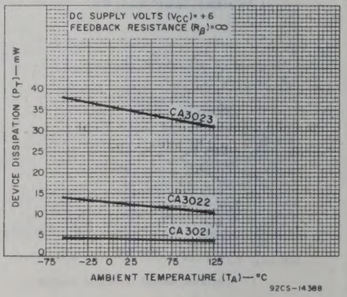
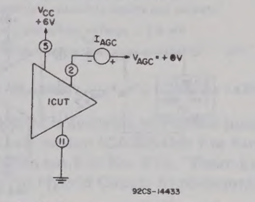


Fig.3(d)

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, V_{CC} = +6V, unless otherwise specified

CHARACTERISTIC		SYMBOL	TEST CONDITIONS			LIMITS									UNITS	TYPICAL CHARAC-TERISTIC CURVE
			TEST SETUP AND PROCEDURE	FEEDBACK RESISTANCE (R_β) BETWEEN TERMINALS 3 AND 7	FRE-QUENCY f	CA3021 (TA5219)			CA3022 (TA5236)			CA3023 (TA5218)				
			Fig.	Ω	MHz	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Fig.
Device Dissipation		P_T	2	∞	–	1	4	8	–	–	–	–	–	–	mW	3a,d
				∞	–	–	–	–	5	12.5	24	–	–	–	mW	3b,d
				∞	–	–	–	–	–	–	–	24	35	48	mW	3c,d
Quiescent Output Voltage		V_o	2	39k	–	–	2.2	–	–	–	–	–	–	–	V	–
				10k	–	–	–	–	–	1.9	–	–	–	–	V	
				4.7k	–	–	–	–	–	–	–	–	1.3	–	V	
AGC Source Current		I_{AGC}	4	V_{AGC} =+6V		–	0.8	–	–	0.8	–	–	0.8	–	mA	–
Voltage Gain		A	5	560k	0.5	50	56	–	–	–	–	–	–	–	dB	6a
				39k	0.8	40	46	–	–	–	–	–	–	–	dB	6a,d
				39k	2.5	–	–	–	50	57	–	–	–	–	dB	6b
				10k	3	–	–	–	40	44	–	–	–	–	dB	6b,d
				18k	5	–	–	–	–	–	–	50	53	–	dB	6c
				4.7k	10	–	–	–	–	–	–	40	44	–	dB	6c,d
Bandwidth at -3 dB Point		BW	5	39k	–	0.8	2.4	–	–	–	–	–	–	–	MHz	6a
				10k	–	–	–	–	3	7.5	–	–	–	–	MHz	6b
				4.7k	–	–	–	–	–	–	–	10	16	–	MHz	6c
Input-Impedance Compo-nents	Input Resistance	R_{IN}	7	39k	1	–	4000	–	–	–	–	–	–	–	Ω	–
				10k	5	–	–	–	–	1300	–	–	–	–	Ω	
				4.7k	10	–	–	–	–	–	–	–	300	–	Ω	
	Input Capaci-tance	C_{IN}	7	39k	1	–	11	–	–	–	–	–	–	–	pF	–
				10k	5	–	–	–	–	18	–	–	–	–	pF	
				4.7k	10	–	–	–	–	–	–	–	13	–	pF	
Output Resistance		R_{OUT}	8	39k	1	–	300	–	–	–	–	–	–	–	Ω	–
				10k	5	–	–	–	–	120	–	–	–	–	Ω	
				4.7k	10	–	–	–	–	–	–	–	100	–	Ω	
Noise Figure		NF	9	39k	1	–	4.2	8.5	–	–	–	–	–	–	dB	–
				10k	1	–	–	–	–	4.4	8.5	–	–	–	dB	
				4.7k	1	–	–	–	–	–	–	–	6.5	8.5	dB	
AGC Range		AGC	10	–	1	–	33	–	–	–	–	–	–	–	dB	–
				–	5	–	–	–	–	33	–	–	–	–	dB	
				–	10	–	–	–	–	–	–	–	33	–	dB	
Maximum Output Voltage (RMS Value)		v_{out}	5	39k	1	–	0.6	–	–	–	–	–	–	–	V(rms)	–
				10k	5	–	–	–	–	0.7	–	–	–	–	V(rms)	
				4.7k	10	–	–	–	–	–	–	–	0.5	–	V(rms)	

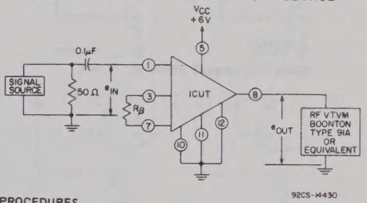
TEST SETUP FOR MEASUREMENT OF AGC SOURCE CURRENT



I_{AGC} IS THE CURRENT FLOWING INTO TERMINAL 2.

Fig.4

TEST SETUP FOR MEASUREMENTS OF VOLTAGE-GAIN, -3dB BANDWIDTH, AND MAXIMUM OUTPUT VOLTAGE



PROCEDURES

Voltage Gain:

(a) Set e_{in} = 0.5 mVat frequency specified, read e_{out} Voltage Gain (A) = $20 \, \mathrm{Log}_{10} \frac{e_{out}}{e_{in}}$

Bandwidth:

(a) Set e_{out} to a convenient reference voltage at f = 100 kHz and record corresponding value of e_{in}.

(b) Increase the frequency, keeping e_{in} constant until e_{out} drops 3-dB. Record Bandwidth.

Fig.5

VOLTAGE GAIN VS FREQUENCY FOR CA3021

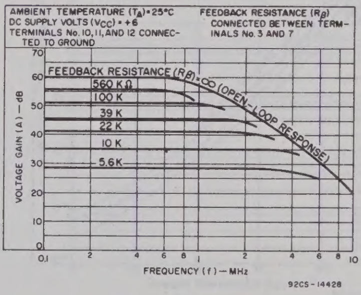


Fig.6(a)

VOLTAGE GAIN VS FREQUENCY FOR CA3022

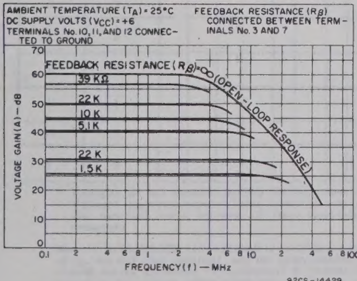


Fig.6(b)

VOLTAGE GAIN VS FREQUENCY FOR CA3023

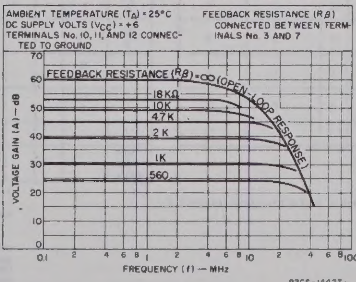


Fig.6(c)

VOLTAGE GAIN VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

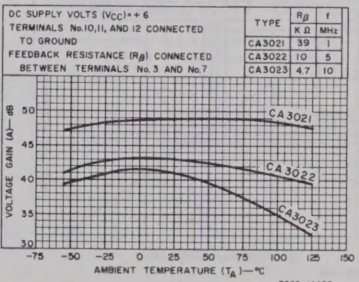
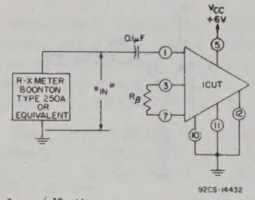


Fig.6(d)

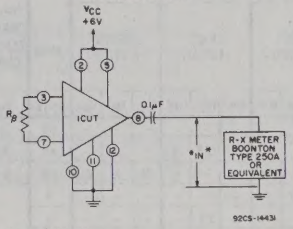
TEST SETUP FOR MEASUREMENT OF INPUT-IMPEDANCE COMPONENTS



* $e_{in} \leq$ 10 mV

Fig.7

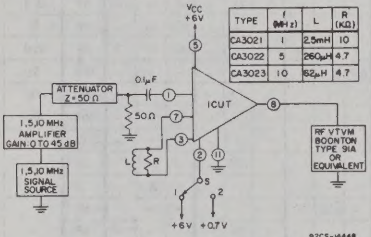
TEST SETUP FOR MEASUREMENT OF OUTPUT RESISTANCE



* $e_{in} \leq$ 10 mV

Fig.8

TEST SETUP FOR MEASUREMENT OF AGC RANGE



TYPE	f (MHz)	L	R (KΩ)
CA3021	1	2.5mH	10
CA3022	5	260μH	4.7
CA3023	10	62μH	4.7

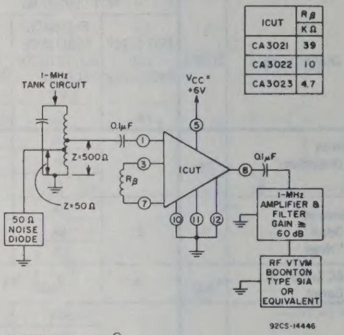
$$\text{AGC RANGE} = 20\ \text{LOG}_{10} \frac{\text{A WITH S IN POSITION 1}}{\text{A WITH S IN POSITION 2}}$$

(A = VOLTAGE GAIN)

	f
	MHz
CA3021	1
CA3022	5
CA3023	10

Fig. 10

TEST SETUP FOR MEASUREMENT OF NOISE FIGURE



ICUT	Rβ KΩ
CA3021	39
CA3022	10
CA3023	4.7

CA3021 - R_β = 39 kΩ
CA3022 - R_β = 10 kΩ
CA3023 - R_β = 4.7 kΩ

Fig.9

CA3026, CA3054

Dual Independent Differential Amplifiers

For Low-Power Applications at Frequencies from DC to 120 MHz

The CA3026 and CA3054 each consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3026 and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

APPLICATIONS

- Dual sense amplifiers
- Dual Schmitt triggers
- Multifunction combinations -- RF Mixer, Oscillator; Converter/IF
- IF amplifiers (differential and or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Pairs of balanced mixers
- Synthesizer mixers
- Balanced (push-pull) cascode amplifiers

FEATURES

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage -- ±5 mV
- Full military temperature range capability -- -55°C to +125°C
- Limited temperature range -- 0°C to 85°C for CA3054

- **The CA3054 is available in a sealed-junction Beam-Lead version (CA3054L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**
- **CA3026—Hermetic 12-lead TO-5 package**
- **CA3054—14-lead dual-in-line plastic package**

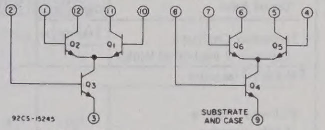


Fig.1a - Schematic Diagram for CA3026.

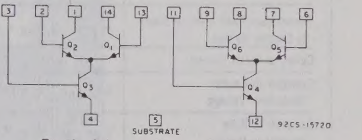


Fig.1b - Schematic Diagram for CA3054.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

Power Dissipation, P:	CA3026	CA3054	
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55$°C	Derate at 5	6.67	mW/°C
Temperature Range:			
Operating	-55 to + 125		°C
Storage	-65 to + 150		°C
Lead Temperature (During Soldering):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1† and horizontal terminal 3† is +15 to -5 volts.

† For CA3026; corresponding terminals for CA3054 are vertical terminal 2 and horizontal terminal 4.

CA3054 TERMINAL No. →		13	14	1	2	3	4	6	7	8	9	11	12	5
↓	CA3026 → TERMINAL No. ↓	10	11	12	1	2	3	4	5	6	7	8	Note 1 9	Note 1 9
13	10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*	*
14	11			*	*	*	+20 0	*	*	*	*	*	*	+20 0
1	12				+20 0	*	+20 0	*	*	*	*	*	*	+20 0
2	1					*	+15 -5	*	*	*	*	*	*	*
3	2						+1 -5	*	*	*	*	*	*	*
4	3							*	*	*	*	*	*	*
6	4								0 -20	*	+5 -5	*	+15 -5	*
7	5									*	*	*	*	+20 0
8	6										+20 0	*	*	+20 0
9	7											*	+15 -5	*
11	8												+1 -5	*
12	9													*
5	9													Ref Sub-strate

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

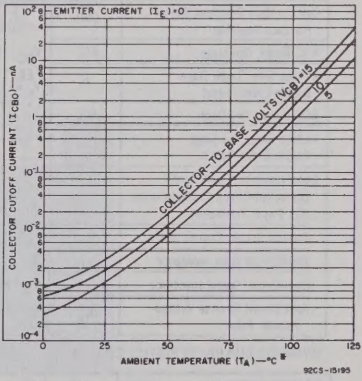
Note 1: In the CA3026 terminal No.9 is connected to the emitter of Q_4, the reference substrate, and the case; therefore, the case should not be grounded. Two terminal 9 columns (CA3026) appear in the voltage rating chart because it is a composite chart for both the CA3026 and the CA3054. Wherever an asterisk is shown in one column 9 and a rating is shown in the other column 9, the asterisk should be ignored.

Maximum Current Ratings

CA3054 TERMINAL No.●	CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
13	10	5	0.1
14	11	50	0.1
1	12	50	0.1
2	1	5	0.1
3	2	5	0.1
4	3	0.1	50
6	4	5	0.1
7	5	50	0.1
8	6	50	0.1
9	7	5	0.1
11	8	5	0.1
12	9	0.1	50

● Terminal No.10 of CA3054 is not used.

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

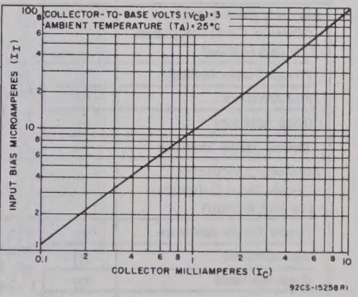


Fig.3 - Input bias current characteristic vs collector current for each transistor.

CA3026, CA3054

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT	CA3026 CA3054 LIMITS			UNITS	TYPICAL CHARACTERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS								
For Each Differential Amplifier								
Input Offset Voltage	V_{IO}	V_{CB} = 3 V	-	-	0.45	5	mV	6
Input Offset Current	I_{IO}		-	-	0.3	2	μA	7
Input Bias Current	I_I		-	-	10	24	μA	3
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$	$I_{E(Q3)} = I_{E(Q4)}$ = 2 mA	-	-	0.98 to 1.02	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$		-	-	1.1	-	μV/°C	5
For Each Transistor								
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V, I_C = 50 μA 1 mA 3 mA 10 mA	- - - -	- - - -	0.630 0.715 0.750 0.800	0.700 0.800 0.850 0.900	V	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA	-	-	-1.9	-	μV/°C	4
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	-	0.002	100	nA	2
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	-	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	-	20	60	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	-	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	-	5	7	-	V	-
DYNAMIC CHARACTERISTICS								
Common-Mode Rejection Ratio For Each Amplifier	CMR	V_{CC} = 12 V V_{EE} = -6 V V_x = -3.3 V f = 1 kHz	8a	-	100	-	dB	8b
AGC Range, One Stage	AGC		9a	-	75	-	dB	9b
Voltage Gain, Single Stage Double-Ended Output	A		9a	-	32	-	dB	9b
AGC Range, Two Stage	AGC		10a	-	105	-	dB	10b
Voltage Gain, Two Stage Double-Ended Output	A		10a	-	60	-	dB	10b
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)								
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	-	3.5	-	kΩ	11
Open-Circuit Output Impedance	h_{oe}		-	-	15.6	-	μmho	11
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	-	1.8×10^{-4}	-	-	11

DYNAMIC CHARACTERISTICS CONT'D

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	FIG.	MIN.	TYP.	MAX.	UNITS	FIG.
1/f Noise Figure (For Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V	-	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA	-	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Each Collector $I_C \approx$ 1.25 mA f = 1 MHz	-	-	-20+j0	-	mmho	13a
Input Admittance	y_{11}		-	-	0.22+j0.1	-	mmho	13b
Output Admittance	y_{22}		-	-	0.01+j0	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-	-0.003 +j0	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Total Stage $I_C \approx$ 2.5 mA f = 1 MHz	-	-	68-j0	-	mmho	14a
Input Admittance	y_{11}		-	-	0.55+j0	-	mmho	14b
Output Admittance	y_{22}		-	-	0+j0.02	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	-	0.004-j0.005	-	μmho	14d
Noise Figure	NF	f = 100 MHz	-	-	8	-	dB	-

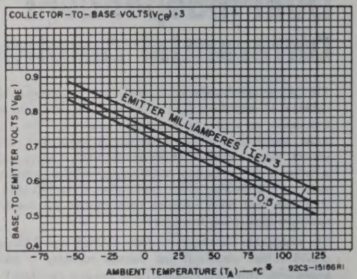


Fig.4 - Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

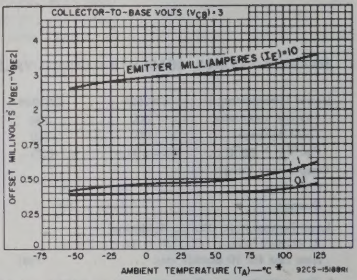


Fig.5 - Offset voltage characteristic vs ambient temperature for differential pairs.

* For CA3054: use data from 0°C to 85°C only

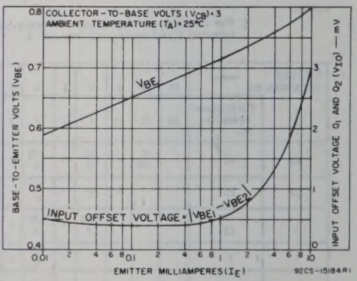


Fig.6 - Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

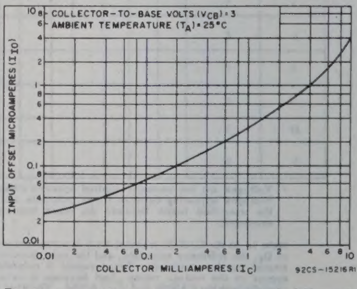
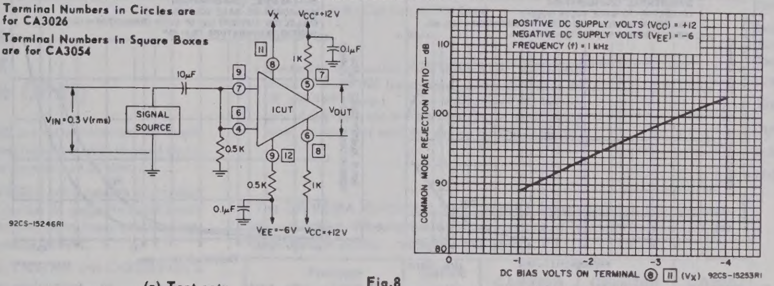


Fig.7 - Input offset current for matched differential pairs vs collector current.

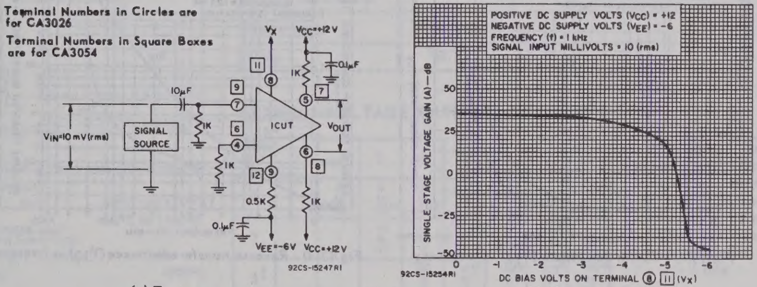
TYPICAL DYNAMIC CHARACTERISTICS

COMMON MODE REJECTION RATIO



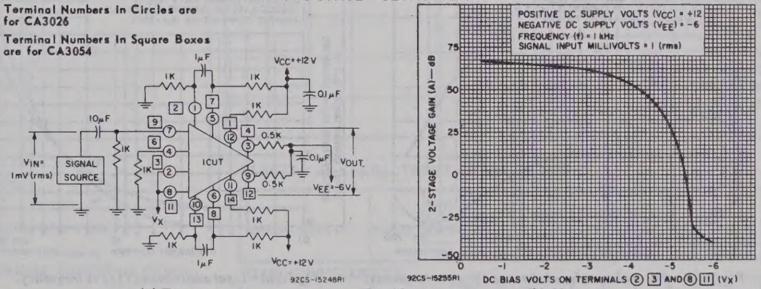
(a) Test setup **Fig.8** *(b) Characteristic*

SINGLE-STAGE VOLTAGE GAIN



(a) Test setup *Fig.9* *(b) Characteristic*

TWO-STAGE VOLTAGE GAIN



(a) Test setup *Fig.10* *(b) Characteristic*

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

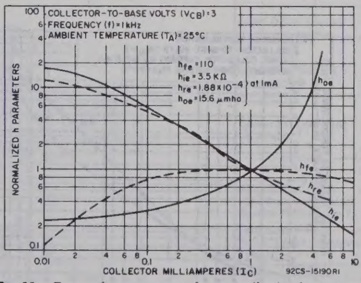


Fig.11 - Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

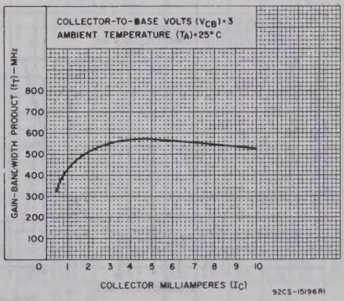


Fig.12 - Gain-bandwidth product (f_T) vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER

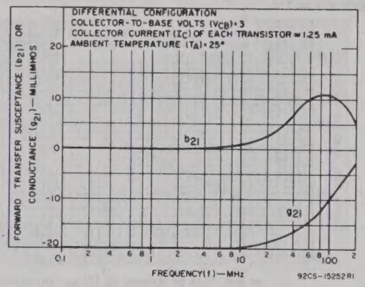


Fig.13(a) - Forward transfer admittance (Y_{21}) vs frequency.

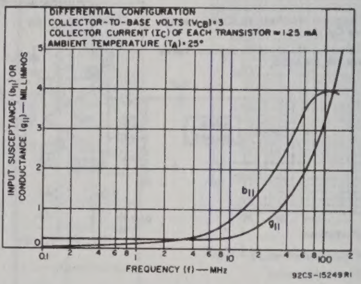


Fig.13(b) - Input admittance (Y_{11}).

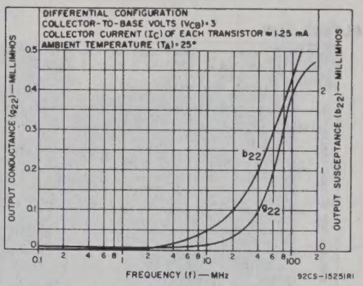


Fig.13(c) - Output admittance (Y_{22}) vs frequency.

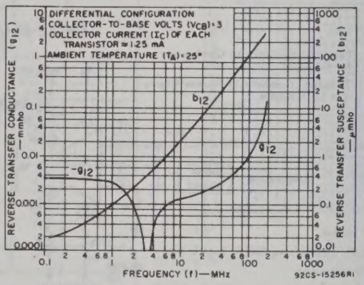


Fig.13(d) - Reverse transfer admittance (Y_{12}) vs frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

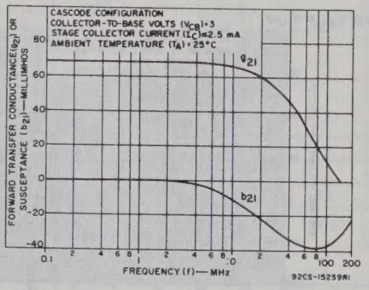


Fig.14(a) - Forward transfer admittance (Y_{21}) vs frequency.

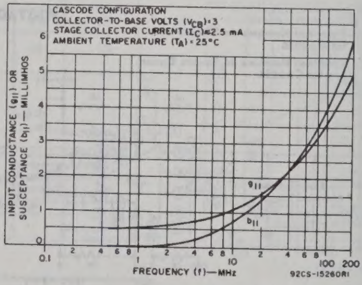


Fig.14(b) - Input admittance (Y_{11}) vs frequency.

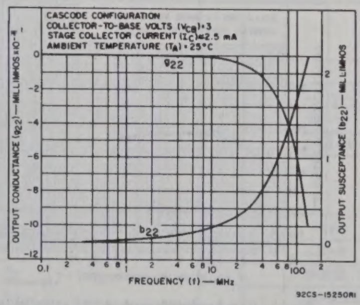


Fig.14(c) - Output admittance (Y_{22}) vs frequency.

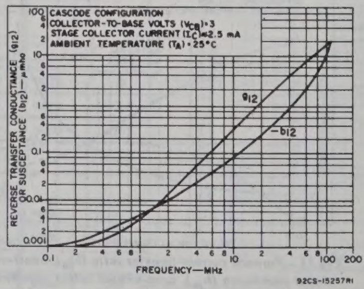


Fig.14(d) - Reverse transfer admittance (Y_{12}) vs frequency.

CA3028A, CA3028B, CA3053 Types

DIFFERENTIAL/CASCODE AMPLIFIERS

For Communications and Industrial Equipment at Frequencies from DC to 120 MHz

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical dc and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

APPLICATIONS

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio, and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator
- Mixer
- Limiter
- Companion Application Note, ICAN 5337 "Application of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.

FEATURES

- **Controlled for Input Offset Voltage, Input Offset Current, and Input Bias Current (CA3028B)**
- **Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide Unexcelled Versatility**
- **Single- and Dual-Ended Operation**
- **Operation from DC to 120 MHz**
- **Balanced-AGC Capability**
- **Wide Operating-Current Range**

The CA3028A, CA3028B, and CA3053 are available in the packages shown below. When ordering these devices, it is important to add the appropriate suffix letter to the device.

Package 8-Lead TO-5	Suffix Letter	CA3028A	CA3028B	CA3053
TO-5	T	✓	✓	✓
With Dual-In-Line Formed Leads (DIL-CAN)	S	✓	✓	✓
Beam-Lead	L	✓		
Chip	H	✓		

ABSOLUTE MAXIMUM RATINGS AT $T_A = 25^\circ C$

DISSIPATION:
At T_A up to 55°C (CA3028AF, CA3028BF, CA3053F) .... 750 mW
At $T_A > 55^\circ C$ (CA3028AF, CA3028BF, CA3053F) .... Derate linearly 6.67 mW/°C
At T_A up to 85°C (CA3028A, CA3028B, CA3053) .... 450 mW
At $T_A > 85^\circ C$ (CA3028A, CA3028B, CA3053) Derate linearly 5 mW/°C
AMBIENT-TEMPERATURE RANGE:
Operating .... −55°C to +125°C
Storage .... −65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. .... +265°C

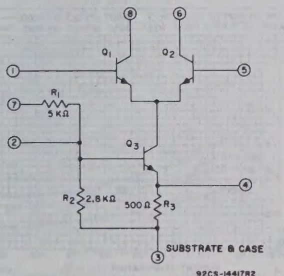
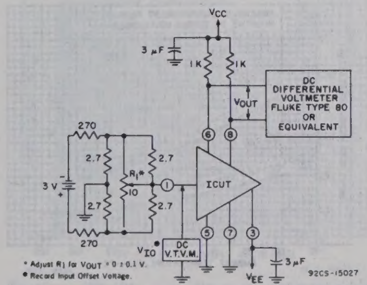


Fig.1 - Schematic diagram for CA3028A, CA3028B and CA3053.



* Adjust R1 for VOUT = 0 ± 0.1 V.
● Record Input Offset Voltage.

Fig.2 - Input offset voltage test circuit for CA3028B.

MAXIMUM VOLTAGE RATINGS at $T_A = 25^\circ C$

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15▲	0 to -15▲	0 to -15▲	+5 to -5	*	*	+20⊕ to 0
2			+5 to -11	+5 to -1	+15♦ to 0	*	+15♦ to 0	*
3‡				+10 to 0	+15♦ to 0	+30● to 0	+15♦ to 0	+30● to 0
4					+15♦ to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

▲ Limit is -12V for CA3053

⊕ Limit is +15V for CA3053

♦ Limit is +12V for CA3053

● Limit is +24V for CA3028A and +18V for CA3053

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVES
		Fig.			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS															
			$+V_{CC}$	$-V_{EE}$											
Input Offset Voltage	V_{IO}	2	6V 12V	6V 12V	- -	- -	- -	- -	0.98 0.89	5 5	- -	- -	- -	mV	4
Input Offset Current	I_{IO}	3a	6V 12V	6V 12V	- -	- -	- -	- -	0.56 1.06	5 6	- -	- -	- -	µA	4
Input Bias Current	I_I	3a	6V 12V	6V 12V	- -	16.6 36	70 106	- -	16.6 36	40 80	- -	- -	- -	µA	5a
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	29 36	85 125		5b
Quiescent Operating Current	I_6 or I_8	3a	6V 12V	6V 12V	0.8 2	1.25 3.3	2 5	1 2.5	1.25 3.3	1.5 4	- -	- -	- -	mA	6a 7
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	1.2 2.0	2.2 3.3	3.5 5.0		6b
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I_7	8a	12V 12V	V_{AGC} = +9 V_{AGC} = +12	- -	1.28 1.65	- -	- -	1.28 1.65	- -	- -	- -	- -	mA	8b
		-	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	1.15 1.55	- -		-
Input Current (Terminal No.7)	I_7	-	6V 12V	6V 12V	0.5 1	0.85 1.65	1 2.1	0.5 1	0.85 1.65	1 2.1	- -	- -	- -	mA	-
Device Dissipation	P_T	3a	6V 12V	6V 12V	24 120	36 175	54 260	24 120	36 175	42 220	- -	- -	- -	mW	9
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	50 100	80 150		-

CA3028A, CA3028B, CA3053 Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			UNITS	TYPICAL CHARACTERISTICS CURVE
			Fig.			Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
DYNAMIC CHARACTERISTICS													
Power Gain		G_P	10a	f = 100 MHz	Cascode	16	20	-	16	20	-	dB	10b
			11a,d	V_{CC} = +9V	Diff.-Ampl.	14	17	-	14	17	-		11b,e
			10a	f = 10.7 MHz	Cascode	35	39	-	35	39	-	dB	10b
			11a	V_{CC} = +9V	Diff.-Ampl.	28	32	-	28	32	-		11b
Noise Figure		NF	10a	f = 100 MHz	Cascode	-	7.2	9	-	7.2	9	dB	10c
			11a,d	V_{CC} = +9V	Diff.-Ampl.	-	6.7	9	-	6.7	9		11c,e
Input Admittance		Y_{11}	-	f = 10.7 MHz V_{CC} = +9V	Cascode				-	0.6 + j 1.6	-	mmho	12
			-		Diff.-Ampl.				-	0.5 + j 0.5	-		13
Reverse Transfer Admittance		Y_{12}	-		Cascode				-	0.0003 - j0	-	mmho	14
			-		Diff.-Ampl.				-	0.01 - j0.0002	-		15
Forward Transfer Admittance		Y_{21}	-		Cascode		←		-	99 - j18	-	mmho	16
			-		Diff.-Ampl.				-	-37 + j0.5	-		17
Output Admittance		Y_{22}	-		Cascode				-	0. + j0.08	-	mmho	18
			-		Diff.-Ampl.				-	0.04 + j0.23	-		19
Power Output (Untuned)		P_o	20a	f = 10.7 MHz	Diff.-Ampl. 50 Ω Input-Output	-	5.7	-	-	5.7	-	μW	20b
AGC Range (Max. Power Gain to Full Cutoff)		AGC	21a	V_{CC} = +9V	Diff.-Ampl.	-	62	-	-	62	-	dB	21b
Voltage Gain	at f = 10.7 MHz	A	22a	f = 10.7 MHz	Cascode	-	40	-	-	40	-	dB	22b
			22c	V_{CC} = +0V R_L = 1 kΩ	Diff.-Ampl.	-	30	-	-	30	-		22d
	Differential at f = 1 kHz		23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	35	38	42	dB	-
				V_{CC} = +12V, V_{EE} = -12V R_L = 1.6 kΩ		-	-	-	40	42.5	45		
Max. Peak-to-Peak Output Voltage at f = 1 kHz		V_o(P-P)	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	7	11.5	-	V_{P-P}	-
				V_{CC} = +12V, V_{EE} = -12V R_L = 1.6 kΩ		-	-	-	15	23	-		
Bandwidth at -3 dB point		BW	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	-	7.3	-	MHz	-
				V_{CC} = +12V, V_{EE} = -12V R_L = 1.6 kΩ		-	-	-	-	8	-		
Common-Mode Input-Voltage Range		V_{CMR}	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	-2.5	(-3.2 - 4.5)	4	V	-
				V_{CC} = +12V, V_{EE} = -12V		-	-	-	-5	(-7 - 9)	7		
Common-Mode Rejection Ratio		CMR	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	60	110	-	dB	-
				V_{CC} = +12V, V_{EE} = -12V		-	-	-	60	90	-		
Input Impedance at f = 1 kHz		Z_{IN}		V_{CC} = +6V, V_{EE} = -6V		-	-	-	-	5.5	-	kΩ	-
				V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	3	-		
Peak-to-Peak Output Current		I_{P-P}		V_{CC} = +9V	f = 10.7 MHz e_{in} = 400 mV Diff.-Ampl.	2	4	7	2.5	4	6	mA	-
				V_{CC} = +12V		3.5	6	10	4.5	6	8		

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVE
			Fig.			Min.	Typ.	Max.		Fig.
DYNAMIC CHARACTERISTICS										
Power Gain		G_P	10a	f = 10.7 MHz	Cascode	35	39	-	dB	
			11a	V_{CC} = +9V	Diff.-Ampl.	28	32			
Input Admittance		Y_{11}	-	f = 10.7 MHz V_{CC} = +9V	Cascode	-	0.6 + j 1.6	-	mmho	12
			-		Diff.-Ampl.	-	0.5 + j 0.5	-		13
Reverse Transfer Admittance		Y_{12}	-		Cascode	-	0.0003 - j0	-	mmho	14
			-		Diff.-Ampl.	-	0.01 - j0.0002	-		15
Forward Transfer Admittance		Y_{21}	-		Cascode	-	99 - j18	-	mmho	16
			-		Diff.-Ampl.	-	-37 + j0.5	-		17
Output Admittance		Y_{22}	-		Cascode	-	0. + j0.08	-	mmho	18
			-		Diff.-Ampl.	-	0.04 + j0.23	-		19
Voltage Gain	at f = 10.7 MHz	A	22a	f = 10.7 MHz	Cascode	-	40	-	dB	22b
			22c	V_{CC} = +0V R_L = 1 kΩ	Diff.-Ampl.	-	30	-		22d
Peak-to-Peak Output Current		P-P		V_{CC} = +9V	f = 10.7 MHz e_{in} = 400 mV Diff.-Ampl.	2	4	7	mA	
				V_{CC} = +12V		3.5	6	10		

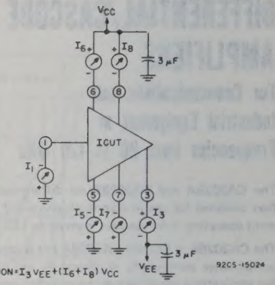


Fig.3a - Input offset current, input bias current, device dissipation, and quiescent operating current test circuit for CA3028A and CA3028B.

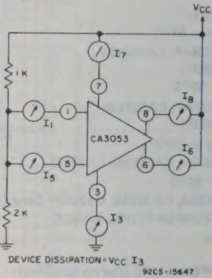


Fig.3b - Input bias current, device dissipation, and quiescent operating current test circuit for CA3053.

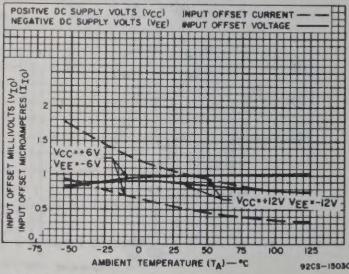


Fig.4 - Input offset voltage and input offset current for CA3028B.

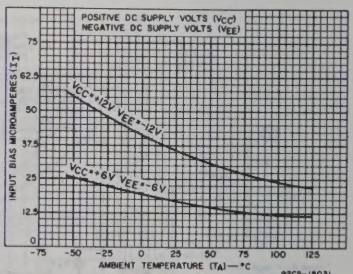


Fig.5a - Input bias current vs. ambient temperature for CA3028A and CA3028B.

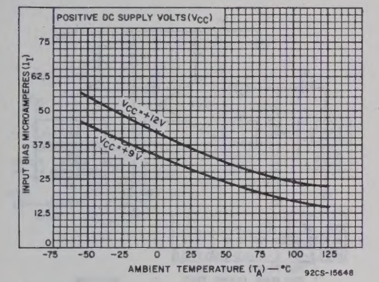


Fig.5b - Input bias current vs. ambient temperature for CA3053.

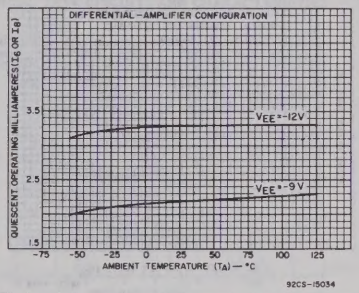


Fig.6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

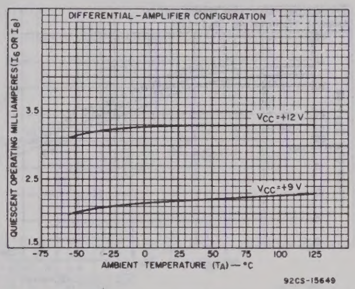


Fig.6b - Quiescent operating current vs. ambient temperature for CA3053.

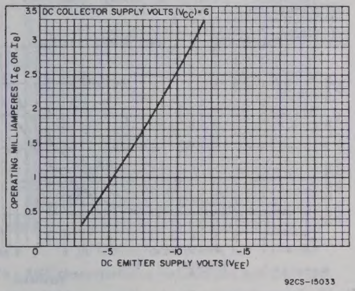


Fig.7 - Operating current vs. V_{EE} voltage for CA3028A and CA3028B.

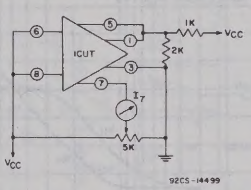


Fig.8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

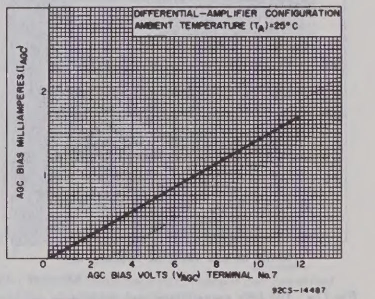


Fig.8b - AGC bias current vs. bias volts (terminal No.7) for CA3028A and CA3028B.

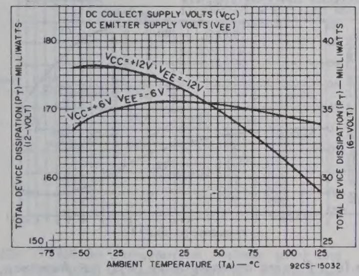
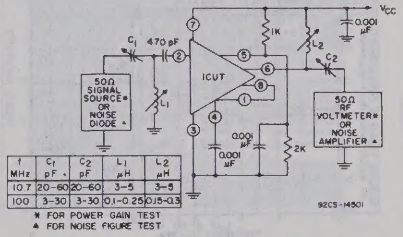


Fig.9 - Device dissipation vs. temperature for CA3028A and CA3028B.


VCC
7
1K
0.001 µF
C1
470 pF
2
L2
5
C2
6
ICUT
50Ω SIGNAL SOURCE* OR NOISE DIODE ▲
L1
8
1
50Ω RF VOLTMETER* OR NOISE AMPLIFIER ▲
4
3
0.001 µF
0.001 µF
2K
92CS-14501

f MHz	C1 pF	C2 pF	L1 µH	L2 µH
10.7	20-60	20-60	3-5	3-5
100	3-30	3-30	0.1-0.25	0.15-0.3

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.

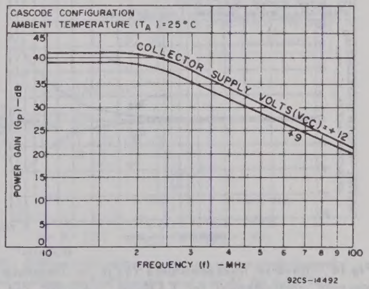


Fig.10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

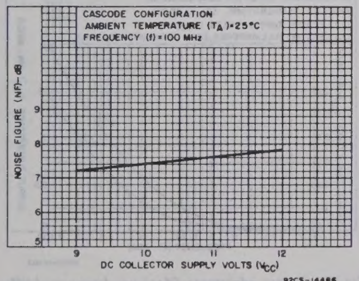
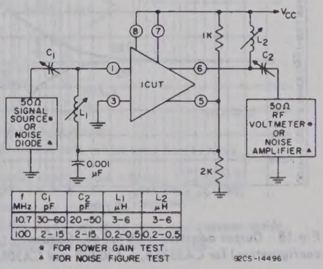


Fig.10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS


VCC
8
7
1K
L2
C1
C2
1
6
ICUT
3
5
50Ω SIGNAL SOURCE* OR NOISE DIODE ▲
L1
50Ω RF VOLTMETER* OR NOISE AMPLIFIER ▲
0.001 µF
2K
92CS-14496

f MHz	C1 pF	C2 pF	L1 µH	L2 µH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No.7 connected to V_{CC}) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.

CA3028A, CA3028B, CA3053 Types

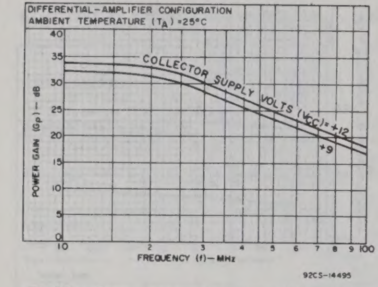


Fig.11b - Power gain vs. frequency (differential-amplifier configuration) for CA3028A and CA3028B.

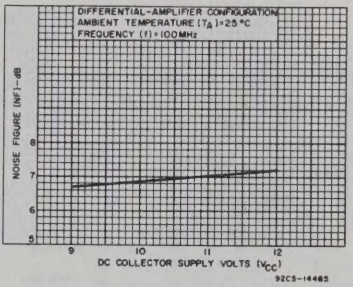
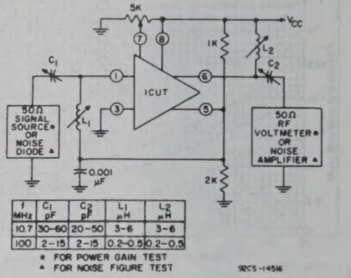


Fig.11c - 100 MHz noise figure vs. collector supply voltage (differential-amplifier configuration) for CA3028A and CA3028B.


5K
V_CC
7
8
1K
L_2
C_2
C_1
1
6
ICUT
3
5
50Ω SIGNAL SOURCE* OR NOISE DIODE ▲
L_1
50Ω RF VOLTMETER* OR NOISE AMPLIFIER ▲
0.001 µF
2K
92CS-14516

f MHz	C1 pF	C2 pF	L1 µH	L2 µH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.11d - Power gain and noise figure test circuit (differential-amplifier configuration for CA3028A and CA3028B.

TYPICAL ADMITTANCE PARAMETERS

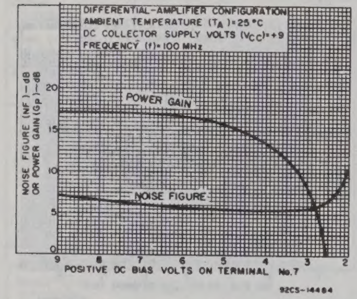


Fig.11e - 100 MHz noise figure and power gain vs. base-to-emitter bias (terminal No.7) for CA3028A and CA3028B.

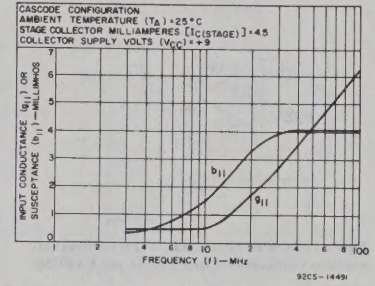


Fig.12 - Input admittance (Y11) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

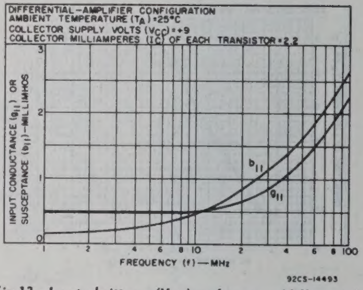


Fig.13 - Input admittance (Y11) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

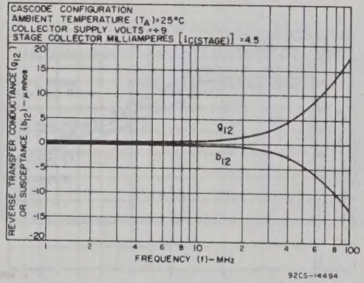


Fig.14 - Reverse transadmittance (Y12) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

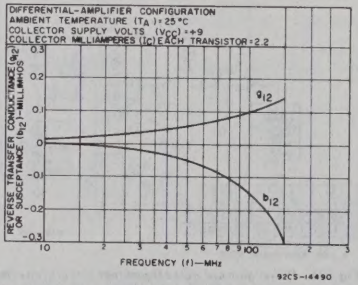


Fig.15 - Reverse transadmittance (Y12) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

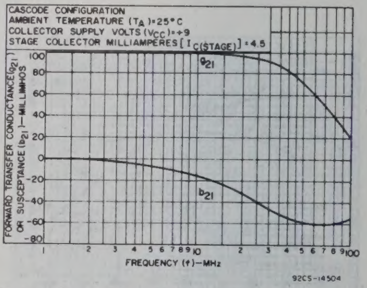


Fig.16 - Forward transadmittance (Y21) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

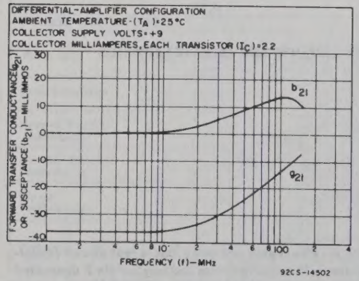


Fig.17 - Forward transadmittance (Y21) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

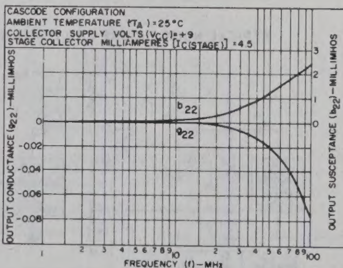


Fig.18 - Output admittance (Y22) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

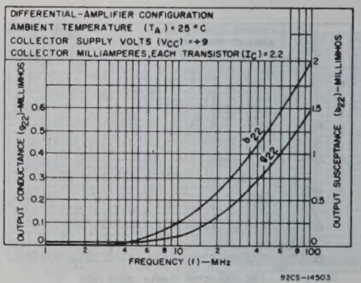


Fig.19 - Output admittance (Y22) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL TEST CIRCUITS AND CHARACTERISTICS

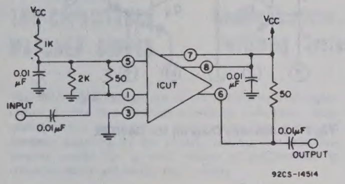


Fig.20a - Output power test circuit for CA3028A and CA3028B.

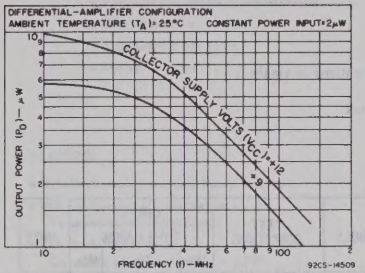
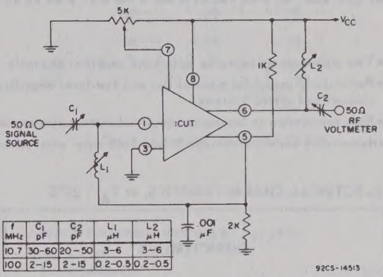


Fig.20b - Output power vs. frequency — 50 Ω input and 50 Ω output (differential-amplifier configuration) for CA3028A and CA3028B.



f MHz	C1 pF	C2 pF	L1 µH	L2 µH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

Fig.21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

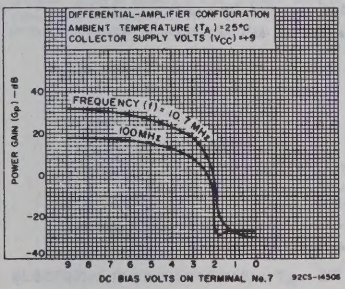


Fig.21b - AGC characteristics for CA3028A and CA3028B.

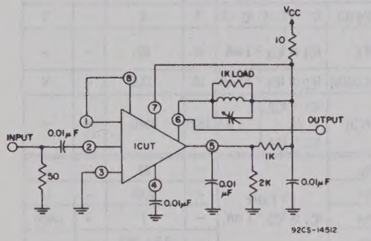


Fig.22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

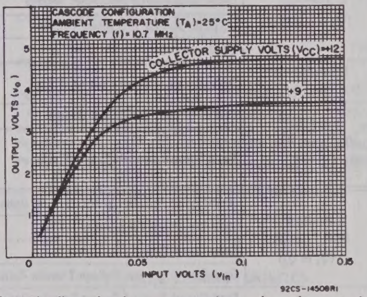


Fig.22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

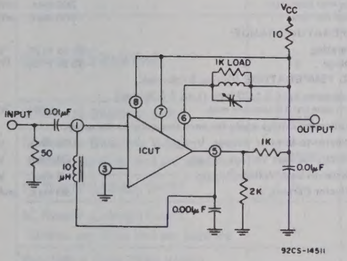


Fig.22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

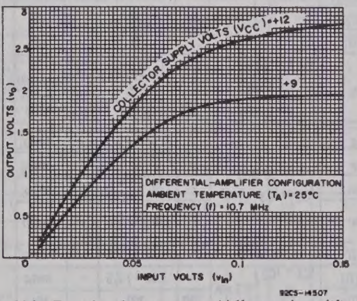
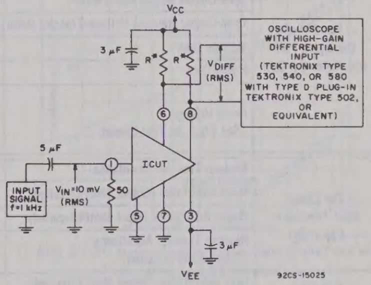
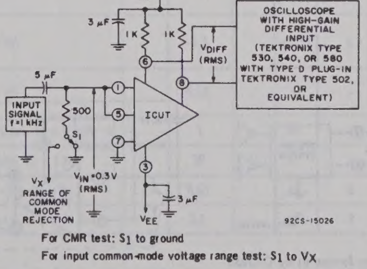


Fig.22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.


VCC
3 µF
R*
R*
VDIFF (RMS)
OSCILLOSCOPE WITH HIGH-GAIN DIFFERENTIAL INPUT (TEKTRONIX TYPE 530, 540, OR 580 WITH TYPE D PLUG-IN TEKTRONIX TYPE 502, OR EQUIVALENT)
5 µF
ICUT
INPUT SIGNAL f = 1 kHz
VIN = 10 mV (RMS)
50
3 µF
VEE
92CS-15025

* For R = 1.6 kΩ – (V_{CC} = 12V, V_{EE} = -12V)
For R = 2 kΩ – (V_{CC} = 6V, V_{EE} = -6V)

Fig.23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.


VCC
3 µF
1K
1K
VDIFF (RMS)
OSCILLOSCOPE WITH HIGH-GAIN DIFFERENTIAL INPUT (TEKTRONIX TYPE 530, 540, OR 580 WITH TYPE D PLUG-IN TEKTRONIX TYPE 502, OR EQUIVALENT)
5 µF
INPUT SIGNAL f = 1 kHz
500
S1
ICUT
VX RANGE OF COMMON MODE REJECTION
VIN = 0.3 V (RMS)
3 µF
VEE
92CS-15026

For CMR test: S_1 to ground

For input common-mode voltage range test: S_1 to V_X

$$\text{Common mode rejection ratio} = 20 \log_{10} \frac{(A^*)\,(2)\,(0.3)}{V_{DIFF}\,(RMS)}$$

* A = Single-ended voltage gain.

Fig.24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.

CA3036

DUAL DARLINGTON ARRAY

- Two independent low-noise wide-band amplifier channels
- Particularly useful for preamplifier and low-level amplifier applications in single-channel and stereo systems
- Wide application in low-noise industrial instrumentation amplifiers
- Hermetically sealed, all-welded 10-lead TO-5-style metal package

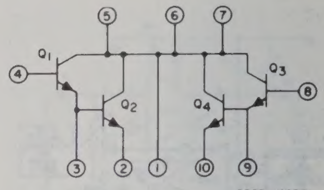


Fig.1 – Schematic Diagram for CA3036.

HIGHLIGHTS

- Matched transistors with emitter-follower outputs
- Low-noise performance
- 200-MHz gain-bandwidth product
- Operation from -55°C to ·125°C

APPLICATIONS

- Stereo phonograph preamplifiers
- Low-level stereo and single channel amplifier stages
- Low-noise, emitter-follower differential amplifiers
- Operational amplifier drivers

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

CHARACTERISTICS		SYMBOLS	TEST CONDITIONS	LIMITS TYPE CA3036 Min.	Typ.	Max.	UNITS
For Each Transistor (Q_1, Q_2, Q_3, Q_4)	Collector-Cutoff Current	I_{CBO}	$V_{CB} = 5V$, $I_E = 0$	–	–	0.5	μA
	Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10\ V$, $I_B = 0$	--	--	5	μA
	Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\ mA$, $I_B = 0$	15	20	--	V
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$	30	44	--	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$	5	6	--	V
For Either Input Transistnr (Q_1 or Q_3)	Static Forward Current-Transfer Ratio	h_{FE}	I_{C1} or $I_{C3} = 1\ mA$	30	82	--	--
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Emitter-to-Base Breadkown Voltage	$V_{(BR)EBO(D)}$	I_{E2} or $I_{E4} = 10\ \mu A$	10	12.6	--	V
	Static Forward Current-Transfer Ratio	$h_{FE(D)}$	$\left.\begin{matrix}I_{C1} + I_{C2}\\ \text{or}\\ I_{C3} + I_{C4}\end{matrix}\right\} = 1\ mA$	1000	4540	--	–
For Each Input Transistor (Q_1 or Q_3)	Short-Circuit Forward Current-Transfer Ratio	h_{fe}	$f = 1\ kHz$ I_{C1} or $I_{C3} = 1\ mA$	--	82	–	--
	Short-Circuit Input Impedance	h_{ie}		--	2.6K	–	Ω
	Open-Circuit Output Admittance	h_{oe}		--	7	–	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	9.8×10^{-5}	--	–
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Short-Circuit Forward Current-Transfer Ratio	$h_{fe(D)}$	$f = 1\ kHz$ $\left.\begin{matrix}I_{C1} + I_{C2}\\ \text{or}\\ I_{C3} + I_{C4}\end{matrix}\right\} = 1\ mA$	–	1300	--	--
	Short-Circuit Input Impedance	$h_{ie(D)}$		–	82K	–	Ω
	Open-Circuit Output Admittance	$h_{oe(D)}$		--	108	--	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	$h_{re(D)}$		--	2.7×10^{-3}	--	--
	Voltage Gain	$A_{(D)}$		--	26	--	dB
	Power Gain	$G_{p(D)}$		--	47	--	dB
	Noise Voltage See Fig.3 for Test Circuit	E_N	$f = 100\ Hz$	–	0.2	3	$\frac{\mu V(rms)}{\sqrt{f(Hz)}}$
			$f = 1\ kHz$	–	0.05	0.3	
			$f = 10\ kHz$	--	0.012	0.1	
For Either Input Transistor (Q_1 or Q_3)	Forward Transfer Admittance	y_{fe}	$f = 50\ MHz$ I_{C1} or $I_{C3} = 2\ mA$	--	0.68 + j 7.9	--	mmho
	Input Admittance (Output Short-Circuited)	y_{ie}		–	4.14 + j 5.95	–	mmho
	Output Admittance (Input Short-Circuited)	y_{oe}		--	1.94 + j 2.64	–	mmho
	Reverse Transfer Admittance (Input Short-Circuited)	y_{re}		--	Negligible	--	mmho
For either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Input Admittance (Output Short-Circuited)	$y_{ie(D)}$	$f = 50\ MHz$ $\left.\begin{matrix}I_{C1} + I_{C2}\\ \text{or}\\ I_{C3} + I_{C4}\end{matrix}\right\} = 2\ mA$	–	1.71 + j 2.8	–	mmho
	Output Admittance (Input Short-Circuited)	$y_{oe(D)}$		–	3.96 + j 2.6	--	mmho
	Gain-Bandwidth Product	$f_{T(D)}$		150	200	--	MHz

MAXIMUM RATINGS, Absolute-Maximum Values:

POWER DISSIPATION, P:

Any one transistor	300 max.	mW
Total for array	600 max.	mW

TEMPERATURE RANGE:

Operating	–55 to +125	°C
Storage	–65 to +150	°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

The following ratings apply for each transistor in the array:

Collector-to-Emitter Voltage, V_{CEO}	15 max.	V
Collector-to-Base Voltage, V_{CBO}	30 max.	V
Emitter-to-Base Voltage, V_{EBO}	5 max.	V
Collector Current, I_C	50 max.	mA

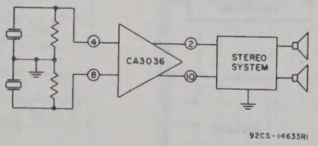


Fig.2 - Block Diagram of Stereo System using CA3036 as Phono Preamplifier.

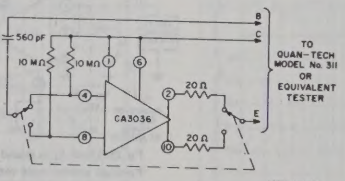


Fig.3 - Noise Voltage Test Circuit for CA3036.

CA3039

Diode Array

Six Matched Diodes on a Common Substrate

ULTRA-FAST LOW-CAPACITANCE MATCHED DIODES

For Applications in Communications and Switching Systems

The RCA-CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

APPLICATIONS

- **Balanced modulators or demodulators**
- **Ring modulators**
- **High speed diode gates**
- **Analog switches**

FEATURES

- **Excellent reverse recovery time – 1 ns typ.**
- **Matched monolithic construction – V_F matched within 5 mV**
- **Low diode capacitance – C_D = 0.65 pF typical at V_R = – 2 V**

* The CA3039 is available in a sealed-junction Beam-Lead version (CA3039L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

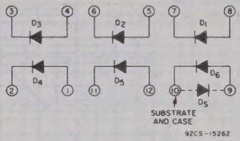


Fig. 1 - Schematic Diagram for CA3039

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:	
Any one diode unit	100 mW
Total for device	600 mW
For $T_A > 55°C$	derate linearly 5.7 mW/°C
TEMPERATURE RANGE:	
Operating	–55 to +125°C
Storage	–65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 265°C
PEAK INVERSE VOLTAGE, PIV for: D_1–D_5	5 V
D_6	0.5 V
PEAK DIODE-TO-SUBSTRATE VOLTAGE, V_{DI}	
for D_1–D_5 (term. 1,4,5,8 or 12 to term. 10)	+ 20, –1 V
DC FORWARD CURRENT, I_F	25 mA
PEAK RECURRENT FORWARD CURRENT, I_f	100 mA
PEAK FORWARD SURGE CURRENT, $I_{f(surge)}$	100 mA

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS	CHARAC-TERISTIC CURVES
			MIN.	TYP.	MAX.		FIG.
DC Forward Voltage Drop	V_F	I_F = 50 µA	–	0.65	0.69	V	2
		1 mA	–	0.73	0.78	V	
		3 mA	–	0.76	0.80	V	
		10 mA	–	0.81	0.90	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = –10 µA	5	7	–	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = –10 µA	20	–	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = –4 V	–	0.016	100	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = –10 V	–	0.022	100	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\left\| V_{F_1} - V_{F_2} \right\|$	I_F = 1 mA	–	0.5	5	mV	2
Temperature Coefficient of $\left\| V_{F_1} - V_{F_2} \right\|$	$\frac{\Delta \left\| V_{F_1} - V_{F_2} \right\|}{\Delta T}$	I_F = 1 mA	–	1	–	µV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	–1.9	–	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	–	0.65	–	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω	7
Diode Capacitance	C_D	V_R = –2 V, I_F = 0	–	0.65	–	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF	9

TYPICAL CHARACTERISTICS

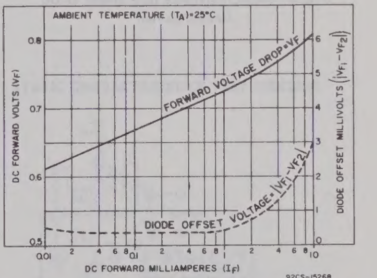


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

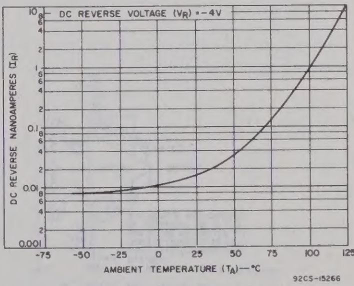


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

This device is supplied in the hermetic 12-lead TO-5 style package.

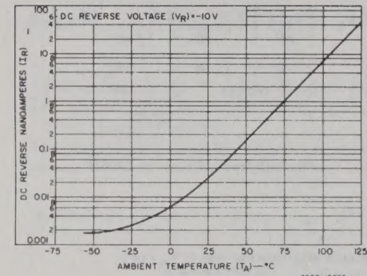


Fig. 4 - DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature

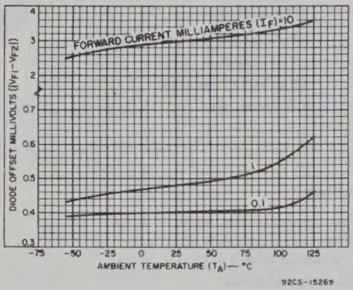


Fig. 5 - Diode offset voltage (any diode) vs temperature

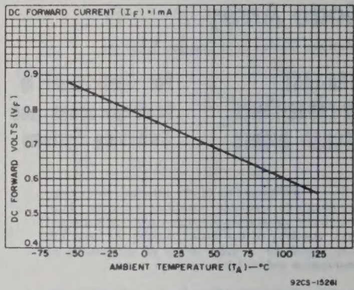


Fig. 6 - DC forward voltage drop (any diode) vs temperature

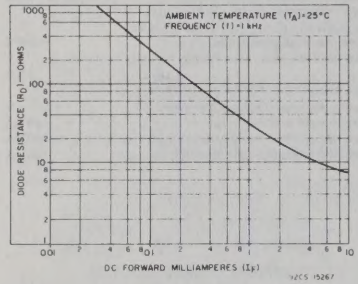


Fig. 7 - Diode resistance (any diode) vs DC forward current

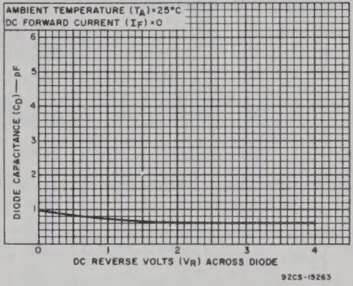


Fig. 8 - Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage

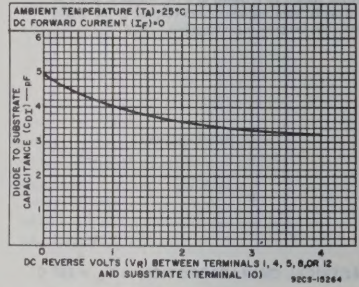


Fig. 9 - Diode-to-substrate capacitance vs reverse voltage

CA3040

Video and Wideband Amplifier

For Industrial and Commercial Equipment at Frequencies up to 200 MHz

The RCA CA3040 is a monolithic silicon integrated circuit designed to meet the requirements of a wide variety of applications requiring high gain and wide bandwidth. The cascode-connected differential amplifier achieves a double-ended gain of 37 dB with a typical 3 dB bandwidth of 55 MHz. Emitter-Follower input and output stages provide the desirable high input impedance and low output impedance for coupling to other circuits.

The CA3040 includes two biasing options, allowing the user to optimize his design over the entire military temperature range of -55 to +125°C. **Bias Mode A** yields a substantially constant voltage at the output terminals for applications using DC coupling to succeeding stages or requiring maximum dynamic range over the temperature range. DC output voltage varies less than 0.1 volt (typically) over the entire temperature range while gain varies ±2 dB. **Bias Mode B** provides extremely stable gain over the temperature range. Gain variation is 0 dB (typically) in this Bias Mode. DC variation is ±0.8 volt.

Provisions are also made for stabilizing the operating point for either single or split power supplies.

FEATURES

• High Differential Push-Pull Voltage Gain	37 dB	typ.
Single-Ended Voltage Gain	31 dB	typ.
• Wide (3dB) Bandwidth	55 MHz	typ.
• Balanced Input and Output		
• High Input Resistance	150 kΩ	typ.
• Low Output Resistance	125 Ω	typ.

- Bias Options for Temperature Compensation:
  - Bias Mode A: "Constant" Voltage
  - Bias Mode B: "Constant" Gain
- **Supplied in the hermetic 12-lead TO-5 style package**

APPLICATIONS

- Video Amplifier
- Schmitt Trigger
- Modulator
- IF Amplifier
- Mixer
- DC Amplifier
- Sense Amplifier

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION *	450 mW
Derating factor for $T_A > 85^{\circ}C$	5 mW/°C
TEMPERATURE RANGE:	
Operating	-55°C to +125°C
Storage	-65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C

* Limitation imposed by the thermal resistance of package.

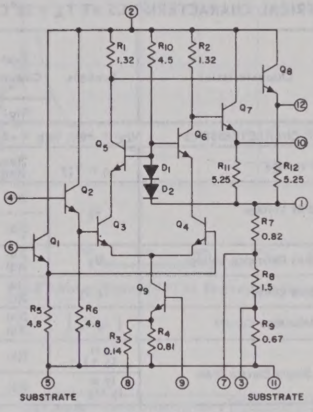


Fig.1 - Schematic Diagram for CA3040

MAXIMUM VOLTAGE RATINGS at $T_A = 25^{\circ}C$

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 2 with respect to terminal 11 is 0 to +14 volts.

TERMINAL No.	1	2	3	4	5▲	6	7	8	9	10	11▲	12
1		0 -14	*	*	+14 0	*	+10 -10	*	*	*	+14 0	*
2			*	+14 0	+14 0	+14 0	*	*	*	+14 0	+14 0	+14 0
3				*	+5 -3	*	*	*	*	*	+5 -3	*
4					*	+3 -3	*	*	*	*	*	*
5▲					▲	*	+10 -3	*	+3 -7	*	0 Note 1	*
6							*	*	*	*	*	*
7								*	*	*	+10 -3	*
8									+3 -3	*	*	*
9										*	+7 -3	*
10											*	*
11▲											▲	*
12												

▲ Reference Substrate

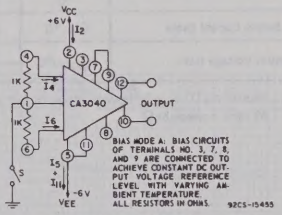
Note 1: External connection required for proper operation.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

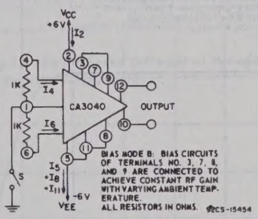
TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	-	-
3	5	5
4	1	0.1
5	-	-
6	1	0.1
7	5	5
8	5	5
9	1	0.1
10	-	10
11	-	-
12	-	10

STATIC CHARACTERISTICS TEST CIRCUITS



VCC
+6V
I2
②
③
⑦
⑨
④
⑫
1K
I4
①
CA3040
OUTPUT
1K
I6
⑩
⑧
⑥
⑪
⑤
S
I5 + I11
-6V
VEE
BIAS MODE A: BIAS CIRCUITS OF TERMINALS NO. 3, 7, 8, AND 9 ARE CONNECTED TO ACHIEVE CONSTANT DC OUTPUT VOLTAGE REFERENCE LEVEL WITH VARYING AMBIENT TEMPERATURE.
ALL RESISTORS IN OHMS.
92CS-15455

Fig.2(a) - Bias Mode A



VCC
+6V
I2
②
③
⑦
⑨
④
⑫
1K
I4
①
CA3040
OUTPUT
1K
I6
⑩
⑧
⑥
⑪
⑤
S
I5 +I8 +I11
-6V
VEE
BIAS MODE B: BIAS CIRCUITS OF TERMINALS NO. 3, 7, 8, AND 9 ARE CONNECTED TO ACHIEVE CONSTANT RF GAIN WITH VARYING AMBIENT TEMPERATURE.
ALL RESISTORS IN OHMS.
92CS-15454

Fig.2(b) - Bias Mode B

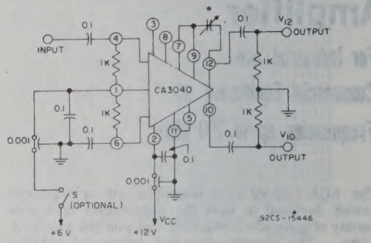
CA3040

ELECTRICAL CHARACTERISTICS AT $T_A = 25°C$ Unless Otherwise Specified

Characteristics	Symbols	Test Circuits Fig.	Special Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
STATIC CHARACTERISTICS	V_{CC} = +6V, V_{EE} = -6V						
Output Voltage	V_{10} or V_{12}	2(a) 2(b)	Bias Mode A or B: Switch Closed	1.4	2.7	3.7	V
Base Bias Voltage	V_9	2(a)	Bias Mode A Switch Closed	-	-1.7	-	V
		2(b)	Bias Mode B Switch Closed	-	-1.7	-	V
Input Bias Reference Voltage	V_1	2(a) 2(b)	Bias Mode A or B: Switch Open	-1	-	+1	V
Input Bias Current	I_4, I_6	2(a) 2(b)	Bias Mode A or B: Switch Closed	-	15	45	μA
Input Unbalance Current	$\lvert I_6 - I_4 \rvert$	2(a) 2(b)	Bias Mode A or B: Switch Closed	-	-	6	μA
Power Supply Current Drain	I_2 or $I_5 + I_{11}$	2(a)	Mode A Switch open or closed	4.7	8.5	15.5	mA
	I_2 or $I_5 + I_8 + I_{11}$	2(b)	Mode B Switch open or closed				
DYNAMIC CHARACTERISTICS	V_{CC} = +12V, V_{EE} = 0, Split Voltage Supply (Optional) = +6V						
Differential Voltage Gain							
Single-Ended Input Differential Output	$A_{DIFF(DE)}$	3(a)	f = 1 MHz R_s = 50 Ω	34	37	-	dB
Single-Ended Input and Output	$A_{DIFF(SE)}$	3(a)	f = 1 MHz R_s = 50 Ω	28	31	-	dB
-3 dB Bandwidth	BW	3(a)	R_s = 50 Ω	40	55	-	MHz
Differential Voltage Gain Balance	$A_{DIFF(SE)10} - A_{DIFF(SE)12}$	3(a)	f = 1 MHz	-1	0	+1	dB
Output Voltage Swing	V_8 or V_{10} RMS	3(a)	f = 1 MHz R_s = 50 Ω	-	0.5	-	V_{RMS}
Noise Figure	NF	3(a)	(Note 1) f = 30 MHz R_s = 400 Ω	-	7.5	9	dB
Parallel Input Resistance	R_I	3(a)	f = 1 MHz	-	150	-	kΩ
Parallel Input Capacitance	C_I	3(a)		-	2.2	-	pF
Output Resistance	R_O	3(a)		-	125	-	Ω
TEMPERATURE DEPENDENT CHARACTERISTICS Temperature coefficients for ambient temperature: $-55°C \leq T_A \leq +125°C$							
Output Voltage	$\frac{\Delta V_{10} \text{ or } \Delta V_{12}}{°C}$	3(a)	Bias Mode A	-	0	-	mV/°C
		3(b)	Bias Mode B	-	6.4	-	mV/°C
Power Supply Current Drain	$\Delta I_2/°C$	3(a)	Bias Mode A	-	5	-	μA/°C
Differential Voltage Gain	$A_{DIFF}/°C$	3(a)	Bias Mode A	-	0.0166	-	dB/°C
		3(b)	Bias Mode B	-	0	-	

Note 1: Replace 1-kΩ resistors between Term. 1 and 4 and Term. 1 and 6 with suitable chokes so that reactance at 30 MHz exceeds 5kΩ

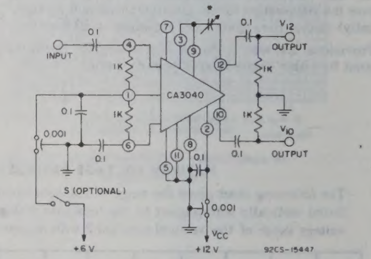
DYNAMIC CHARACTERISTICS TEST CIRCUITS



* VARIABLE CAPACITANCE (0.5-1.0μF) ADJUSTMENT FOR EQUAL 3dB BANDWIDTH AT AMPLIFIER OUTPUTS, TERMINALS 10 AND 12

ALL RESISTORS IN OHMS
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED)
BIAS MODE A IS AS DEFINED IN FIG 2(a)

Fig.3(a) - Bias Mode A



* SEE FIG 3(a)

BIAS MODE B IS AS DEFINED IN FIG 2(b)
ALL RESISTORS IN OHMS
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED)

Fig.3(b) - Bias Mode B

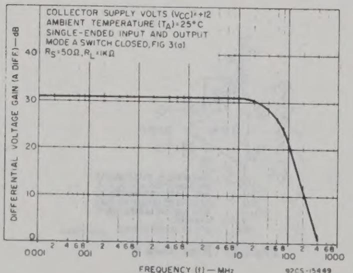


Fig.4 - Differential Voltage Gain vs Frequency

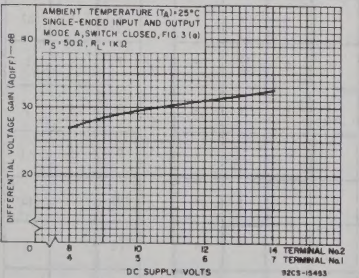


Fig.5 - Differential Voltage Gain vs DC Supply Voltages

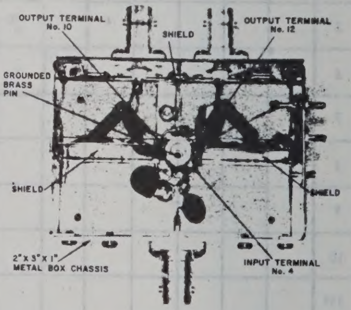


Fig.6 - Test Circuit Layout

OPERATING CONSIDERATIONS

General

The CA3040 is designed to provide flexibility in the selection of power supply configurations and to provide the circuit designer the choice between two modes of temperature-compensated performance. Mode A, which provides constant DC output voltage, is recommended for most applications. The control of the operating point provided by this mode maintains the dynamic range of the device while gain variation over most of the range is less than ±1 dB. Mode B provides constant gain for applications where this consideration is critical, but will exhibit a reduction of dynamic range at the temperature extremes.

Power Supply Considerations

Figures 2 and 3 illustrate the use of the CA3040 with balanced dual supplies and single power supplies, respectively. Both figures demonstrate that the inputs may be directly referenced to the center point of the supply (ground in Fig.2) by closing the included switch. This is the natural connection in Fig.2. This connection is optional, however, and need not be made. Use of this connection in Fig.3 implies the presence of another DC supply or a "stiff" bleeder. If such a source is present its use is suggested in order to maintain maximum common mode range. Dynamic performance and dynamic range of the output circuit are unaffected by the choice of biasing scheme used so that in most cases direct connection of Terminal No.1 to the center point of the supply is not required. Where direct connection is not used, Terminals No.4 and No.6 must be biased from Terminal No.1 for proper operation.

High-Frequency Considerations

Stable high-frequency operation requires that proper high-frequency construction techniques be followed. The photograph of Fig.6 illustrates the precautions taken in the construction of the test circuit of Fig.3.

Extreme caution is required because of the extended gain bandwidth capability of the device. Oscillations have been observed in the 400-to-800 MHz range when precautions were not taken. In addition to normal considerations of shielding, parts layout, and isolation, the following specific suggestions are made:

1. Use sockets only when necessary. Sockets, when used, must provide shielding within the pin circle. The socket shown in the chassis of Fig.6 is a Barnes MG-1201, or equivalent, modified by drilling a 1/8" hole in the center and inserting a grounded brass pin.
2. Do not bypass Terminal No.9 in normal operation. Fig.3 shows the use of neutralization between Terminal No.9 and one output to balance the amplifier at high frequencies. Experience shows that stable operation, while possible, is difficult to achieve if Terminal No.9 is bypassed to ground.
3. In DC testing, 1 kΩ, 1/4 W carbon resistors should be soldered directly to the socket Terminals No.4 and No.6 to suppress parasitic oscillations. All current carrying connections are made at the other end of the resistors. Direct sensing of Terminal No.4 or No.6 voltage should not be attempted.

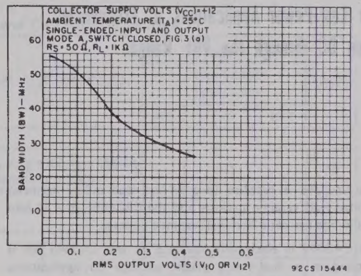


Fig.7 - 3dB Bandwidth vs Single-Ended Output Voltage

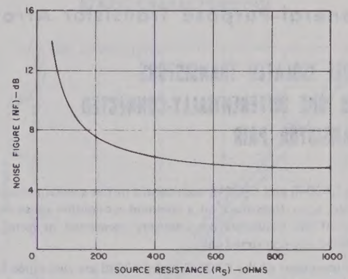


Fig.8 - Noise Figure (NF) vs Source Impedance

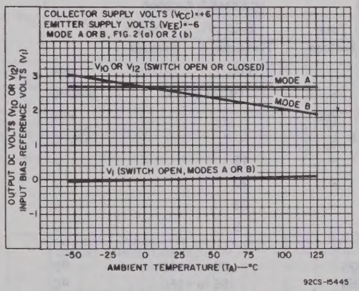


Fig.9 - Output Volts or Input Bias Reference Volts vs Ambient Temperature

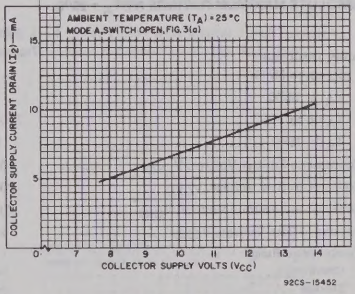


Fig.10 - Collector Supply Current Drain (I_2) vs Collector Supply Voltage (V_{CC})

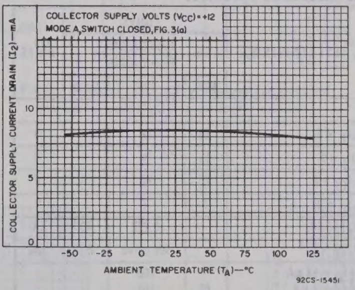


Fig.11 - Collector Supply Current Drain (I_2) vs Ambient Temperature

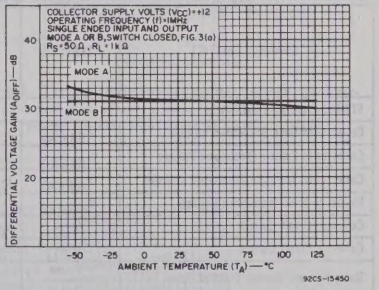


Fig.12 - Single-Ended Differential Voltage Gain vs Ambient Temperature

CA3045, CA3046 Types

General-Purpose Transistor Arrays For Low-Power Applications at Frequencies from DC through the VHF Range

THREE ISOLATED TRANSISTORS AND ONE DIFFERENTIALLY-CONNECTED TRANSISTOR PAIR

The CA3045 and CA3046 each consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

	CA3045		CA3045F, CA3046		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A up to 55°C	–	–	300	750	mW
$T_A > 55$°C	–	–	Derate at 6.67		mW/°C
T_A up to 75°C	300	750	–	–	mW
$T_A > 75$°C	Derate at 8		–	–	mW/°C
Collector-to-Emitter Voltage, V_{CEO}	15	–	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	5	–	V
Temperature Range:					
Operating	−55 to +125		−55 to +125		°C
Storage	−65 to +150		−65 to +150		°C
Lead Temperature (During Soldering): At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max:	+265		+265		°C

** The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046			UNITS
			MIN.	TYP.	MAX.	
STATIC CHARACTERISTICS						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μA, I_{CI} = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V $\begin{cases} I_C = 10\text{ mA} \\ I_C = 1\text{ mA} \\ I_C = 10\ \mu\text{A} \end{cases}$	- 40 -	100 100 54	- - -	- - -
Input Offset Current for Matched Pair Q_1 and Q_2. $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V $\begin{cases} I_E = 1\text{ mA} \\ I_E = 10\text{ mA} \end{cases}$	- -	0.715 0.800	- -	V
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	−1.9	-	mV °C
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} 3 V, I_C 1 mA	-	1.1	-	μV°C

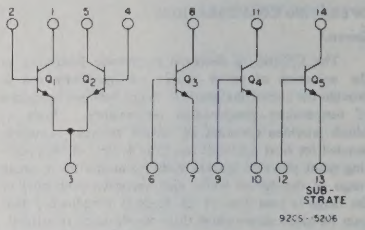


Fig.1 - Schematic diagram.

FEATURES

- **Two matched pairs of transistors**
  V_{BE} matched ±5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- **5 general purpose monolithic transistors**
- **Operation from DC to 120 MHz**
- **Wide operating current range**
- **Low noise figure - - 3.2 dB typ. at 1 kHz**
- **Full military temperature range for CA3045**
  -55 to +125°C
- The CA3045 is available in a sealed-junction Beam-Lead version (CA3045L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

APPLICATIONS

- **General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF**
- **Custom designed differential amplifiers**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

STATIC CHARACTERISTICS

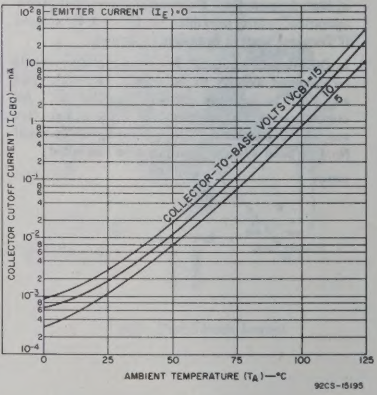


Fig. 2 — Typical collector-to-base cutoff current vs ambient temperature for each transistor.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046			UNITS
			MIN.	TYP.	MAX.	
DYNAMIC CHARACTERISTICS						
Low-Frequency Noise Figure	NF	**f = 1 kHz, V_{CE} = 3V, I_C = 100 μA Source Resistance = 1 kΩ**	-	3.25	-	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF

STATIC CHARACTERISTICS

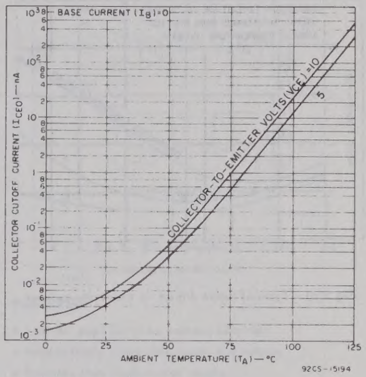


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

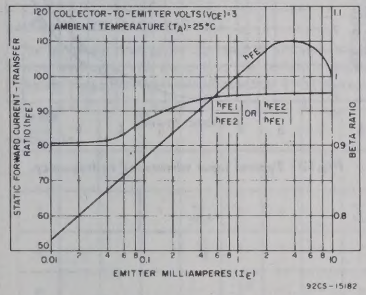


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

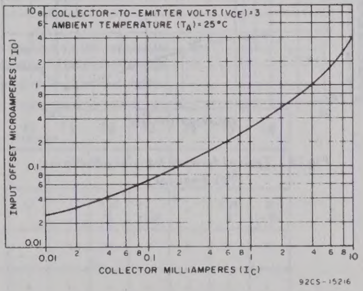


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

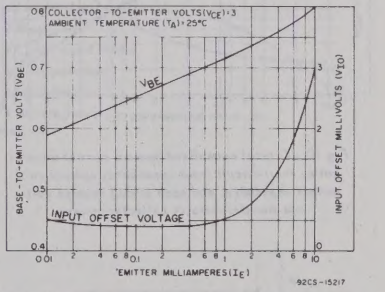


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

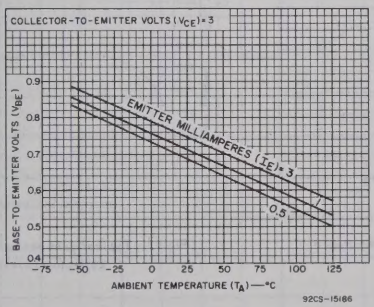


Fig. 7 — Typical base-to-emitter voltage characteristics vs ambient temperature for each transistor.

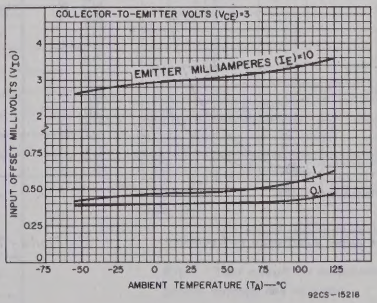


Fig. 8 — Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

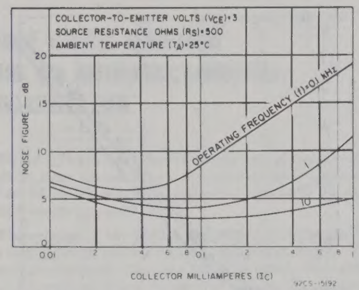


Fig.9(a) - Typical noise figure vs collector current.

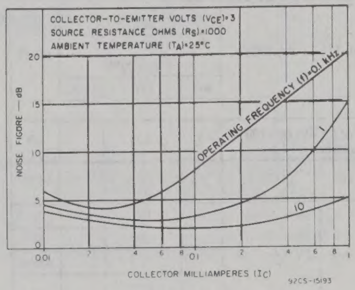


Fig.9(b) - Typical noise figure vs collector current.

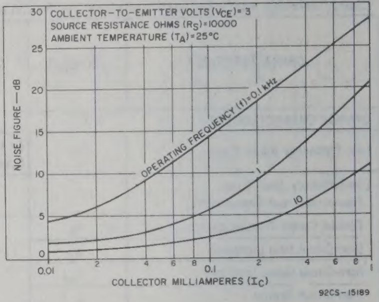


Fig.9(c) - Typical noise figure vs collector current.

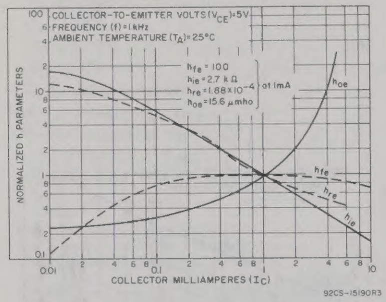


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

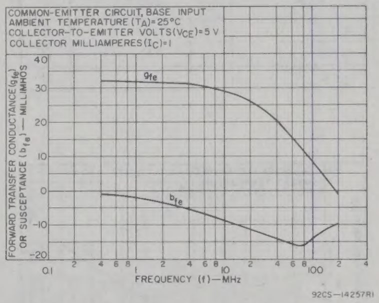


Fig.11 - Typical forward transfer admittance vs frequency.

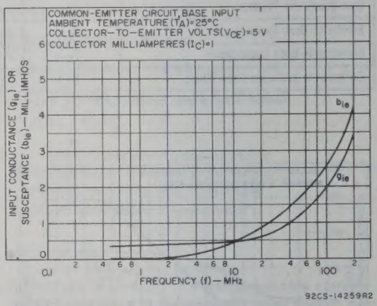


Fig.12 - Typical input admittance vs frequency.

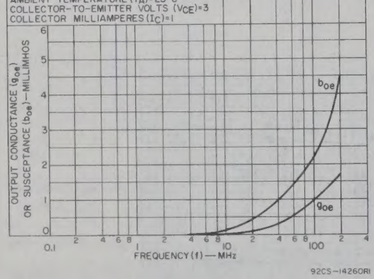


Fig.13 - Typical output admittance vs frequency.

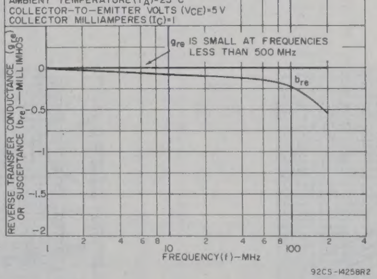


Fig.14 - Typical reverse transfer admittance vs frequency.

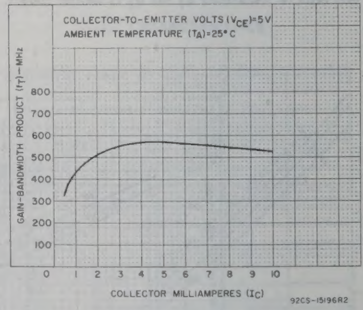


Fig.15 - Typical gain-bandwidth product vs collector current.

Amplifier Array

FOUR INDEPENDENT AC AMPLIFIERS

For Low-Noise and General AC Applications In Industrial Service

The RCA CA3048 is a silicon monolithic integrated circuit consisting of four independent identical AC amplifiers which can operate from a single-ended power supply.

The amplifiers include internal DC bias and feedback to provide temperature-stabilized operation. They may be used in a wide variety of AC applications in which operational amplifiers have previously been used.

Each high gain amplifier has a high impedance non-inverting input, and a lower impedance inverting input for the application of feedback. Two power-supply terminals and two ground terminals are provided to reduce internal and external coupling between amplifiers.

The CA3048 is supplied in a 16-lead dual-in-line plastic package.

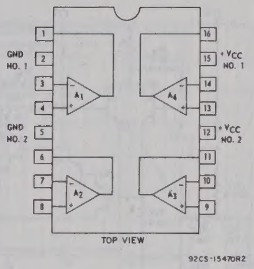


Fig.1 - Block diagram for CA3048.

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

• Noise figure at 1 kHz	2 dB typ.
• High voltage gain	53 dB min.
• High input resistance	90 kΩ typ.
• Undistorted output voltage	2 V rms min.
• Output Impedance	1 kΩ typ.
• Open-loop bandwidth	300 kHz typ.

APPLICATIONS

- Multi-channel or cascade operation
- Low-level preamplifiers
- Equalizers
- Linear signal mixers
- Tone generators
- Multivibrators
- AC integrators

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

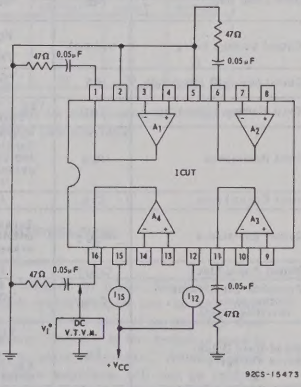
DISSIPATION:	
At T_A = 55°C	750 mW
Above T_A = 55°C	Derate linearly at 7.7 mW/°C
TEMPERATURE RANGE:	
Operating	-40°C to +85°C
Storage	-65°C to +150°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ±0.79mm) from case for 10 seconds max.	+265°C
POWER SUPPLY VOLTAGE	+16 V
AC INPUT VOLTAGE	0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

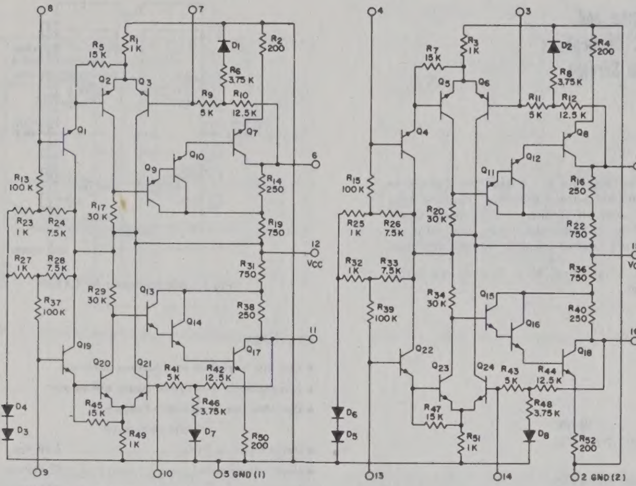
TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	-3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*		*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.



* CONNECT TO APPROPRIATE TERMINAL TO READ VOLTAGE

Fig.2 - Test circuit for measurement of collector supply voltage and currents.



Note: All resistor values are in ohms

92CM-15412

Fig.3 - Schematic diagram for CA3048.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIRCUIT FIG.	LIMITS CA3048 MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC									
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12V		2	9.5	13.5	17.5	mA	4,5
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12V		2	6.1	6.9	8.1	V	-
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12V		2	1.7	2.0	2.3	V	-
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12V		2	2.2	2.5	2.8	V	-
DYNAMIC (Characteristics given are for each amplifier with no AC feedback)									
Open-Loop Gain	A_{OL}	V_{CC} = +12V E_{IN} = 2mV f = 10kHz		6	53	58	-	dB	7,8
Output Voltage Swing	V_O(rms)	V_{CC} = +12V f = 1kHz THD = 5%		6	2.0	2.4	-	V	-
Open-Loop -3dB Bandwidth	BW	V_{CC} = +12V E_{IN} = 2mV		6	250	300	-	kHz	9
Total Harmonic Distortion	THD	V_{CC} = +12V, f = 1kHz E_{OUT} = 2V rms		6	-	0.65	-	%	10
Input Resistance	R_{IN}	OPEN LOOP Terminals 3, 7, 10, and 14 are by-passed to ground f = 1kHz		–	-	90	-	kΩ	-
Input Capacitance	C_{IN}	f = 1MHz		–	-	9	-	pF	–
Output Resistance	R_{OUT}	Terminals 3, 7, 10 and 14 are by-passed to ground		–	-	1	-	kΩ	–
Output Capacitance	C_{OUT}	f = 1MHz		–	-	18	-	pF	–
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12V f = 1MHz		-	-	<0.1	-	pF	–
Broad-Band Output Noise Voltage	E_N	V_{CC} = +12V R_S = 10 kΩ A = 40dB Equivalent Noise BW = 50kHz		11	-	0.3	1	mV	–
Output Noise Voltage "Weighted"	E_N(WT)			12	-	0.5	2.2	mV	–
Noise Figure	NF (R_S = 5 kΩ)	f =	10Hz	-	-	10	-	dB	–
			100Hz	-	-	5.8	-	dB	
			1kHz	-	-	2	-	dB	
			10kHz	-	-	1.1	-	dB	
			100kHz	-	-	0.6	-	dB	
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12V f = 1kHz 0dB = 0.78V		13	-	<-45	-	dB	–
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12V f = 1MHz		-	-	<0.02	-	pF	–

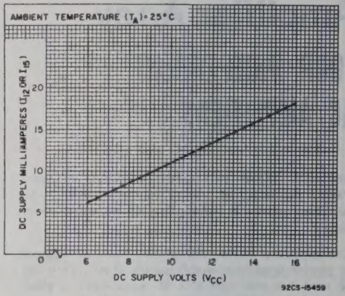


Fig.4 - Typical DC supply current vs supply voltage.

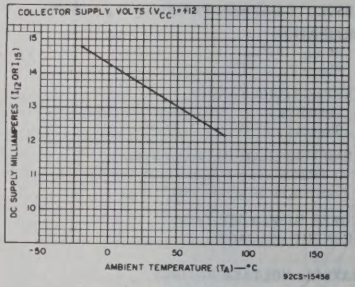
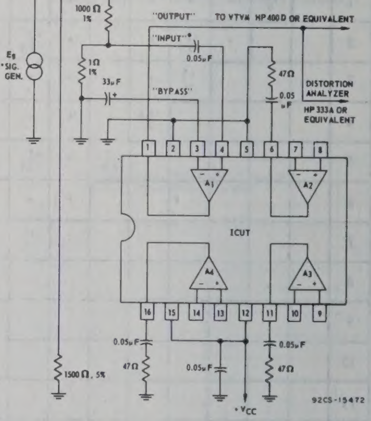


Fig.5 - Typical DC supply current vs ambient temperature.



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

• Adjustment of E_g to 2 volts will make E_s = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.6 - Test circuit for measurement of distortion, open-loop gain and bandwidth characteristics.

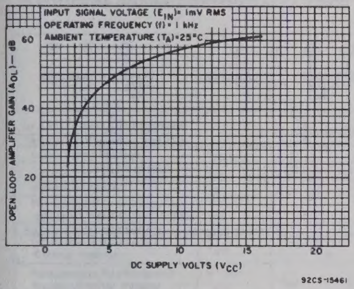


Fig.7 - Typical amplifier gain vs DC supply voltage.

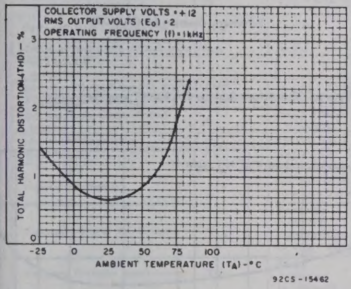
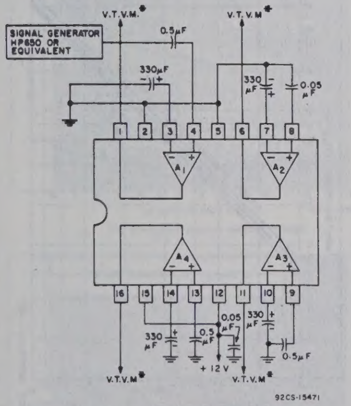


Fig.10 - Typical total harmonic distortion vs ambient temperature.



* V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig.13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

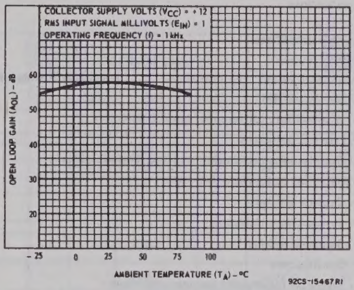
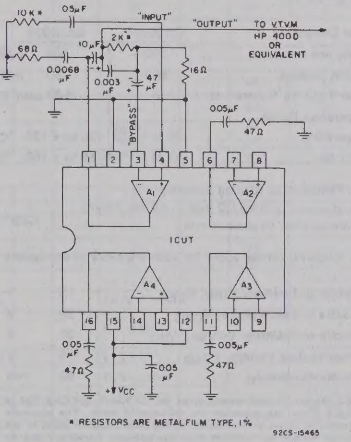


Fig.8 - Typical open-loop gain vs ambient temperature.



To test Amplifiers 1, 2, 3, or 4, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.11 - Test circuit for measurement of broadband noise characteristic.

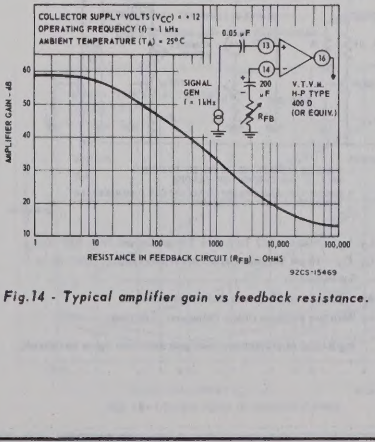


Fig.14 - Typical amplifier gain vs feedback resistance.

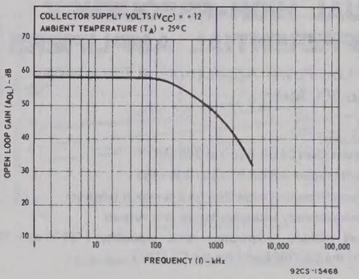
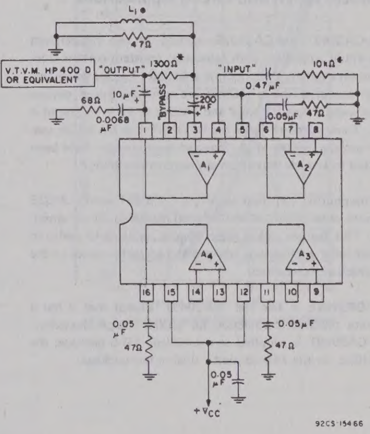


Fig.9 - Typical open-loop gain vs frequency.



● L1 - 2.5 millihenry inductor, dc resistance 0.3 ohms or less.
* Resistors metal film type, 1%. To test amplifiers, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.12 - Test circuit for measurement of "weighted" output noise voltage characteristic.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3048 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig.14 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3048, as in other devices having high gain-bandwidth product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3048 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

CA3049T, CA3102E

DUAL HIGH-FREQUENCY DIFFERENTIAL AMPLIFIERS

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- Power Gain 23 dB (typ.) at 200 MHz
- Noise Figure 4.6 dB (typ.) at 200 MHz
- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Full military-temperature-range capability- (−55°C to + 125°C) for the CA3102E and for the CA3049T

- **The CA3049 is available in a sealed-junction Beam-Lead version (CA3049L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

RCA-CA3049T and CA3102E consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low I/f noise and a value of f_T in excess of 1 GHz. These features make the CA3049T and CA3102E useful from dc to 500 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3049T and CA3102E provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102E is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102E, in the 14-lead plastic dual-in-line package.

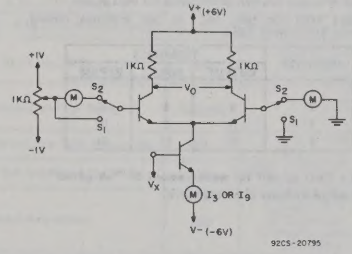


Fig.1—Static characteristics test circuit for CA3102E.

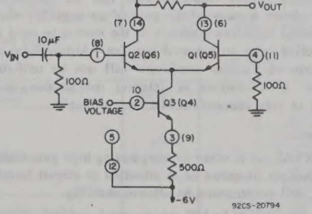


Fig.2—AGC range and voltage gain test circuit for CA3102E.

Applications

- VHF amplifiers
- VHF mixers
- Multifunction combinations — RF/Mixer/Oscillator; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Balanced mixers
- Synthesizers
- Balanced (push-pull) cascode amplifiers
- Sense amplifiers

MAXIMUM RATINGS, *ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C*

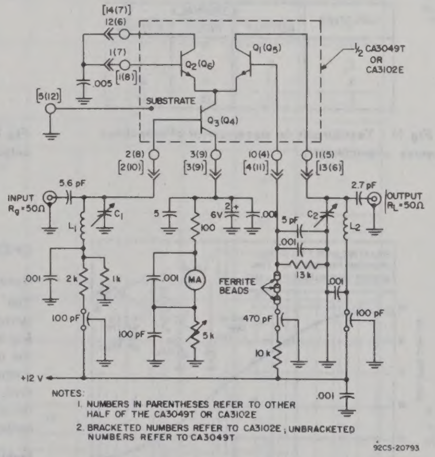
Power Dissipation, P:	CA3049T	CA3102E	
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55°C$ Derate at:	5	6.67	mW/°C
Temperature Range:			
Operating	−55 to + 125	−55 to + 125	°C
Storage	−65 to + 150	−65 to + 150	°C

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T and CA3102E is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.



NOTES:
1. NUMBERS IN PARENTHESES REFER TO OTHER HALF OF THE CA3049T OR CA3102E
2. BRACKETED NUMBERS REFER TO CA3102E; UNBRACKETED NUMBERS REFER TO CA3049T

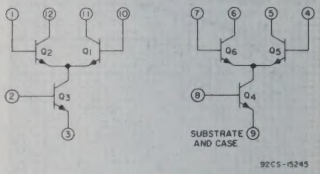
L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.

C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)

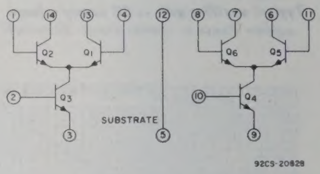
All Capacitors in μF Unless Otherwise Indicated

All Resistors in Ohms Unless Otherwise Indicated

Fig.3—200 MHz cascode power gain and noise figure test circuit.



Schematic Diagram for CA3049T



Schematic Diagram for CA3102E

Typical Characteristics for CA3049T and CA3102E

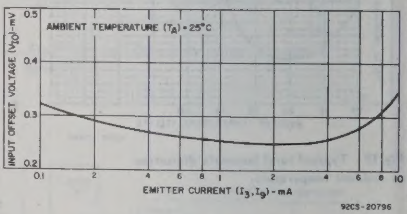


Fig. 4—Input offset voltage vs. emitter current.

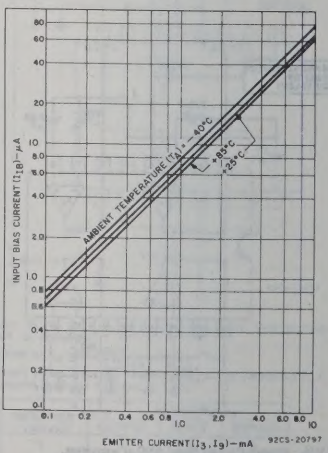


Fig. 5—Input bias current vs. emitter current.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIRCUIT FIG.	CA3049T LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	---	0.25	---	mV	-4
Input Offset Current	I_{IO}	$I_3 = I_9 = 2\text{ mA}$		1	---	0.3	---	μA	---
Input Bias Current	I_{IB}			1		13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			1	---	1.1	---	μV/°C	4
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6\text{ V}$ $I_C = 1\text{ mA}$		---	---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 6\text{ V}, I_C = 1\text{ mA}$		---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10\text{ V}, I_E = 0$		---	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\text{ mA}, I_B = 0$		---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A, I_E = 0$		---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\ \mu A, I_B = 0, I_E = 0$		---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A, I_C = 0$		---	5	7	---	V	---
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	$f = 100\text{ KH}_3$, $R_S = 500\ \Omega$ $I_C = 1\text{ mA}$		---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 6\text{ V}, I_C = 5\text{ mA}$		---	---	1.35	---	GH_z	11
Collector-Base Capacitance	C_{CB}	$I_C = 0$	$V_{CB} = 5V$	* **	--- ---	0.28 0.28	--- ---	pF pF	8
Collector-Substrate Capacitance	C_{CI}	$I_C = 0$	$V_{CI} = 5V$		---	1.65	---	pF	8
For Each Differential Amplifier									
Common-Mode Rejection Ratio	CMR	$I_3 = I_9 = 2\text{ mA}$		---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V f = 10 MHz		2	---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	---	23	---	dB	---
Noise Figure	NF	$V_{CC} = 12V$	Cascode	3	---	4.6	---	dB	---
Input Admittance	Y_{11}	For Cascode Configuration $I_3 = I_9 = 2\text{ mA}$	Cascode	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration $I_3 = I_9 = 4mA$	Cascode	---	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}	(each collector $I_C \simeq 2mA$)	Cascode	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

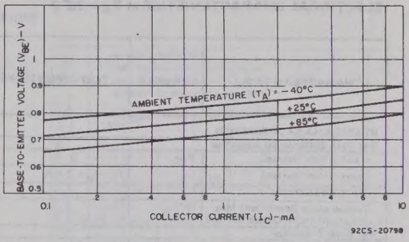


Fig. 6—Base-to-emitter voltage vs. collector current.

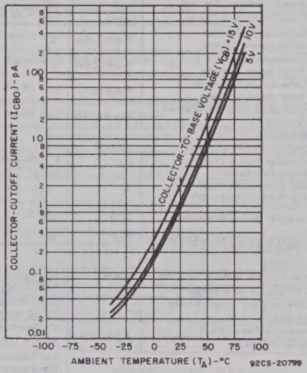


Fig. 7—Collector-cutoff current vs. temperature.

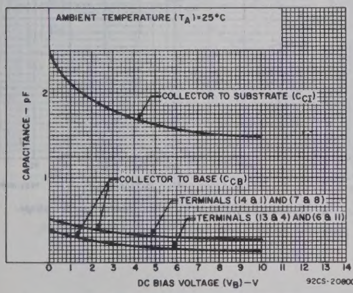


Fig. 8—Capacitance vs. dc bias voltage.

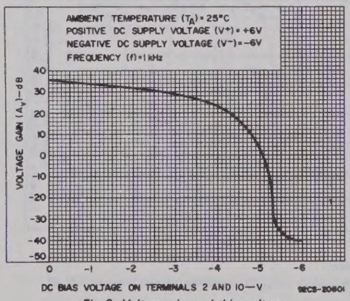


Fig. 9—Voltage gain vs. dc bias voltage.

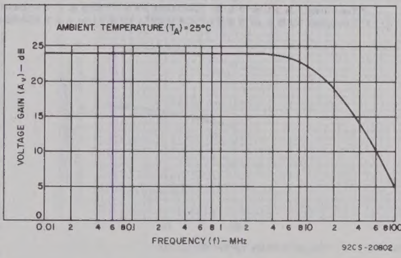


Fig. 10—Voltage gain vs. frequency.

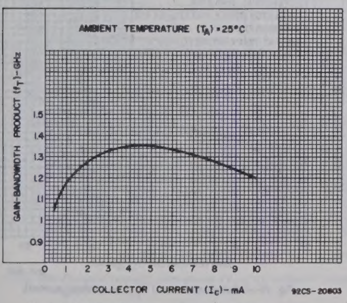


Fig. 11—Gain-bandwidth product vs. collector current.

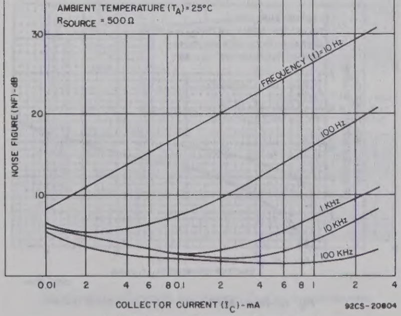


Fig. 12—1/f noise figure vs. collector current.

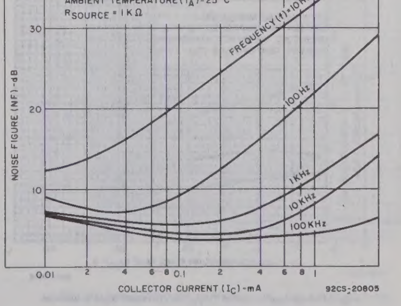


Fig. 13—1/f noise figure vs. collector current.

CA3049T, CA3102E

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIR-CUIT FIG.	CA3102E LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARAC-TERISTICS CURVES FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	···	0.25	5	mV	-4
Input Offset Current	I_{IO}	$I_3 = I_9 = 2$ mA		1	···	0.3	3	μA	···
Input Bias Current	I_{IB}			1	···	13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$			1	···	1.1	···	μV/°C	4
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$ V $I_C = 1$ mA		···	674	774	874	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 6$ V, $I_C = 1$ mA		···	···	-0.9	···	mV/°C	6
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$		···	···	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$		···	15	24	···	V	···
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ μA, $I_E = 0$		···	20	60	···	V	···
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10$ μA, $I_B = 0$, $I_E = 0$		···	20	60	···	V	···
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10$ μA, $I_C = 0$		···	5	7	···	V	···
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 KH3, $R_S = 500\ \Omega$ $I_C = 1$ mA		···	···	1.5	···	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 6$ V, $I_C = 5$ mA		···	···	1.35	···	GH_z	11
Collector-Base Capacitance	C_{CB}	$I_C = 0$	$V_{CB} = 5V$	* **	··· ···	0.28 0.15	··· ···	pF pF	8
Collector-Substrate Capacitance	C_{CI}	$I_C = 0$	$V_{CI} = 5V$		···	1.65	···	pF	8
For Each Differential Amplifier									
Common-Mode Rejection Ratio	CMR	$I_3 = I_9 = 2$ mA		···	···	100	···	dB	···
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	···	75	···	dB	···
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V f = 10 MHz		2	18	22	···	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	···	23	···	dB	···
Noise Figure	NF	$V_{CC} = 12V$	Cascode	3	···	4.6	···	dB	···
Input Admittance	Y_{11}	For Cascode Configuration	Cascode	···	···	1.5 + j 2.45	···	mmho	14, 16, 18
		$I_3 = I_9 = 2$ mA	Diff.Amp.	···	···	0.878 + j 1.3	···		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration	Cascode	···	···	0 - j 0.008	···	mmho	···
		$I_3 = I_9 = 4$mA	Diff.Amp.	···	···	0 - j 0.013	···		···
Forward Transfer Admittance	Y_{21}	(each collector	Cascode	···	···	17.9 - j 30.7	···	mmho	26, 28, 30
		$I_C \simeq 2$mA)	Diff. Amp.	···	···	- 10.5 + j 13	···		27, 29, 31
Output Admittance	Y_{22}		Cascode	···	···	- 0.503 - j 15	···	mmho	20, 22, 24
			Diff.Amp.	···	···	0.071 + j 0.62	···		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

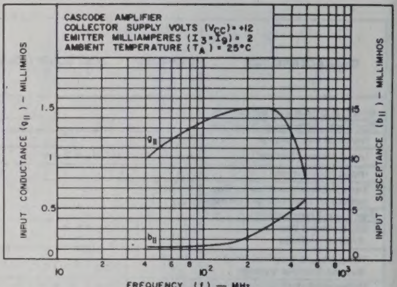


Fig. 14—Input admittance (Y_{11}) vs. frequency.

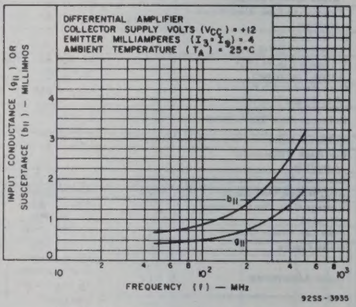


Fig. 15—Input admittance (Y_{11}) vs. frequency.

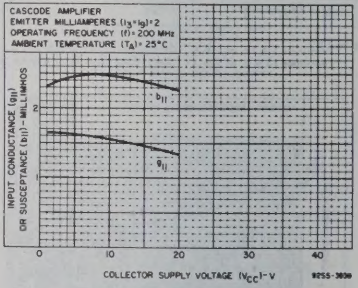


Fig. 16—Input admittance (Y_{11}) vs. collector supply voltage.

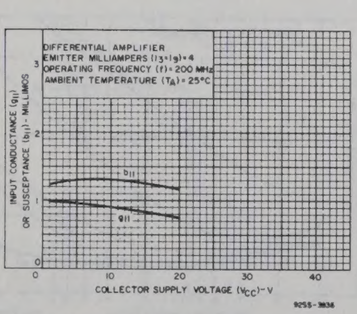


Fig. 17—Input admittance (Y_{11}) vs. collector supply voltage.

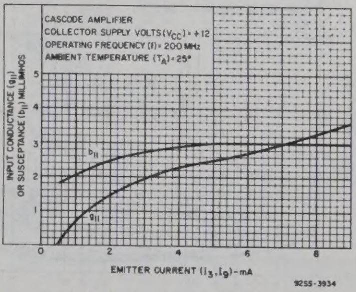


Fig. 18—Input admittance (Y_{11}) vs. emitter current.

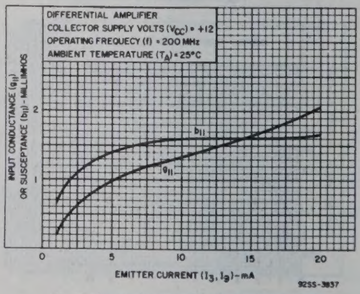


Fig. 19—Input admittance (Y_{11}) vs. emitter current.

Typical Output Admittance Characteristics for CA3049T and CA3102E

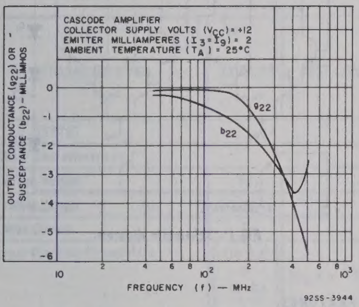


Fig. 20–Output admittance (Y_{22}) vs. frequency.

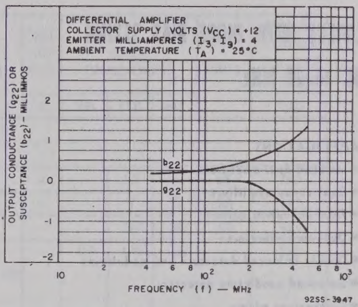


Fig. 21–Output admittance (Y_{22}) vs. frequency.

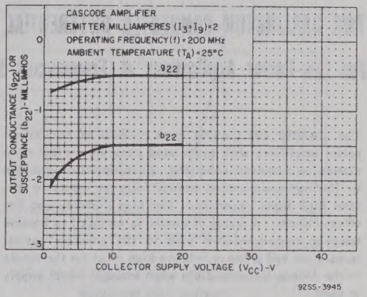


Fig. 22–Output admittance (Y_{22}) vs. collector supply voltage.

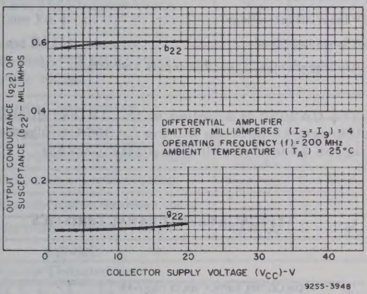


Fig. 23–Output admittance (Y_{22}) vs. collector supply voltage.

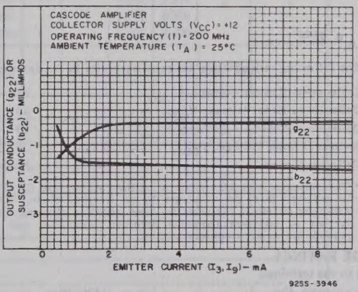


Fig. 24–Output admittance (Y_{22}) vs. emitter current.

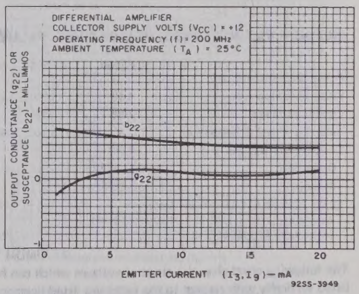


Fig. 25–Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

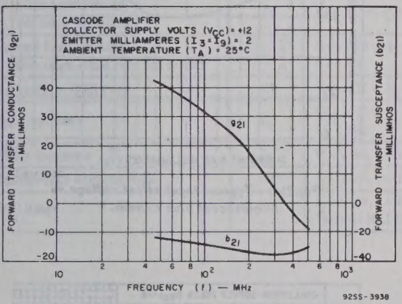


Fig. 26–Forward transfer admittance (Y_{21}) vs. frequency.

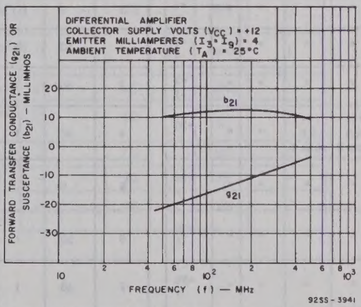


Fig. 27–Forward transfer admittance (Y_{21}) vs. frequency.

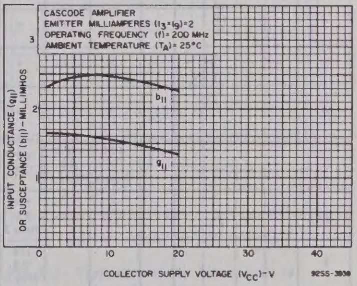


Fig. 28–Forward transfer admittance (Y_{21}) vs. collector supply voltage.

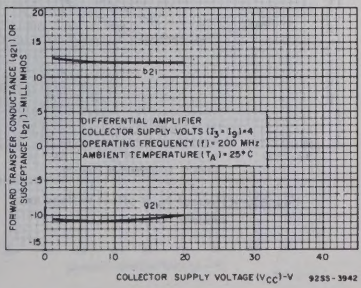


Fig. 29–Forward transfer admittance (Y_{21}) vs. collector supply voltage.

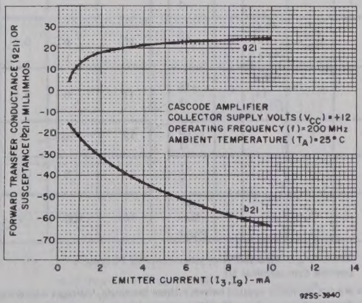


Fig. 30–Forward transfer admittance (Y_{21}) vs. emitter current.

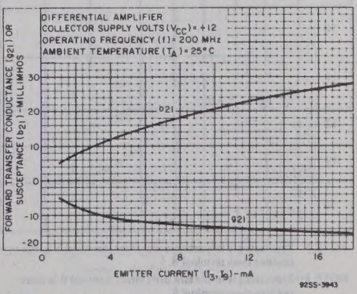


Fig. 31–Forward transfer admittance (Y_{21}) vs. emitter current.

CA3050, CA3051

Dual Differential Amplifiers

TWO DARLINGTON-CONNECTED DIFFERENTIAL AMPLIFIERS WITH DIODE BIAS STRING

For Low-Power Applications at Frequencies from DC to 20 MHz

The CA3050 and CA3051 each consists of two differential amplifiers with associated constant current transistors on a common substrate. Each amplifier is driven by Darlington-connected emitter follower inputs to provide high input impedance, low bias current, and low offset current. A string of diodes is included to provide temperature-compensated bias to the constant current transistors and a low impedance bias point for the inputs to the differential amplifiers when a single power supply is used.

APPLICATIONS

- Matched dual amplifiers
- Dual sense amplifiers
- Dual Schmitt triggers
- Dual multivibrators
- Doubly balanced detectors and modulators
- Balanced quadrature detectors
- Synthesizer mixers
- Product detectors

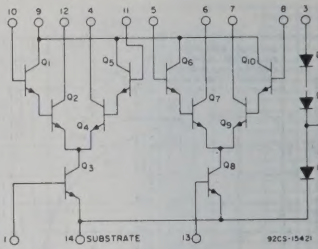


Fig.1 - Schematic diagram.

FEATURES

• Input offset current	70 nA max.
• Input bias current	500 nA max.
• Input offset voltage	5 mV max.
• Input impedance	460 kΩ typ.

- Independently accessible inputs and outputs

The CA3050 is supplied in the 14-lead dual-in-line ceramic package and the CA3051 is supplied in the 14-lead dual-in-line plastic package.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3050	CA3051	
Power Dissipation, P:			
Any one transistor	150	150	mW
Total package	900	750	mW
For T_A > 55°C, Derate at	8	6.67	mW/°C
Temperature Range:			
Operating	-55 to +125		°C
Storage	-65 to +150		°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3050 and CA3051 is isolated from the substrate by an integral diode. *The substrate (terminal 14) must be more negative than all collectors to maintain isolation between transistors and to provide for normal transistor action.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +5 to –2 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	–	*	*	*	*	*	*	*	*	*	*	*	*	+1 -5
2			+5 -2	*	*	*	*	*	*	*	*	*	*	+1 -1
3				*	*	*	*	*	*	*	*	*	*	+3 -1
4					*	*	*	*	*	+14 -2.5 Note 3	+14 -2.5 Note 4	*	*	+20 -1
5						+2.5 -14 Note 1	+2.5 -14 Note 1	+10 -10	+1 -20	*	*	*	*	+16 -1
6							*	+14 -2.5 Note 2	*	*	*	*	*	+20 -1
7								+14 -2.5 Note 2	*	*	*	*	*	+20 -1
8									+1 20	*	*	*	*	+16 -1
9										+20 -1	+20 -1	*	*	+20 -1
10											+10 -10	+2.5 -14 Note 3	*	+16 -1
11												+2.5 -14 Note 4	*	+16 -1
12														+20 -1
13														+1 -5
14														Ref. Sub-strate

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	0.1
2	50	50
3	50	1
4	50	1
5	5	0.1
6	50	1
7	50	1
8	5	0.1
9	50	1
10	5	0.1
11	5	0.1
12	50	1
13	5	0.1
14	100	5

NOTE 1: This rating is important only when terminal 5 is more positive than terminal 8.

NOTE 2: This rating is important only when terminal 8 is more positive than terminal 5.

NOTE 3: This rating is important only when terminal 10 is more positive than terminal 11.

NOTE 4: This rating is important only when terminal 11 is more positive than terminal 10.

*Voltages are not normally applied betwe.n these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

TYPICAL STATIC CHARACTERISTICS

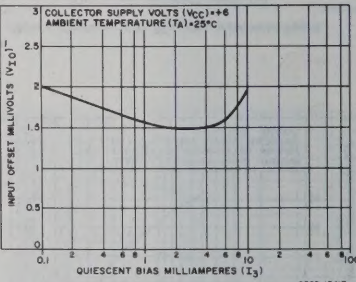


Fig.2(a) - Typical input offset voltage vs quiescent bias current.

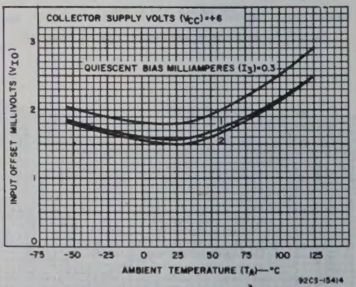


Fig.2(b) - Typical input offset voltage vs ambient temperature.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT	LIMITS CA3050/CA3051			UNITS	TYPICAL CHARACTERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Amplifier Characteristics								
Input Offset Voltage	V_{IO}		–	–	1.5	5	mV	2a,b
Input Offset Current	I_{IO}		–	–	7	70	nA	3a,b
Input Bias Current	I_{IB}		–	–	200	500	nA	4a,b
Quiescent Operating Current Ratio	$\left\lvert\frac{(I_4+I_{12})\ \text{or}\ (I_6+I_7)}{I_3}\right\rvert$	V_{CC} = + 6 V, I_3 = 2 mA	–	0.9	1.00	1.13	–	5a,b
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 50 µA 1 mA 3 mA 10 mA	– – – –	– – – –	0.645 0.725 0.760 0.805	0.700 0.800 0.850 0.900	V	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	–	–	-1.9	–	mV/°C	7
Transistor Characteristics								
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	0.002	100	nA	8
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 µA, I_E = 0	–	20	60	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 µA, I_{CI} = 0	–	20	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 µA, I_C = 0	–	5	7	–	V	–
DYNAMIC								
Transistor Characteristics								
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	–	–	0.78	–	pF	9
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	–	–	0.47	–	pF	9
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	–	–	1.92	–	pF	9
Amplifier Characteristics								
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 5 V, I_C = 3 mA	–	–	600	–	MHz	10
Forward Transadmittance (With single-ended input and output)	$\lvert y_{21}\rvert$	V_{CC} = 10 V, I_3 = 2 mA f = 1 MHz	11	7	9	11	mmho	11
Bandwidth at -3 dB Point	BW	V_{CC} = 10 V, I_3 = 2 mA	11	–	4.3	–	MHz	11
Input Impedance	Z_I	V_{CC} = 10 V, I_3 = 2 mA f = 1 KHz	12	–	460	–	kΩ	12
Output Impedance	Z_O	I_3 = 2 mA, f = 1 KHz	13	–	170	–	kΩ	13
Common-Mode Rejection Ratio	CMR	I_3 = 2 mA, f = 1 KHz	–	–	65	–	dB	–
AGC Range	AGC	I_3 = 2 mA, f = 1 KHz Terminal No.3 Grounded	11	–	60	–	dB	–

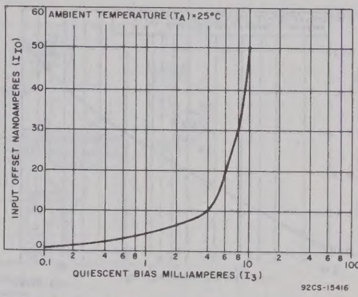


Fig.3(a) - Typical input offset current vs quiescent bias current.

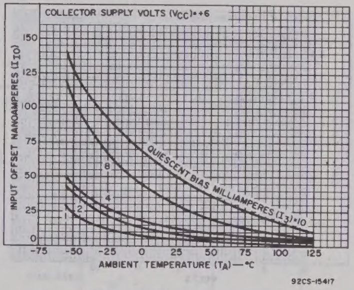


Fig.3(b) - Typical input offset current vs ambient temperature.

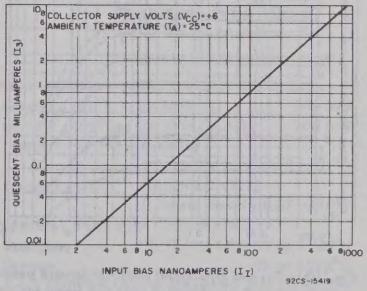


Fig.4(a) - Typical quiescent bias current vs input bias current.

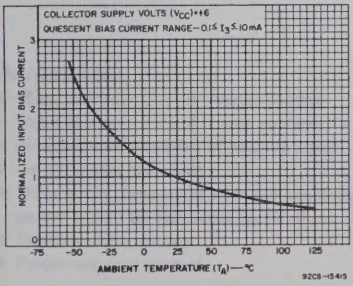


Fig.4(b) - Typical normalized input bias current vs ambient temperature.

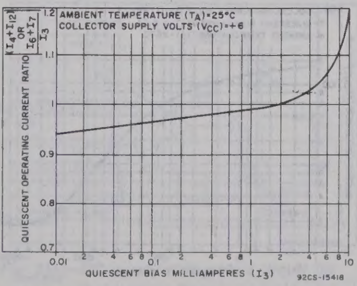


Fig.5(a) - Typical quiescent operating current ratio vs quiescent bias current.

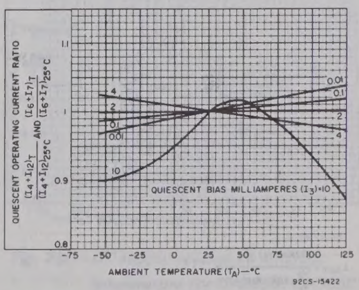


Fig.5(b) - Typical quiescent operating current ratio vs ambient temperature.

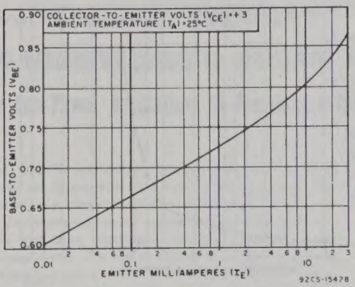


Fig.6 - Typical static base-to-emitter voltage characteristic vs emitter current for all transistors and forward diode voltage drops.

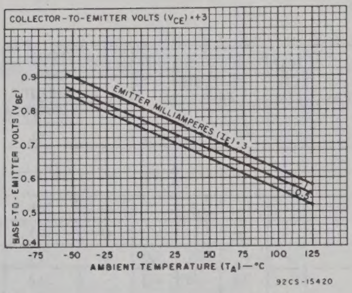


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

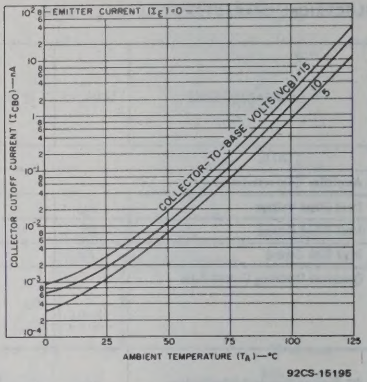


Fig.8 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

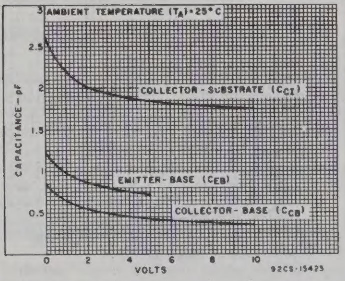


Fig.9 - Typical capacitance for each transistor.

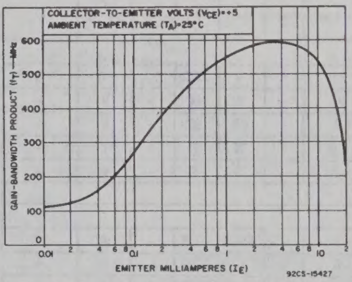
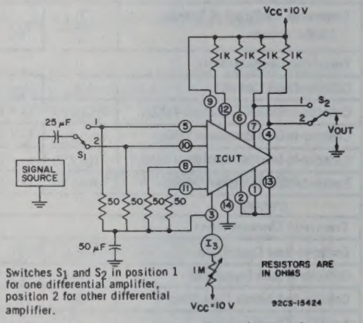


Fig.10 - Typical gain-bandwidth product (f_T) for each transistor vs emitter current.



Switches S_1 and S_2 in position 1 for one differential amplifier, position 2 for other differential amplifier.

Fig.11(a) - Test circuit for forward transadmittance, -3 dB bandwidth, and AGC range.

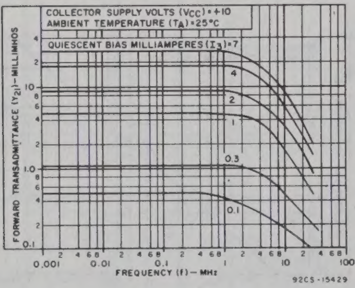
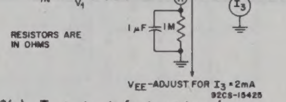


Fig.11(b) - Typical differential amplifier forward transadmittance with single-ended output vs frequency.



$$Z_{IN} = \frac{V_{IN} - V_1}{V_1} (10^6)$$

Fig.12(a) - Test circuit for input impedance.

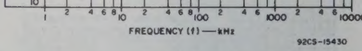
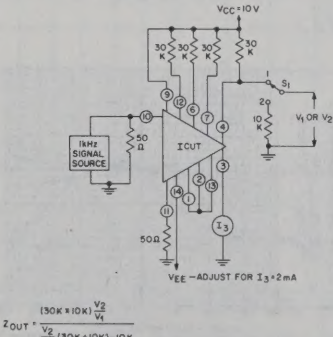


Fig.12(b) - Typical input impedance vs frequency with output short-circuited.



$$Z_{OUT} = \frac{(30K \times 10K)\frac{V_2}{V_1}}{\frac{V_2}{V_1}(30K + 10K) - 10K}$$

Fig.13(a) - Test circuit for output impedance.

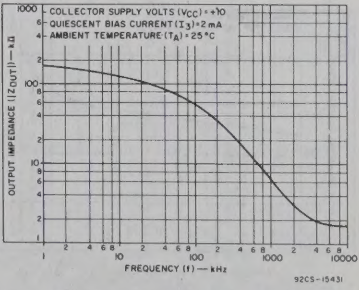


Fig.13(b) - Typical output impedance vs frequency with input short-circuited.

CA3058, CA3059, CA3079

Zero-Voltage Switches

For 50/60 and 400 Hz Thyristor Control Applications

The RCA-CA3058, CA3059, and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see Fig. 1) as follows:

1. Limiter-Power Supply—Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier—Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector—Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit—Provides high-current pulses to the gate of the power controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (see Fig. 1):

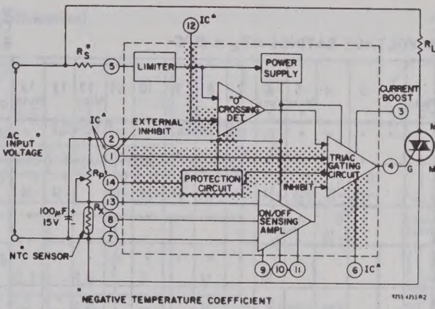
1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

For an explanation of these functions see Operating Considerations. For detailed application information, see companion Application Note, ICAN-6182, "Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)".

The CA3058 is supplied in a hermetic 14-lead dual-in-line ceramic package. Types CA3059 and CA3079 are supplied in 14-lead dual-in-line plastic packages.

Applications:

- **Relay control**
- **Valve control**
- **Synchronous switching of flashing lights**
- **On-off motor switching**
- **Differential comparator with self-contained power supply for industrial applications**
- **Photosensitive control**
- **Power one-shot control**
- **Heater control**
- **Lamp control**



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE:

Circuitry, within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal Connection - - DO NOT USE (Terminal Restriction applies only to CA3079).

Fig. 1—Functional block diagram of CA3058, CA3059, and CA3079.

Features	CA3058	CA3059	CA3079
■ 24V, 120V, 208/230V, 277V at 50 60, or 400 Hz operation	√	√	√
■ Differential Input	√	√	√
■ Low Balance Input Current (max.) -µA	1	1	2
■ Built-in Protection Circuit for opened or shorted sensor (Term. 14)	√	√	
■ Sensor Range (R_X) - kΩ	2 to 100	2 to 100	2 to 50
■ DC Mode (Term 12)	√	√	
■ External Trigger (Term. 6)	√	√	
■ External Inhibit (Term. 1)	√	√	
■ DC Supply Volts (max.)	14	14	10
■ Operating Temperature Range - °C		−55 to +125	

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 7):
CA3058, CA3059 .... 14 V
CA3079 .... 10 V
DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 8):
CA3058, CA3059 .... 14 V
CA3079 .... 10 V
PEAK SUPPLY CURRENT (TERMS. 5 AND 7)
.... ±50 mA
OUTPUT PULSE CURRENT (TERM. 4)
.... 150 mA

POWER DISSIPATION:
Up to T_A=75°C – CA3058 .... 700 mW
Up to T_A=55°C – CA3059,CA3079 ... 700 mW
Above T_A=75°C – CA3058
.... Derate Linearly 8 mW/°C
Above T_A=55°C – CA3059,CA3079
.... Derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating .... −55 to +125°C
Storage .... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ...... +265°C

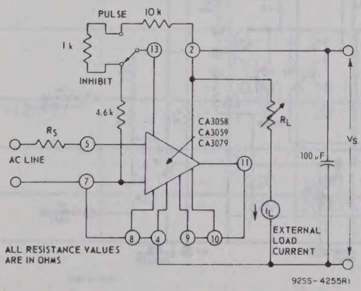


Fig. 2(a)—DC supply voltage test circuit for CA3058, CA3059, and CA3079.

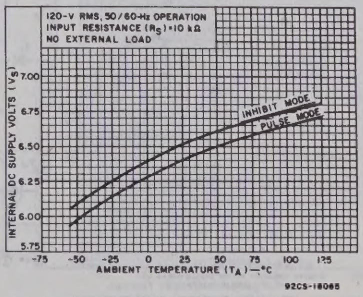


Fig. 2(b)—DC supply voltage vs. ambient temperature for CA3058, CA3059 and CA3079.

MAXIMUM VOLTAGE RATINGS at T_A = 25°C | **MAXIMUM CURRENT RATINGS**

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3	I_{IN} mA	I_{OUT} mA
1 Note 3		*	*	*	*	15 0	10 −2	*	*	*	*	*	*	*	10	0.1
2			0 −15	0 −15	2 −14	0 −14	0▲ −14	0▲ −14	0 −14	0 −14	0 −14	*	0 −14	0 −14	150	10
3				0 −15	*	*	*	*	*	*	*	*	*	*	*	*
4					*	2 −10	*	*	*	*	*	*	*	*	0.1	150
5 Note 1						*	7 −7	*	*	*	*	*	*	*	50	10
6 Note 3							14 0	*	*	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 −2.5	14 0	6 −6	*	*
8									10 0	*	*	*	*	*	0.1	2
9										*	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12 Note 3													*	*	50	50
13														*	*	*
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to −10 volts.

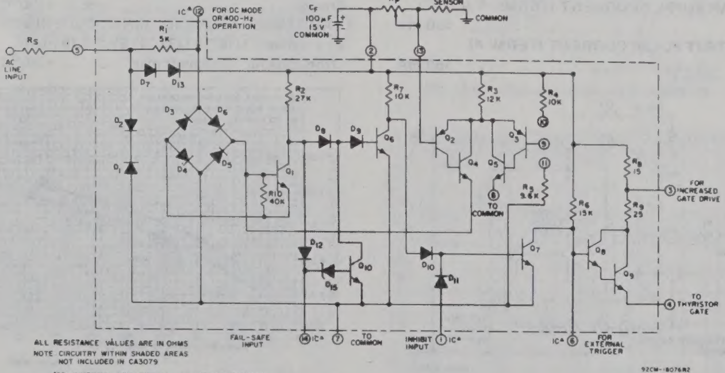
Note 1 – Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2 mA.

Note 3 – For the CA3079 indicated terminal is internally connected and, therefore, should not be used.

▲For CA3079 (0 to −10 V).

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.



ALL RESISTANCE VALUES ARE IN OHMS
NOTE CIRCUITRY WITHIN SHADED AREAS NOT INCLUDED IN CA3079
▲IC = INTERNAL CONNECTION – DO NOT USE (TERMINAL RESTRICTION APPLIES ONLY TO CA3079)

Fig. 4– Schematic diagram of CA3058, CA3059, and CA3079.

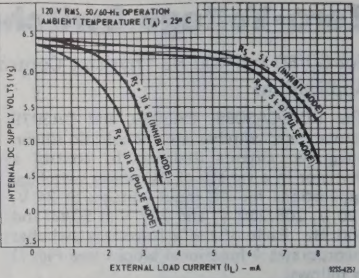


Fig. 2(c)–DC supply voltage vs. external load –current for CA3058, CA3059, and CA3079.

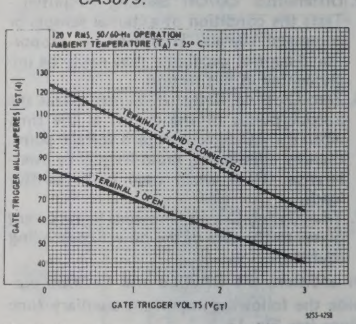
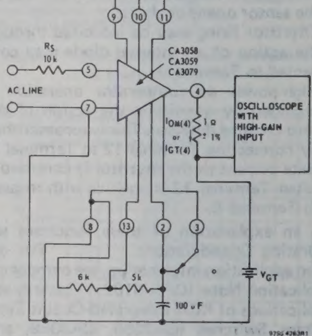


Fig. 3– Gate trigger current vs. gate trigger voltage for CA3058, CA3059, and CA3079.



ALL RESISTANCE VALUES ARE IN OHMS

Fig. 5(a)–Peak output (pulsed) and gate trigger current with internal power supply test circuit for CA3058, CA3059, and CA3079.

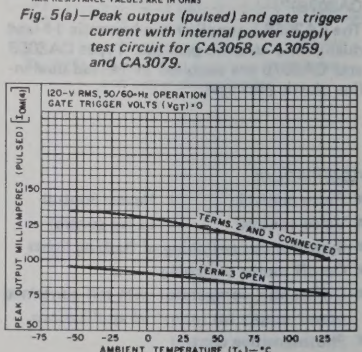


Fig. 5(b)–Peak output current (pulsed) vs. ambient temperature for CA3058, CA3059, and CA3079.

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS $T_A = 25^oC$ (Unless Indicated Otherwise)	LIMITS			UNITS
		Min.	Typ.	Max.	
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
DC Supply Voltage, V_S Inhibit Mode At 50/60 Hz	$R_S = 8\ k\Omega$, $I_L = 0$	6.1	6.5	7	V
At 400 Hz	$R_S = 10\ k\Omega$, $I_L = 0$	–	6.8	–	V
At 50/60 Hz	$R_S = 5\ k\Omega$, $I_L = 2\ mA$	–	6.4	–	V
Pulse Mode At 50/60 Hz	$R_S = 8\ k\Omega$, $I_L = 0$	6	6.4	7	V
At 400 Hz	$R_S = 10\ k\Omega$, $I_L = 0$	–	6.7	–	V
At 50/60 Hz	$R_S = 5\ k\Omega$, $I_L = 2\ mA$	–	6.3	–	V
At 50/60 Hz (CA3058) *See Fig. 2*	$R_S = 8\ k\Omega$, $I_L = 0$ $T_A = -55$ to $+125^oC$	5.5	–	7.5	V
Gate Trigger Current, I_{GT} (4) *See Figs. 3, 5(a)*	Terms. 3 and 2 connected, $V_{GT} = 1\ V$	–	105	–	mA
Peak Output Current (Pulsed), I_{OM} (4) With Internal Power Supply	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	–	mA
	Terms. 3 and 2 connected, Gate Trigger Voltage (V_{GT})=0	90	124	–	mA
With External Power Supply	Term. 3 open, V^+=12 V, V_{GT}=0	–	170	–	mA
	Terms. 3 and 2 connected, V^+=12 V, V_{GT} = 0	–	240	–	mA
See Figs. 5, 6					
Inhibit Input Ratio, V_9/V_2 All Types	Voltage Ratio of Term. 9 to 2	0.465	0.485	0.520	–
CA3058	$T_A = -55$ to $+125^oC$	0.450	–	0.520	–
See Fig. 7					
Total Gate Pulse Duration:* For positive dv/dt, t_P 50-60 Hz	$C_{EXT} = 0$	70	100	140	µs
400 Hz	$C_{EXT} = 0$, $R_{EXT} = \infty$	–	12	–	µs
For negative dv/dt, t_N 50-60 Hz	$C_{EXT} = 0$	70	100	140	µs
400 Hz	$C_{EXT} = 0$, $R_{EXT} = \infty$	–	10	–	µs
See Fig. 8					
Pulse Duration After Zero Crossing (50-60 Hz): For positive dv/dt, t_{P1}	$C_{EXT} = 0$ $R_{EXT} = \infty$	–	50	–	µs
For negative dv/dt, t_{N1}		–	60	–	µs
See Fig. 8					
Output Leakage Current, I_4 Inhibit Mode: All Types		–	0.001	10	µA
CA3058	$T_A = -55$ to $+125^oC$	–	–	20	µA
See Fig. 9					
Input Bias Current, I_I CA3058, CA3059		–	220	1000	nA
CA3079		–	220	2000	nA
See Fig. 10					

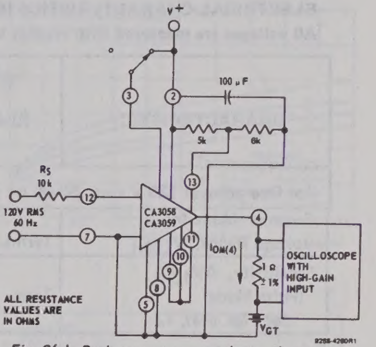


Fig. 6(a)—Peak output current (pulsed) with external power supply test circuit for CA3058 and CA3059.

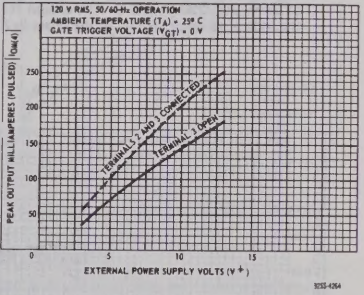


Fig. 6(b)—Peak output current (pulsed) vs. external power supply voltage for CA3058 and CA3059.

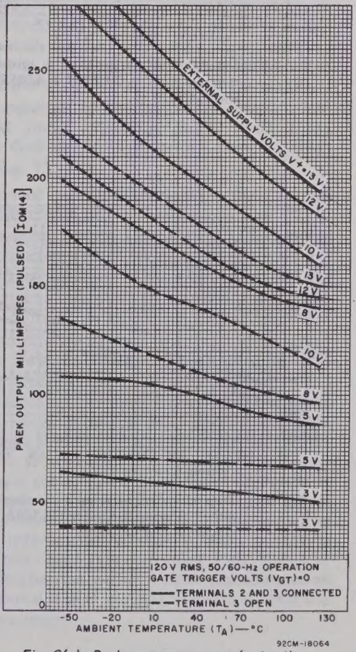


Fig. 6(c)—Peak output current (pulsed) vs. ambient temperature for CA3058 and CA3059.

CA3058, CA3059, CA3079

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise) (Cont'd)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS $T_A = 25^oC$ (Unless Indicated Otherwise)	LIMITS			UNITS
		Min.	Typ.	Max.	
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
Common-Mode Input Voltage Range, V_{CMR}	Terms. 9 and 13 connected	–	1.5 to 5	–	V
Sensitivity, $\Delta V_{13}^{\neq}$ (Pulse Mode) *See Figs. 5(a), 12*	Term. 12 open	–	6	–	mV

≠ Required voltage change at Term. 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

* Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 8(b).

● The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in Fig. 1, for the specified input voltage.

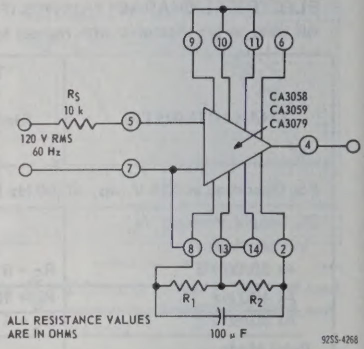


Fig. 7(a)—Input inhibit voltage ratio test circuit for CA3058, CA3059, and CA3079.

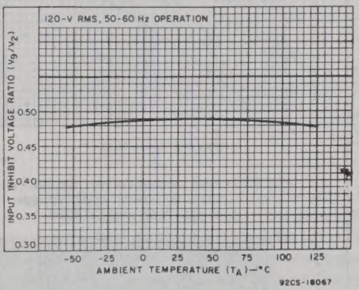


Fig. 7(b)—Input inhibit voltage ratio vs. ambient temperature for CA3058, CA3059, and CA3079.

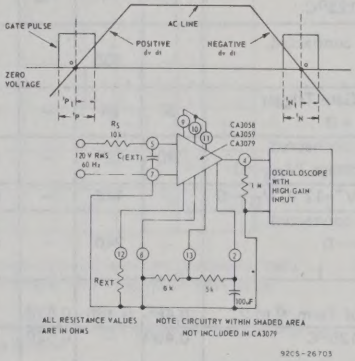


Fig. 8(a)—Gate pulse duration test circuit with associated waveform for CA3058, CA3059, and CA3079.

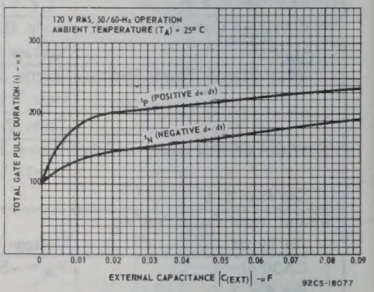


Fig. 8(b)—Total gate pulse duration vs. external capacitance for CA3058, CA3059, and CA3079.

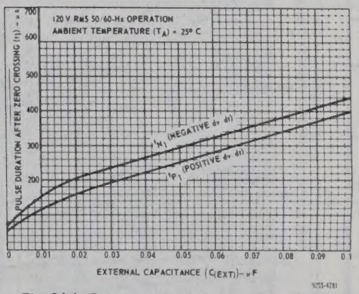


Fig. 8(c)—Pulse duration after zero crossing vs. external capacitance for CA3058, CA3059, and CA3079.

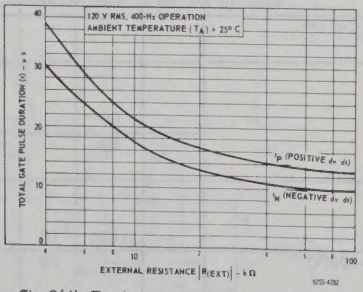


Fig. 8(d)—Total gate pulse duration vs. external resistance for CA3058 and CA3059.

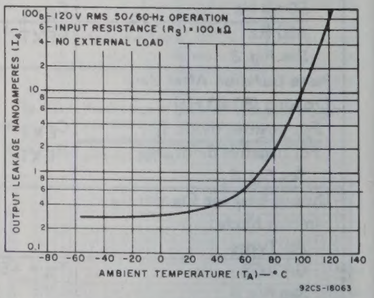


Fig. 9—Output leakage current (inhibit mode) vs. ambient temperature for CA3058, CA3059, and CA3079.

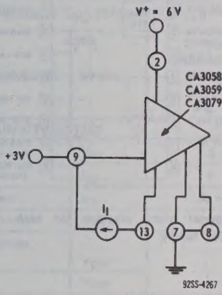


Fig. 10—Input bias current test circuit for CA3058, CA3059, and CA3079.

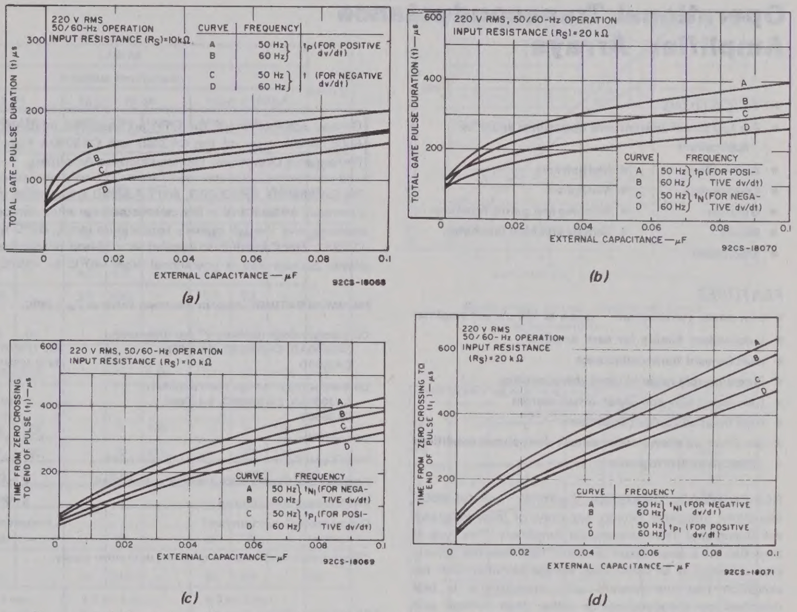


Fig. 11—Relative pulse width and location of zero crossing for 220-volt operation for CA3058, CA3059, and CA3079.

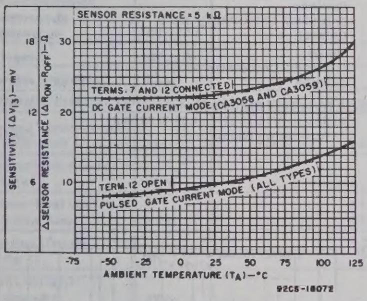


Fig. 12—Sensitivity vs. ambient temperature for CA3058, CA3059, and CA3079.

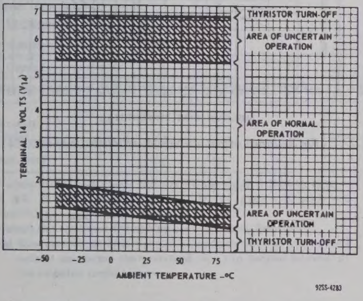


Fig. 13—Operating regions for built-in protection circuit for CA3058 and CA3059.

OPERATING CONSIDERATIONS

Power Supply Considerations for CA3058, CA3059, and CA3079

The CA3058, CA3059, and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3(b) and 3(c).

Power Supply Considerations for CA3058 and CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5(a).

Operation of Built-in Protection for the CA3058, CA3059

A special feature of the CA3058 and CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2 mA with a 5 kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2 kΩ and 100 kΩ.
3. The ratio of R_X to R_P, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

External Inhibit Function for the CA3058 and CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10 µA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3058 and CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

CA3060, CA3060A Types

Operational Transconductance Amplifier Arrays

APPLICATIONS

- For low power conventional operational amplifier applications
- Active filters
- Comparators
- Gyrators
- Mixers
- Modulators
- Multiplexers
- Multipliers
- Strobing and gating functions
- Sample and hold functions

FEATURES

- Low power consumption — as low as 100 μW per amplifier
- Independent biasing for each amplifier
- High forward transconductance
- Programmable range of input characteristics
- Low input bias and input offset current
- High input and output impedance
- No effect on device under output short-circuit conditions
- Zener diode bias regulator

RCA-CA3060AD, CA3060BD, CA3060D, and CA3060E, monolithic integrated circuits, are arrays of three independent Operational Transconductance Amplifiers. This type of amplifier is a new circuit concept that has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, $g_m R_L$). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filters.

The three amplifiers in the CA3060 family are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific applications. The electrical characteristics of each amplifier are a function of the amplifier bias current (I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of non-linear applications such as mixers, multipliers, and modulators.

In addition, the types in the CA3060 family incorporate a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

Generic applications of the OTA are described in ICAN-6668, Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers.

The CA3060AD, CA3060BD, and CA3060D are supplied in a hermetic 16-lead dual-in-line ceramic package which can be operated over the full military temperature range, -55°C to +125°C. The CA3060E is supplied in a 16-lead dual-in-line plastic package and is operational from -40°C to +85°C.

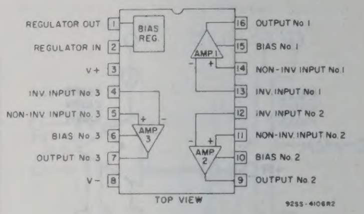


Fig.1—Functional block diagram for each type in the CA3060 family.

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

DC Supply Voltage (between V+ and V− terminals):	
CA3060AD, CA3060BD, CA3060E	36V (±18V)
CA3060D	14 V (±7V)
Differential Input Voltage (each amplifier):	
CA3060AD, CA3060BD, CA3060E	±5V
CA3060D	±5V
DC Input Voltage	V^+ to V^-
Input Signal Current (each amplifier of each type)	±1 mA
Amplifier Bias Current (each amplifier of each type)	2 mA
Bias Regulator Input Current	-5 mA
Output Short-Circuit Duration*	No limitation
Device Dissipation:	
Total Package of each type up to T_A = 75°C	490 mW
Above T_A = 75°C	Derate linearly 6.67 mW/°C
Temperature Range:	
Operating —	
CA3060AD, CA3060BD, CA3060D	-55 to +125°C
CA3060E	-40 to +85°C
Storage —	
CA3060AD, CA3060BD, CA3060D, CA3060E	-65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max	+300°C

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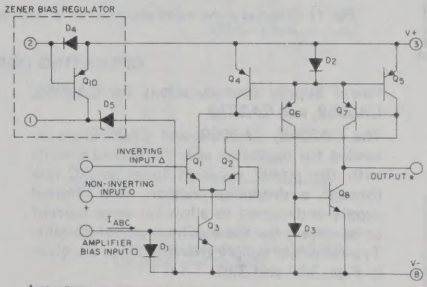
*Short circuit may be applied to ground or to either supply.



Δ INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 13, 12 AND 4, RESPECTIVELY

○ NON-INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS TERMINAL Nos. 14, 11, AND 5, RESPECTIVELY

• OUTPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 16, 9, AND 7, RESPECTIVELY

□ AMPLIFIER BIAS CURRENT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 15, 10, AND 6, RESPECTIVELY

92CS-15860R1

Fig.2—Simplified schematic diagram showing bias regulator and one operational transconductance amplifier for each type of the CA3060 family.

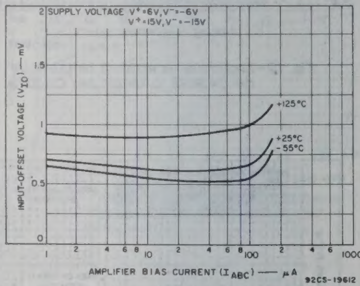


Fig.3—Input offset voltage vs. amplifier bias current.

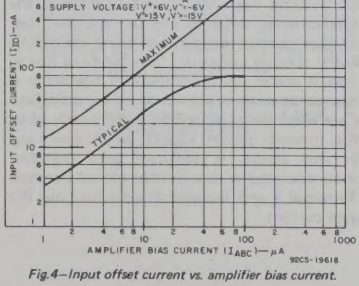


Fig.4—Input offset current vs. amplifier bias current.

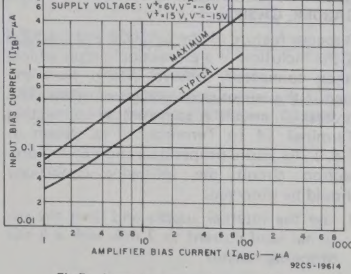


Fig.5a—Input bias current vs. amplifier bias current

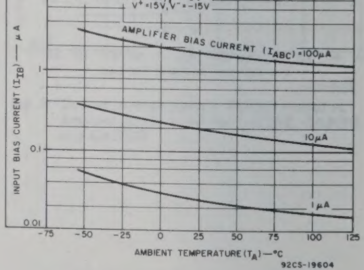


Fig.5b—Input bias current vs. ambient temperature.

CA3060, CA3060A Types

ELECTRICAL CHARACTERISTICS (CA3060D)

For each amplifier at $T_A = 25^oC$, $V^+ = 6$ V, $V^- = -6$ V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVES Fig.	LIMITS									UNITS
			Amplifier Bias Current									
			$I_{ABC} = 1\ \mu A$			$I_{ABC} = 10\ \mu A$			$I_{ABC} = 100\ \mu A$			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a, b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a, b	1.3	2.3	–	15	26	–	150	240	–	µA
Peak Output Voltage: Positive	V_{OM^+}	7	4.6	5	–	4.5	4.8	–	4.5	4.7	–	V
Negative	V_{OM^-}		5.8	5.95	–	5.8	5.95	–	5.7	5.9	–	
Amplifier Supply Current (each amplifier)	I_A	8a, b	–	8.5	14	–	85	120	–	850	1200	µA
Power Consumption (each amplifier)	P	–	–	0.10	0.17	–	1	1.45	–	10	14.5	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	120	–	2	120	–	2	120	µV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	20	120	–	20	120	–	30	120	
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a, b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–	4.4 to -5.1 min. 4.7 to -5.3 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			V
Slew Rate (Test ckt., Fig. 13	SR		–	0.1	–	–	1	–	–	8	–	V/µs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at $T_A = 25^oC$, $I_2 = 0.1$ mA)												
						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature-Coefficient; -2.2 mV/°C (at $V_{ABC} = 0.54$ V, $I_{ABC} = 1\ \mu A$; -2.1 mV/°C (at $V_{ABC} = 0.060$ V, $I_{ABC} = 10\ \mu A$); -1.9 mV/°C (at $V_{ABC} = 0.66$ V, $I_{ABC} = 100\ \mu A$)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test —

V^+ is reduced to 5 volts for V^+ sensitivity

V^- is reduced to -5 volts for V^- sensitivity

$$\text{(b) } V^+ \text{ sensitivity in } \mu V/V = \frac{\text{Voffset - Voffset for +5 V and -6 V supplies}}{\text{1 volt}}$$

$$V^- \text{ sensitivity in } \mu V/V = \frac{\text{Voffset - Voffset for -5 V and +6 V supplies}}{\text{1 volt}}$$

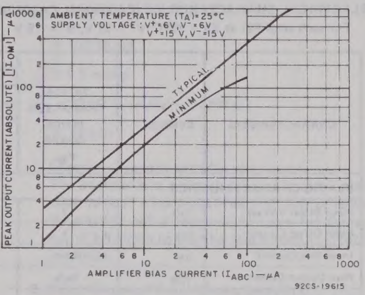


Fig.6a—Peak output current vs. amplifier bias current.

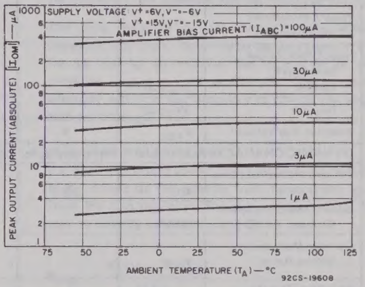


Fig.6b—Peak output current vs. ambient temperature.

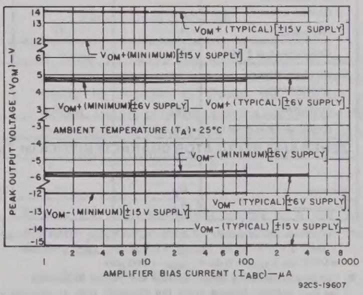


Fig.7—Peak output voltage vs. amplifier bias current.

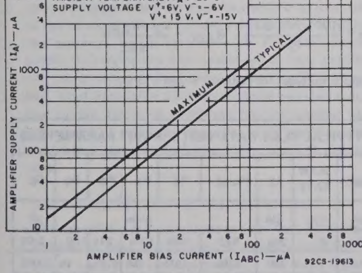


Fig.8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

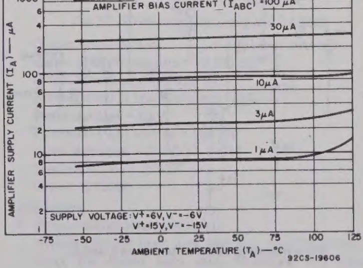


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

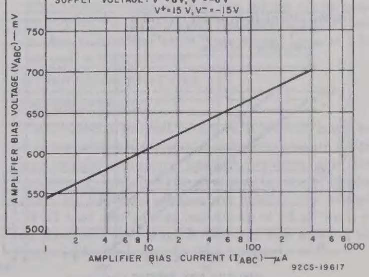


Fig.9—Amplifier bias voltage vs. amplifier bias current.

CA3060, CA3060A Types

ELECTRICAL CHARACTERISTICS (CA3060AD, CA3060BD, CA3060E)
For each amplifier at T_A = 25°C, V^+ = 15 V, V^- = -15 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVE Fig.	LIMITS									UNITS
			Amplifier Bias Current									
			I_{ABC} = 1 µA			I_{ABC} = 10 µA			I_{ABC} = 100 µA			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
			CA3060BD						CA3060AD CA3060BD CA3060E			
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a,b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a,b	1.3	2.3		15	26	–	150	240	–	µA
Peak Output Voltage: Positive	V_{OM^+}	7	12	13.6	–	12	13.6	–	12	13.6	–	V
Negative	V_{OM^-}		12	14.7	–	12	14.7	–	12	14.7	–	
Amplifier Supply Current (each amplifier)	I_A	8a,b	–	8.5	14	–	85	120	–	850	1200	µA
Power Consumption (each amplifier)	P	–	–	0.26	0.42	–	2.6	3.6	–	26	36	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	150	–	2	150	–	2	150	µV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	20	150	–	20	150	–	30	150	
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a,b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110		70	110	–	70	90	–	dB
Common-Mode Input Voltage Range	V_{ICR}	–	+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			V
Slew Rate (Test ckt., Fig. 13)	SR		–	0.1	–	–	1	–	–	8	–	V/µs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25°C, I_2 = 0.1 mA)												
						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature-Coefficient: -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 µA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 µA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 µA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test ...

V^+ is reduced to 13 volts for V^+ sensitivity
V^- is reduced to −13 volts for V^- sensitivity

(b) V^+ sensitivity in µV/V = $\frac{V_{offset} - V_{offset}\text{ for +13 V and −15 V supplies}}{1\text{ volt}}$

V^- sensitivity in µV/V = $\frac{V_{offset} - V_{offset}\text{ for −13 V and +15 V supplies}}{1\text{ volt}}$

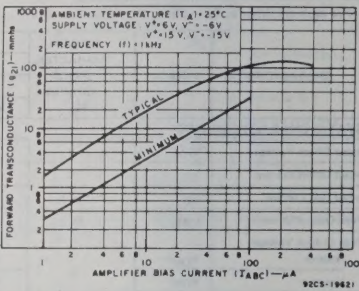


Fig. 10a—Forward transconductance vs. amplifier bias current.

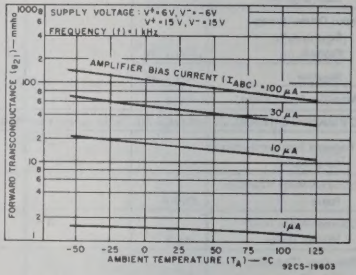


Fig. 10b—Forward transconductance vs. ambient temperature.

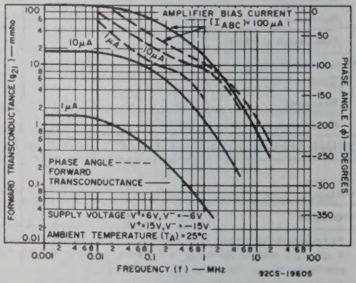


Fig. 11—Forward transconductance vs. frequency.

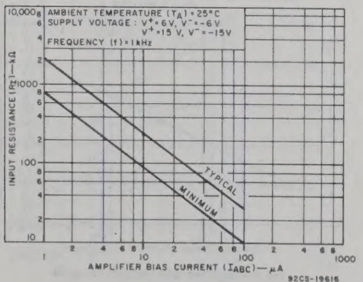
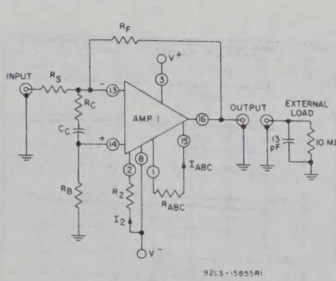


Fig. 12—Input resistance vs. amplifier bias current.



V_Z is measured between terminals 1 and 8.

V_{ABC} is measured between terminals 15 and 8.

$$R_Z = \frac{[(V^+)-(V^-)-0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: for both ±6 V and ±15 V.

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS								
I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
µA	V/µs	µA	ohms					µF
100	8	200	62 k	100k	100k	51k	100	0.02
10	1	200	620k	1M	1M	510k	1k	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

Fig. 13—Slew rate test circuit for amplifier No. 1 of CA3060.

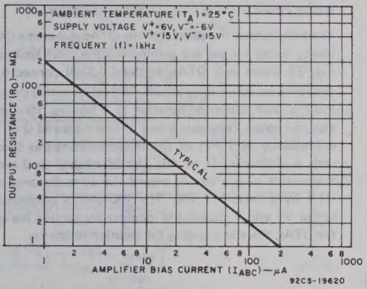


Fig.14—Output resistance vs. amplifier bias current.

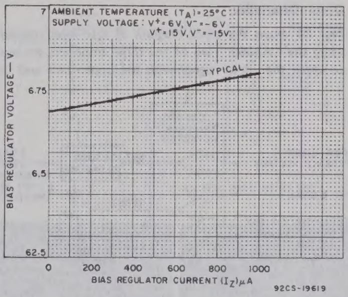


Fig.15—Bias regulator voltage vs. bias regulator current.

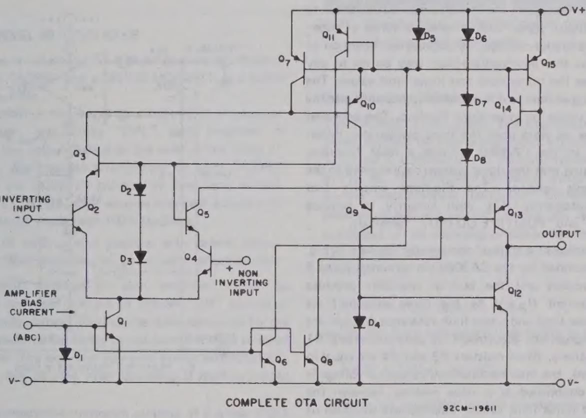


Fig.16 – Complete schematic diagram showing one of the three operational transconductance amplifiers.

OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

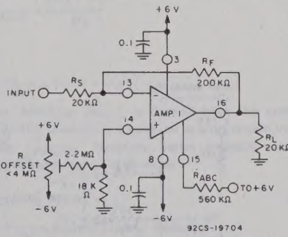


Fig.17–20-dB amplifier using the CA3060.

Circuit Requirements
Closed loop voltage gain = 10 (20 dB)
Offset voltage adjustable to zero
Current drain as low as possible
Supply voltage = ±6 V
Maximum input voltage = ±50 mV
Input resistance = 20 kΩ
Load resistance = 20 kΩ
Device: CA3060

Calculation

1. Required transconductance g_{21}.
   Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

   $$g_{21} = A_{OL}/R_L$$
   $$= 100/18\ k\Omega$$
   $$\cong 5.5\ \text{mmho}$$

   (R_L = 20 kΩ in parallel with 200 kΩ $\cong$ 18 kΩ)

2. Selection of suitable amplifier bias current.
   The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5 mmho an amplifier bias current I_{ABC} of 20 μA is suitable.

3. Determination of Output Swing Capability.
   For a loop gain of 10 the output swing is ±0.5 V and the peak load current 25 μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20 kΩ than R_F = 200 kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200 kΩ = 2.5 μA.

   The total amplifier current output requirements are, therefore, ±27.5 μA. Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20 μA the amplifier output current is ±40 μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. Calculation of bias resistance.
   For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

   $$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

   $$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

   $$= 568.5\ k\Omega \text{ or } \cong 560\ k\Omega$$

5. Calculation of offset adjustment circuit.
   In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

   $$\text{i.e.}\quad \frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18\ k\Omega$$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e. $200 \times 10^{-9} \times 18 \times 10^3$ volts), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV = ±8.6 mV

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48\ \mu A$$

With a supply voltage of ±6 V, this current can be provided by a 10 MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 MΩ was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-kΩ load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-kΩ 15-pF load modifies the frequency characteristic.

CA3060, CA3060A Types

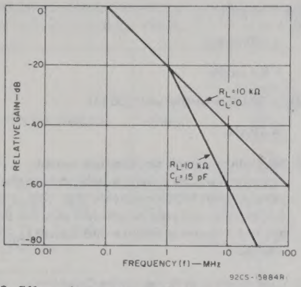


Fig.18—Effect of capacitive loading on frequency response.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (see Fig. 6a), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore,

$$SR = dV/dt = I_{OM}/C_L$$

where C_L is the total load capacitance including strays. This relationship is shown graphically in Fig. 19. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13 pF.

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Fig. 13. The values given in Fig. 13 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13 pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

APPLICATIONS

Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op-amps, and thus, are well suited for most op-amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

TRI-LEVEL COMPARATOR

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper or lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

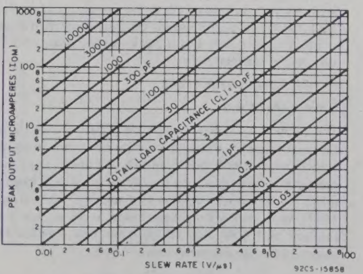


Fig.19—Effect of load capacitance on slew rate.

Circuit Description

Fig. 20 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper-limit and lower-limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate-limit reference voltage. By appropriate selection or resistance ratios this intermediate-limit may be set to any voltage between the upper-limit and lower-limit values. The output of the upper-limit and lower-limit comparator sets the corresponding upper or lower-limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate-limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate-limit selected. The flip-flops employ two CA3086 transistor-array IC's, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.

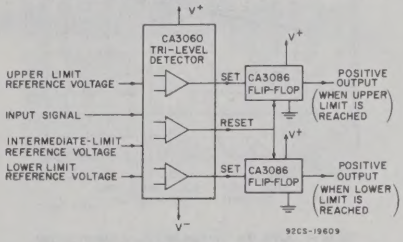


Fig.20—Functional block diagram of a tri-level comparator.

The circuit diagram of a tri-level comparator appears in Fig. 21. Power is provided for the CA3060 via terminals 3 and 8 by ±6-volt supplies and the built-in regulator provides amplifier-bias-current (I_{ABC}) to the three amplifiers via terminal 1. Lower-limit and upper-limit reference voltages are selected by appropriate adjustment of potentiometers R1 and R2, respectively. When resistors R3 and R4 are equal in value (as shown), the intermediate-limit reference voltage is automatically established at a value midway between the lower-limit and upper-limit values. Appropriate variation of resistors R3 and R4 permits selection of other values of intermediate-limit voltages. Input signal (E_S) is applied to the three comparators via terminals 5, 12, and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate-value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Fig. 21 are 5-V, 25-mA lamps.

Active Filters — Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Fig. 22 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3-μF capacitor function as a floating 10-kilohenry inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1 Hz) of this inductor compares favorably with a calculated Q of 16. The 20-kilohm to 2-megohm attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100-kilohm potentiometer, across V+ and V−, tunes the inductor by varying the g_{21} of the OTAs, thereby changing the gyration resistance.

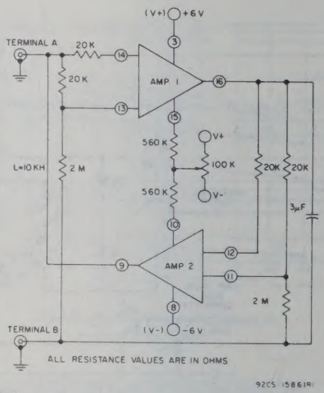


Fig.22—Two operational transconductance amplifiers of the CA3060 connected as a gyrator in an active filter circuit.

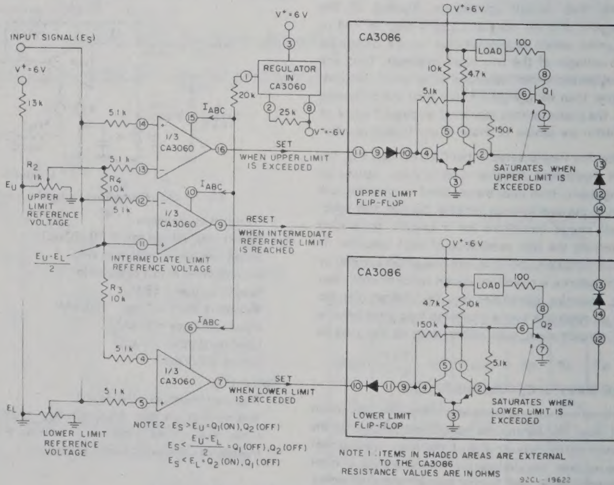

INPUT SIGNAL (E_S)
V+=6V
13k
V+=6V
REGULATOR
IN
CA3060
20k
25k
V−=-6V
I_{ABC}
5.1k
1/3
CA3060
SET
WHEN UPPER LIMIT IS EXCEEDED
R2
1k
E_U
UPPER LIMIT REFERENCE VOLTAGE
R4
10k
5.1k
1/3
CA3060
RESET
WHEN INTERMEDIATE REFERENCE LIMIT IS REACHED
$\frac{E_U - E_L}{2}$
INTERMEDIATE LIMIT REFERENCE VOLTAGE
R3
10k
5.1k
1/3
CA3060
SET
WHEN LOWER LIMIT IS EXCEEDED
EL
LOWER LIMIT REFERENCE VOLTAGE
CA3086
V+=6V
LOAD
100
10k
4.7k
5.1k
Q1
150k
SATURATES WHEN UPPER LIMIT IS EXCEEDED
UPPER LIMIT FLIP-FLOP
CA3086
V+=6V
LOAD
100
4.7k
10k
150k
Q2
5.1k
SATURATES WHEN LOWER LIMIT IS EXCEEDED
LOWER LIMIT FLIP-FLOP
NOTE 2 $E_S > E_U$ = Q_1(ON), Q_2(OFF)
$E_S < \frac{E_U - E_L}{2}$ = Q_1(OFF), Q_2(OFF)
$E_S < E_L$ = Q_2(ON), Q_1(OFF)
NOTE 1 : ITEMS IN SHADED AREAS ARE EXTERNAL TO THE CA3086
RESISTANCE VALUES ARE IN OHMS
92CL-19622

Fig.21—Tri-level comparator circuit.

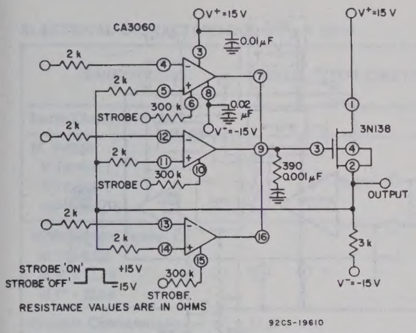


Fig.23—Three-channel multiplexer.

THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N138 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at ±6 volts is also possible with several minor changes. First, the resistance in series with amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100 µA of strobe–"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

The phase compensation network consists of a single 390Ω resistor and a 1000-pF capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is 0.3 volts/µsec. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

NON LINEAR APPLICATIONS

AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to V⁻.

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.

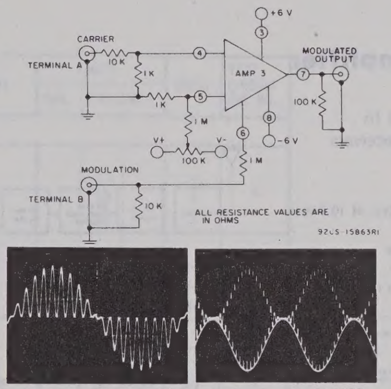


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

Four-Quadrant Multiplier

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_O(1) = [-V_X]\ [g_{21}(1)] \qquad \text{(Eq.3)}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_O(2) = [+V_X]\ [g_{21}(2)] \qquad \text{(Eq. 4)}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\ [g_{21}(2) - g_{21}(1)] \qquad \text{(Eq. 5)}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{(Eq. 6)}$$

Hence,

$$g_{21}\ (2) \approx k\ [\ (V\text{-}) + V_Y\ ]. \qquad \text{(Eq. 7)}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\ [(V\text{-}) - V_Y]. \qquad \text{(Eq. 8)}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left\{[(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\right\} \quad \text{or}$$

$$V_O \approx 2\,k\,R_L\,V_X\,V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

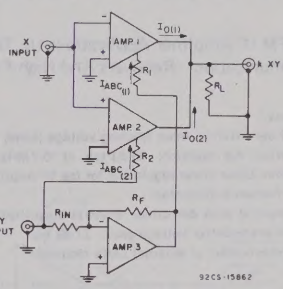


Fig.25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

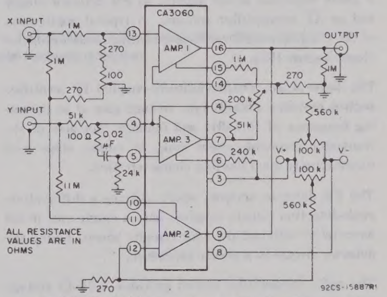


Fig.26—Typical four-quadrant multiplier circuit.

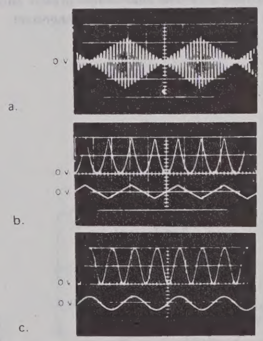


Fig.27—Voltage waveforms of four-quadrant multiplier circuit.

CA3075

FM IF Amplifier - Limiter, Detector, and Audio Preamplifier

For FM IF Amplifier Applications Up To 20 MHz In Communications Receivers And High-Fidelity Receivers

Features:

- Good sensitivity: Input limiting voltage (knee) = 250 μV typ. at 10.7 MHz
- Excellent AM rejection: 55 dB typ. at 10.7 MHz
- Internal Zener diode regulation for the IF amplifier section
- Low harmonic distortion
- Differential peak detection: Permits simplified single-coil tuning
- Audio preamplifier voltage gain: 21 dB typ.
- Minimum number of external parts required

RCA CA3075 is an integrated circuit which provides, in a single monolithic chip, an FM IF subsystem for Communications and High-Fidelity Receivers. This device, shown in the schematic diagram (Fig. 2), consists of a multistage IF amplifier-limiter section with a Zener regulated power supply, an FM detector stage, and an AF preamplifier section. A typical application of the CA3075, in FM receiver circuits, is shown in the block diagram (Fig. 1).

The three-stage, emitter-follower-coupled IF amplifier section provides a 60-dB typ. voltage gain at an operating frequency of 10.7 MHz and features, because of its transistor constant-current sink, an output stage with exceptionally good limiting characteristics.

The FM detector section, which utilizes a differential-peak-detection circuit, requires only a single coil in the associated outboard detector circuit; hence, tuning the detector circuit is a simple procedure.

The audio preamplifier circuit provides a 21-dB voltage gain with low impedance output for driving subsequent audio amplifier stages.

The CA3075 utilizes a 14-lead dual-in-line plastic package with leads in a special quad-formed arrangement.

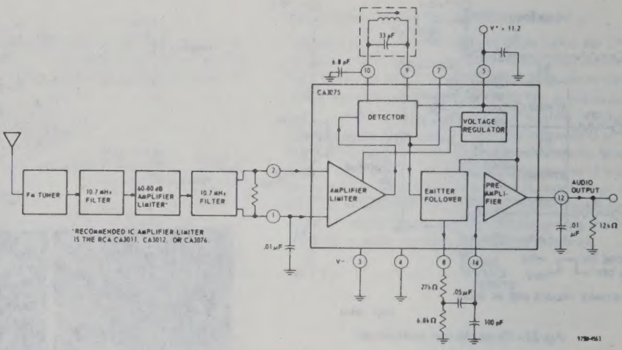
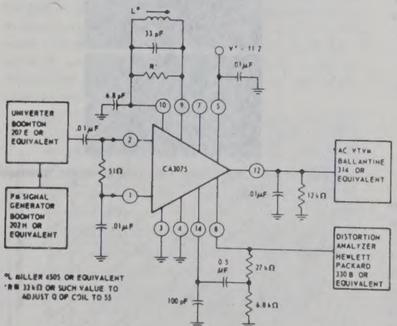


Fig. 1 - Block diagram of typical FM receiver utilizing the CA3075

MAXIMUM RATINGS, ***Absolute-Maximum Values at*** T_A **= 25°C**

DC Supply Voltage [between Terminals 5 (V$^+$) and 3 (V$^-$)]	12.5	V
DC Current (into Terminal 5)	30	mA
Device Dissipation:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
Ambient Temperature Range:		
Operating	−55 to + 125	°C
Storage	− 65 to + 150	°C
Lead Temperature (During soldering for 10 s max.)	+265	°C



L*
33 pF
R*
V+ = 11.2
.01 µF
6.8 pF
UNIVERTER BOONTON 207 E OR EQUIVALENT
FM SIGNAL GENERATOR BOONTON 202 H OR EQUIVALENT
.01 µF
51Ω
.01 µF
CA3075
AC VTVM BALLANTINE 314 OR EQUIVALENT
.01 µF
12 kΩ
DISTORTION ANALYZER HEWLETT PACKARD 330 B OR EQUIVALENT
0.5 µF
27 kΩ
100 pF
6.8 kΩ
*L MILLER 4505 OR EQUIVALENT
*R = 33 kΩ OR SUCH VALUE TO ADJUST Q OF COIL TO 55
10
9
7
5
2
1
12
3
4
14
8

Fig. 2 - **Test Circuit for input limiting voltage, recovered AF voltage, and total harmonic distortion**

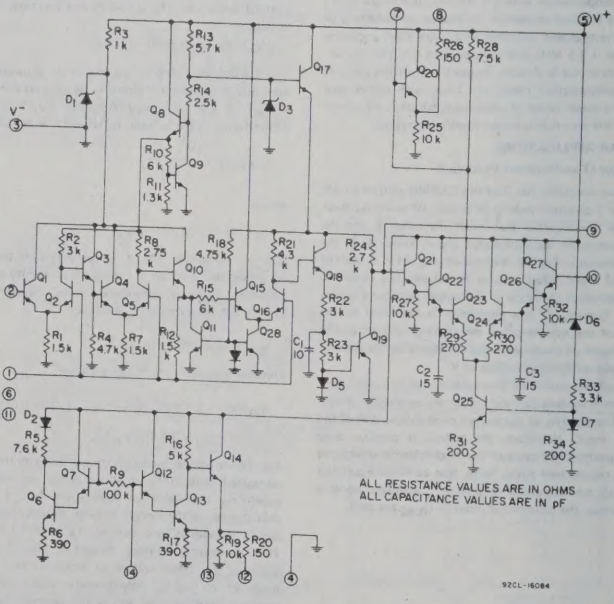
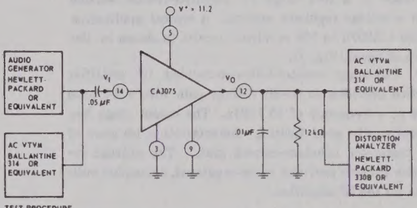


Fig.3 – Schematic diagram of CA3075

ELECTRICAL CHARACTERISTICS at T_A = 25° C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CIRCUIT FIG. NO.
Static Characteristics							
DC Voltage:							
At Terminal 7	V_7	V^+ = 11.2 V	–	6.1	–	V	6
At Terminal 8	V_8		–	5.4	–	V	
At Terminal 12	V_{12}		–	5.2	–	V	
DC Current (into Terminal 5):							
At V^+ = 8.5 V	I_5	–	8.5	15	–	mA	6
At V^+ = 11.2 V			–	17.5	–	mA	
At V^+ = 12.5 V			–	19	29	mA	
Dynamic Characteristics at V^+ = 11.2							
IF AMPLIFIER Input Limiting Voltage (knee, – 3 dB point)	V_I(lim)	f_O = 10.7 MHz f(Modulation) = 400 Hz Deviation = ±75 kHz	–	250	600	µV	3
AM Rejection	AMR	f_O = 10.7 MHz f(Modulation) = 400 Hz FM: Deviation = ±75 kHz AM: Modulation = 30%	–	55	–	dB	5
Input Impedance Components:							
Parallel Resistance	R_I	f_O = 10.7 MHz	–	4.5	–	kΩ	–
Parallel Capacitance	C_I	V_{IN} = 10 mV RMS	–	4.5	–	pF	
DETECTOR Recovered AF Voltage (at Terminal 12)	V_O(AF)	f_O = 10.7 MHz f(Modulation) = 400 Hz Deviation = ± 75 kHz	–	1.5	–	V	3
Total Harmonic Distortion	THD		–	1	2	%	
AUDIO PREAMPLIFIER Voltage Gain	A(AF)	V_{IN} = 100 mV, f_O = 400 Hz	–	21	–	dB	4
Total Harmonic Distortion	THD	V_{OUT} = 2 V, f_O = 400 Hz	–	1.5	5	%	4


V+ = 11.2
AUDIO GENERATOR HEWLETT-PACKARD OR EQUIVALENT
AC VTVM BALLANTINE 314 OR EQUIVALENT
V_I
.05 µF
14
5
3
9
CA3075
V_O
12
.01µF
124Ω
AC VTVM BALLANTINE 314 OR EQUIVALENT
DISTORTION ANALYZER HEWLETT-PACKARD 330B OR EQUIVALENT

TEST PROCEDURE

VOLTAGE GAIN

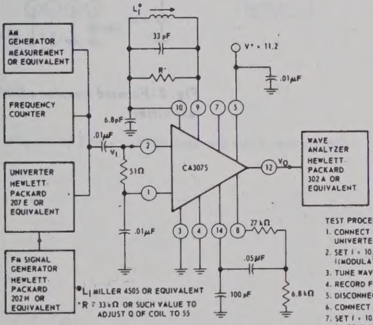
1. SET AUDIO GENERATOR FOR V_I = 100 mV RMS
2. READ V_O
3. GAIN = 20 $\log_{10} V_O/V_I$

DISTORTION

1. SET AUDIO GENERATOR FOR V_O = 2 V RMS
2. READ DISTORTION IN %

9 SS-156

Fig.4 — Test circuit for audio preamplifier voltage gain and total harmonic distortion


AM GENERATOR MEASUREMENT OR EQUIVALENT
FREQUENCY COUNTER
UNIVERTER HEWLETT-PACKARD 207 E OR EQUIVALENT
FM SIGNAL GENERATOR HEWLETT-PACKARD 202 H OR EQUIVALENT
L1*
33 pF
R*
V+ = 11.2
.01µF
6.8pF
.01µF
V_I
51Ω
.01µF
10
9
7
5
2
1
CA3075
3
4
14
8
27 kΩ
.05µF
100 pF
6.8 kΩ
12
V_O
WAVE ANALYZER HEWLETT-PACKARD 302 A OR EQUIVALENT

•L_1 MILLER 4505 OR EQUIVALENT
*R ≈ 33 kΩ OR SUCH VALUE TO ADJUST Q OF COIL TO 55

TEST PROCEDURE

1. CONNECT FM GENERATOR, FREQUENCY COUNTER, AND UNIVERTER TO INPUT OF CA3075
2. SET f = 10.7 MHz, V_I = 100 mV, f(MODULATION) = 400 Hz, f(DEVIATION) = ± 75 kHz
3. TUNE WAVE ANALYZER FOR PEAK READING AT 400 Hz
4. RECORD FM V_O(AF)
5. DISCONNECT FM GENERATOR
6. CONNECT AM GENERATOR TO INPUT OF CA3075
7. SET f = 10.7 MHz, V_I = 100 mV, f(MODULATION) = 400 Hz WITH 30% MODULATION
8. TUNE WAVE ANALYZER FOR PEAK READING AT 400 Hz
9. RECORD AM V_O(AF)

$$\text{AM REJECTION} = 20 \log_{10} \frac{\text{FM}:V_O(\text{AF})}{\text{AM}:V_O(\text{AF})}$$

92SS-1566

Fig.5 – Test circuit for AM rejection

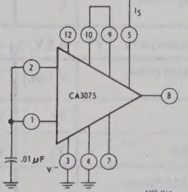


Fig. 6- Test circuit for static characteristics

CA3076

High-Gain Wide-Band IF Amplifier-Limiter

For FM IF Amplifier Applications
in Communications Receivers

RCA CA3076, monolithic integrated circuit, is a high-gain wide-band amplifier-limiter for use in the IF sections of Communications and High-Fidelity FM Receivers. The CA3076, shown in the schematic diagram (Fig. 2), consists of a four stage IF amplifier-limiter section with a voltage regulator section. A typical application of the CA3076 in FM receiver circuits is shown in the block diagram (Fig. 1).

The four-stage emitter-follower-coupled IF amplifier section provides an 80-dB voltage gain with a 2-kilohm load at a frequency of 10.7 MHz. The output stage has exceptionally good limiting characteristics because of its transistor constant-current sink. The voltage regulator section provides zener-regulated, decoupled voltages for the IF amplifier.

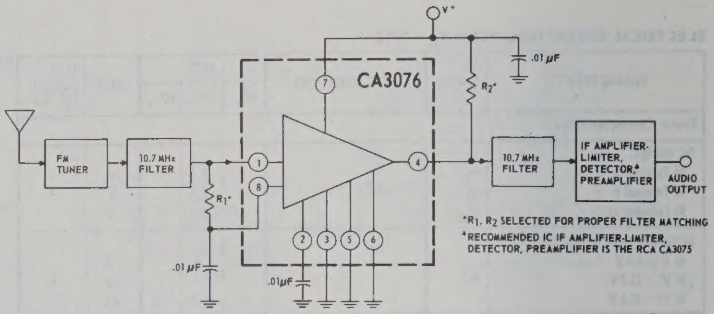
The CA3076 utilizes an hermetically-sealed 8-lead TO-5 package.

MAXIMUM RATINGS, ***Absolute Maximum-Values at*** T_A **= 25° C**

DC Supply Voltage [between Terminals 7 (V^+) and 3 (V^-)]	15	V
DC Current (into Terminal 7)	35	mA
Device Dissipation:		
Up to $T_A = 50^\circ C$	500	mW
Above $T_A = 50^\circ C$	derate linearly 5 mW/°C	
Ambient Temperature Range:		
Operating	− 55 to + 125	°C
Storage	− 65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+ 265	°C

ELECTRICAL CHARACTERISTICS at T_A **= 25°C**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Static Characteristics – $V^+ = 8.5$ V						
DC Current (into Term. 7)	I_7	–	10	15	24	mA
Quiescent Operating Current (into Term. 4)	I_4	–	–	0.65	–	mA
Dynamic Characteristics – $V^+ = 8.5$ V, $f_O = 10.7$ MHz						
Input Limiting Voltage (knee, − 3 dB point)	V_I (lim.)	–	–	50	200	µV
Output Voltage	V_O	$V_I = 20 \mu V$	4	12	–	mV
Output Noise Voltage	V_N	$V_I = 0$	–	1	–	mV
Forward Transfer Admittance: Magnitude Phase	 $\lvert Y_{21} \rvert$ θ_{21}	 $V_I =$ $10 \mu V$	 – –	 6 80	 – –	 mho degrees
Reverse Transfer Admittance: Magnitude Phase	 $\lvert Y_{12} \rvert$ θ_{12}	–	 – –	 0.1 − 90	 – –	 µmho degrees
Input-Impedance Components: Parallel Resistance Parallel Capacitance	 R_I C_I	–	 – –	 7.5 4	 – –	 kΩ pF
Output-Impedance Components: Parallel Resistance Parallel Capacitance	 R_O C_O	–	 50 –	 – 1.7	 – –	 kΩ pF



*R1, R2 SELECTED FOR PROPER FILTER MATCHING

▲RECOMMENDED IC IF AMPLIFIER-LIMITER, DETECTOR, PREAMPLIFIER IS THE RCA CA3075

Fig. 1 - Block diagram of typical FM receiver utilizing the CA3076.

Features:

- exceptionally good sensitivity: input limiting voltage (knee) = 50 µV typ. at 10.7 MHz
- high gain: 80 dB with 2-kilohm load
- internal voltage supply regulator
- wide frequency capability: > 20 MHz

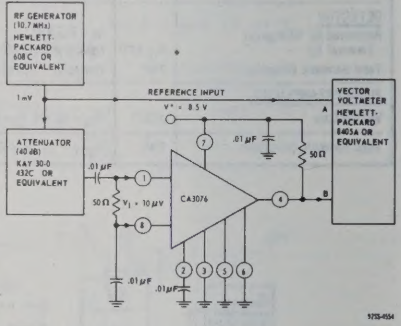

RF GENERATOR (10.7 MHz) HEWLETT-PACKARD 608C OR EQUIVALENT
1 mV
REFERENCE INPUT
VECTOR VOLTMETER HEWLETT-PACKARD 8405A OR EQUIVALENT
A
V+ = 8.5 V
ATTENUATOR (40 dB) KAY 30-0 432C OR EQUIVALENT
.01 µF
7
.01 µF
50Ω
1
50Ω
V1 = 10 µV
CA3076
4
B
8
2
3
5
6
.01 µF
.01µF
92SS-4554

Fig. 2 - Forward transfer admittance (Y_{21}) test circuit

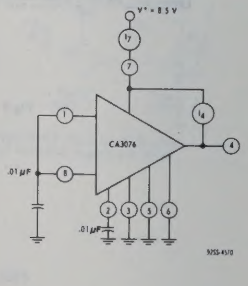
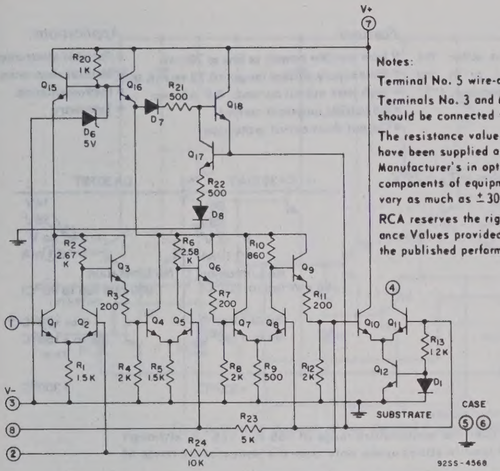


Fig. 3 - Test circuit for DC current (Terminal 7) and operating current (Terminal 4).



Notes:

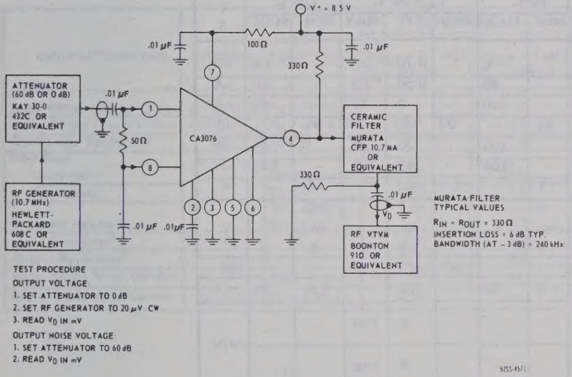
Terminal No. 5 wire-connected to the case.

Terminals No. 3 and 6 which are connected to the substrate should be connected to the most negative point in the circuit.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturer's in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

Fig. 4 - Schematic diagram of CA3076.


V+ = 8.5 V
.01 µF
100 Ω
.01 µF
330 Ω
7
ATTENUATOR (60 dB OR 0 dB) KAY 30-0 432C OR EQUIVALENT
.01 µF
1
50 Ω
CA3076
4
8
CERAMIC FILTER MURATA CFP 10.7 MA OR EQUIVALENT
330 Ω
.01 µF
V0
RF GENERATOR (10.7 MHz) HEWLETT-PACKARD 608 C OR EQUIVALENT
2
3
5
6
.01 µF
.01µF
RF VTVM BOONTON 91D OR EQUIVALENT
92SS-4571

MURATA FILTER TYPICAL VALUES

$R_{IN} = R_{OUT} = 330\ \Omega$

INSERTION LOSS = 6 dB TYP.

BANDWIDTH (AT – 3 dB) = 240 kHz

TEST PROCEDURE

OUTPUT VOLTAGE

1. SET ATTENUATOR TO 0 dB
2. SET RF GENERATOR TO 20 µV CW
3. READ V_0 IN mV

OUTPUT NOISE VOLTAGE

1. SET ATTENUATOR TO 60 dB
2. READ V_0 IN mV

Fig. 5 - 10.7 MHz voltage gain and noise test circuit

CA3078, CA3078A Types
Micropower Operational Amplifier

The RCA CA3078T and CA3078AT are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078T and CA3078AT provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

The CA3078AT is a premium device having a supply voltage range of V± = 0.75V to V± = 15V and an operating temperature range of -55°C to +125°C. The CA3078T has the same lower supply voltage limit but the upper limit is V+ +6V and V− = -6V. The operating temperature range is from 0°C to +70°C.

The CA3078 and CA3078A are supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix).

Features:

- **Low standby power: as low as 700 nW**
- **Wide supply voltage range: ±0.75 to ±15 V**
- **High peak output current: 6.5 mA min.**
- **Adjustable quiescent current**
- **Output short-circuit protection**

Applications:

- **Portable electronics**
- **Medical electronics**
- **Instrumentation**
- **Telemetry**

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

	CA3078AT	CA3078T
DC Supply Voltage (between V+ and V− terminal	36V	14V
Differential Input Voltage	±6V	±6V
DC Input Voltage	V+ to V−	V+ to V−
Input Signal Current	0.1 mA	0.1 mA
Output Short-Circuit Duration*	No Limitation	No Limitation
Device Dissipation	50 mW (up to 125°C)	500 mW (up to 70°C)
Temperature Range		
Operating	-55 to +125°C	0 to +70°C ▲
Storage	-65 to +150°C	-65 to +150°C
Lead Temperature (During Soldering) At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+300°C	+300°C

---

*Short circuit may be applied to ground or to either supply.

▲ Types CA3078S and T can be operated over the temperature range of -55 to +125° C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70° C.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			CA3078T LIMITS					CA3078AT LIMITS					UNITS
					R_{SET} = 1 MΩ, I_Q = 100 μA					R_{SET} = 5.1 MΩ, I_Q = 20 μA					
		V+ & V−	R_S KΩ	R_L KΩ	T_A = 25°C			T_A = 0 to 70°C		T_A = 25°C			T_A = -55 to 125°C		
					MIN	TYP	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	6	≤10		–	1.3	4.5	–	5	–	0.70	3.5	–	4.5	mV
Input Offset Current	I_{IO}				–	6	32	–	40	–	0.50	2.5	–	5.0	nA
Input Bias Current	I_{IB}					60	170	–	200	–	7	12	–	50	nA
Open-Loop Diff. Voltage Gain	A_{OL}			≥10	88	92	–	86	–	92	100	–	90	–	dB
Total Quiescent Current	I_Q					100	130	–	150	–	20	25	–	45	μA
Device Dissipation	P_D				–	1200	1560	–	1800	–	240	300	–	540	μW
Maximum Output Voltage	V_{OM}			≥10	±5.1	±5.3	–	±5	–	±5.1	±5.3	–	±5	–	V
Common-Mode Input Voltage Range	V_{ICR}		≤10		–	-5.5 to +5.8		-5 to +5	–		-5.5 to +5.8	–	-5 to +5	–	V
Common-Mode Rejection Ratio	CMRR		≤10		80	110		–	–	80	115	–	–	–	dB
Maximum Output Current	I_{OM}^+ or I_{OM}^-					12	–	6.5	30		12	–	6.5	30	mA
Input Offset Voltage Sensitivity															
Positive	$\Delta V_{IO}/\Delta V^+$		≤10			22	150	–	–		6	150	–	–	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$					22	150		–		6	150		–	
										R_{SET} = 13 MΩ, I_Q = 20 μA					
Input Offset Voltage	V_{IO}	15	≤10					–	–		1.4	3.5	–	4.5	mV
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10			–	–	–	92	100	–	88	–	dB
Total Quiescent Current	I_Q						–	–	–		20	30		50	μA
Device Dissipation	P_D							–	–	–	600	750	–	1350	μW
Maximum Output Voltage	V_{OM}			≥10				–	–	±13.7	±14.1		±13.5	–	V
Common-Mode Rejection Ratio	CMRR		≤10					–	–	80	106		–	–	dB
Input Bias Current	I_{IB}						–	–	–		7	14	–	55	nA
Input Offset Current	I_{IO}					–	–	–	–		0.50	2.7	–	5.5	nA

OPERATING CONSIDERATIONS

Compensation Techniques

The CA3078AT and CA3078T can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figs. 24 and 25. These curves represent the compensation necessary at quiescent currents of 20 μA and 100 μA, respectively, for a transient response with 10% overshoot. Figs. 21 and 22 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 20 μA and 100 μA.

Single Supply Operation

The CA3078AT and CA3078T can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figs. 27 and 28 show the CA3078AT or CA3078T in inverting and non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300 mV p-p with a 20 kΩ load.

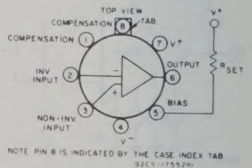


Fig.1 – Functional diagram of the CA3078T and CA3078AT.

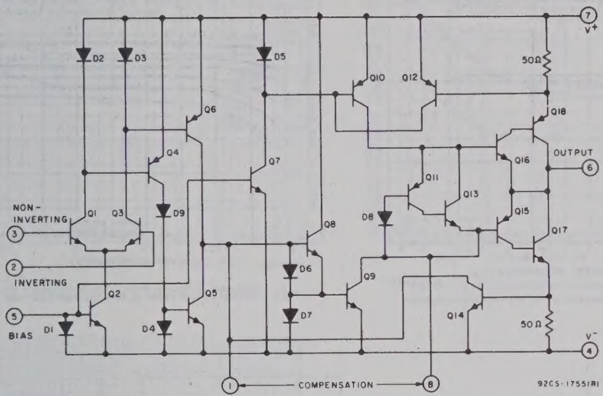


Fig.2-Schematic diagram of the CA3078T and CA3078AT.

Typical Values Intended Only for Design Guidance at T_A = 25°C and V^+ = +6 V, V^- = 6 V

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CA3078AT R_{SET} = 5.1 MΩ I_Q = 20 μA	CA3078AT R_{SET} = 1 MΩ I_Q = 100 μA	CA3078T R_{SET} = 1 MΩ I_Q = 100 μA	UNITS
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ KΩ	5	6	6	μV/°C
Input Offset Current Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ KΩ	6.3	70	70	pA/°C
Open-Loop Bandwidth	BW_{OL}	3dB pt	0.3	2	2	kHz
Slew Rate:						
Unity Gain	SR	See Figs. 20, 21	0.027	0.04	0.04	V/μs
Comparator			0.5	1.5	1.5	
Transient Response		10% to 90% Rise Time	3	2.5	2.5	μs
Input Resistance	R_I		7.4	1.7	0.87	MΩ
Output Resistance	R_O		1	0.8	0.8	KΩ
Equiv. Input Noise Voltage	e_N(10Hz)	R_S 0	40	–	25	nV/$\sqrt{Hz}$
Equiv. Input Noise Current	i_N(10Hz)	R_S 1 MΩ	0.25	–	1	pA/$\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS, at T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTICS SYMBOLS	TYPICAL VALUES CA3078AT V^+ = +1.3V, V^- = -1.3V R_{SET} = 2 MΩ I_Q = 10 μA	CA3078AT V^+ = +0.75V, V^- = -0.75V R_{SET} = 10 MΩ I_Q = 1 μA	CA3078T V^+ = +1.3V, V^- = -1.3V R_{SET} = 2 MΩ I_Q = 10 μA	CA3078T V^+ = 0.75V, V^- = -0.75V R_{SET} = 10 MΩ I_Q = 1 μA	UNITS
V_{IO}	0.7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1.7	0.5	nA
I_{IB}	3.7	0.45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	μA
P_D	26	1.5	26	1.5	μW
V_{OPP}	1.4	0.3	1.4	0.3	V
V_{ICR}	−0.8 to +1.1	−0.2 to +0.5	−0.8 to +1.1	−0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}^{\pm}$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V^{\pm}$	20	50	20	50	μV/V

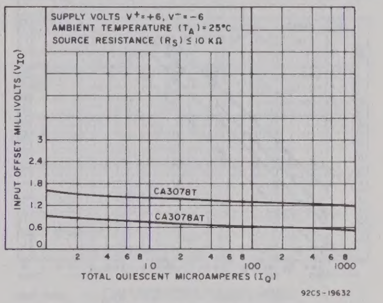


Fig.3 – Input offset voltage vs. total quiescent current.

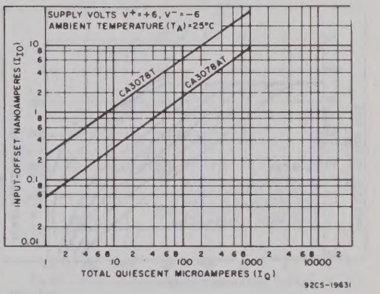


Fig.4 – Input offset current vs. total quiescent current.

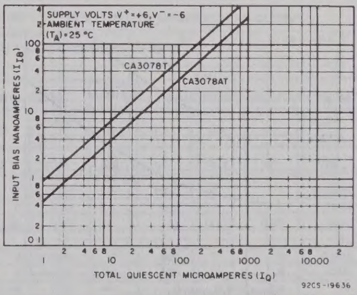


Fig.5 – Input bias current vs. total quiescent current.

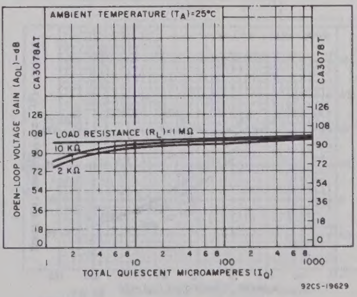
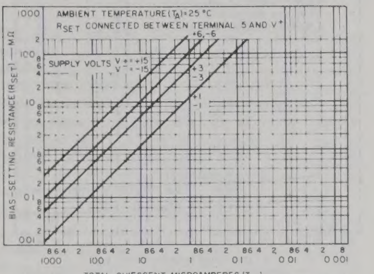


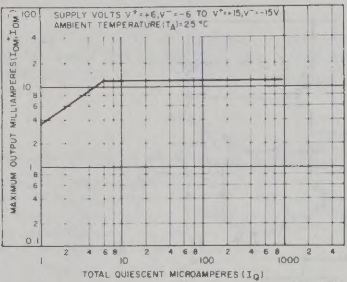
Fig.6 – Open-loop voltage gain vs. total quiescent current.

CA3078, CA3078A Types



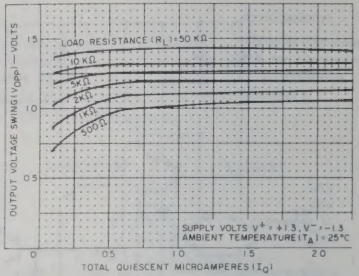
92CS-19637

Fig.7 – Bias-setting resistance vs. total quiescent current.



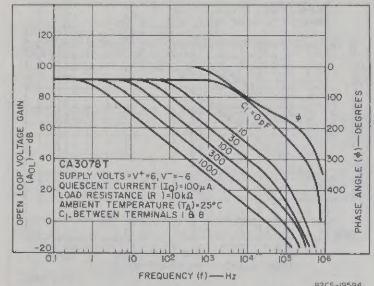
92CS-19630

Fig.8 – Maximum output current vs. total quiescent current.



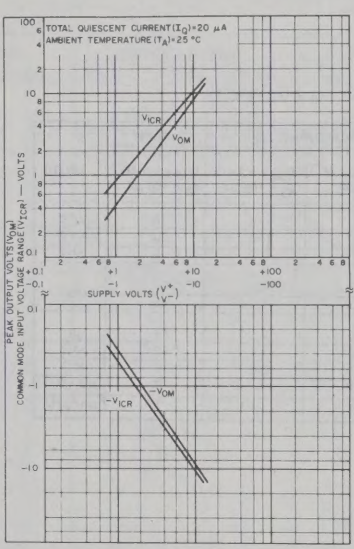
92CS-19627

Fig.9 – Output voltage swing vs. total quiescent current.



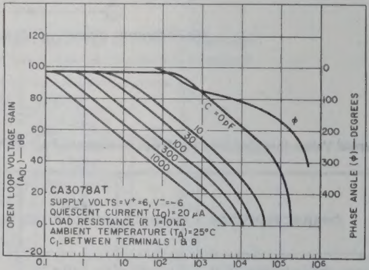
92CS-19594

Fig.10 – Open-loop voltage gain vs. frequency for I_Q = 100 μA – CA3078T.



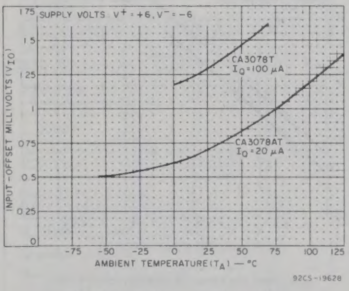
92CS-19635

Fig.11 – Output and common-mode voltage vs. supply voltage.



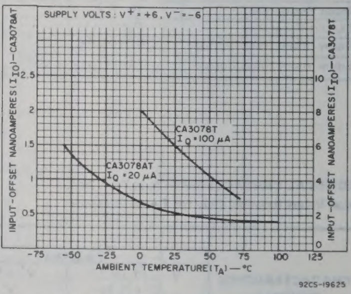
92CS-19593

Fig.12 – Open-loop voltage gain vs. frequency for I_Q = 20 μA – CA3078AT.



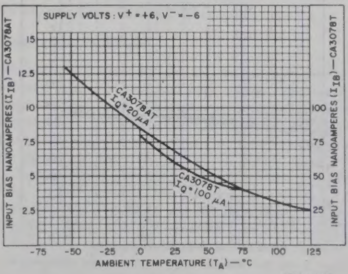
92CS-19628

Fig.13 – Input offset voltage vs. temperature.



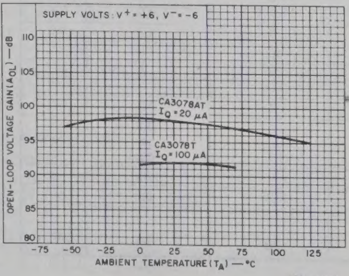
92CS-19625

Fig.14 – Input offset current vs. temperature.



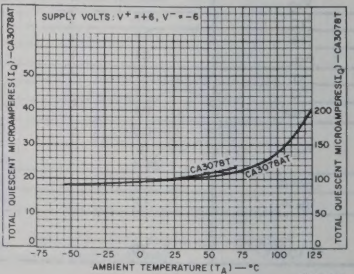
92CS-19623

Fig.15 – Input bias current vs. temperature.



92CS-19624

Fig.16 – Open-loop voltage gain vs. temperature.



92CS-19626

Fig.17 – Total quiescent current vs. temperature.

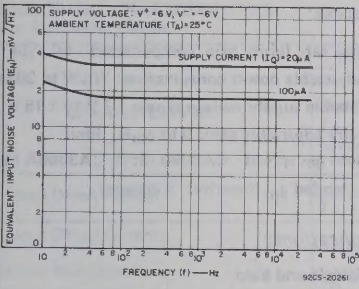


Fig.18 – Equivalent input noise voltage vs. frequency.

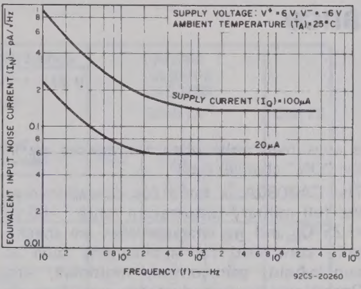


Fig.19 – Equivalent input noise current vs. frequency.

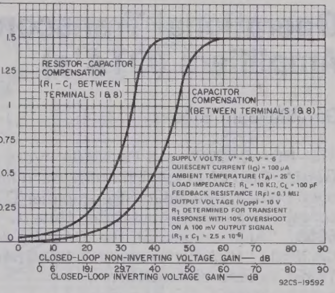


Fig.20 – Slew rate vs. closed-loop gain for I_Q = 100 μA – CA3078T.

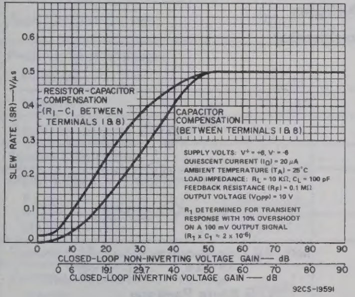


Fig.21 – Slew rate vs. closed-loop gain for I_Q = 20 μA – CA3078AT.

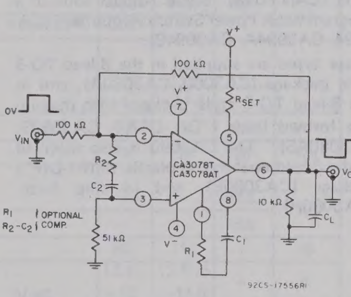


Fig.22 – Transient response and slew-rate, unity gain (inverting) test circuit.

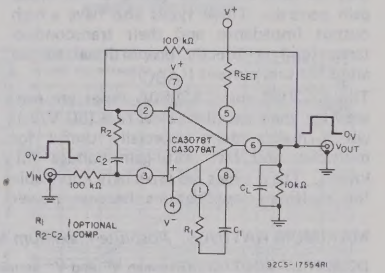


Fig.23 – Slew, rate, unity gain (non-inverting) test circuit.

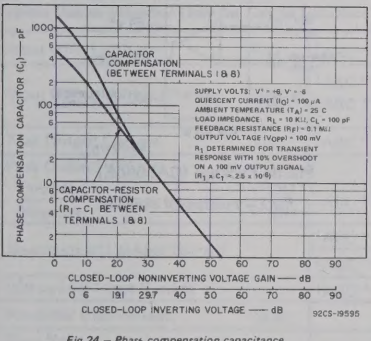


Fig.24 – Phase compensation capacitance vs. closed-loop gain – CA3078T.

Table I - Unity-gain slew rata vs. compensation – CA3078T and CA3078AT

SUPPLY VOLTS: $V^+ = 6$, $V^- = -6$

OUTPUT VOLTAGE (V_O) = ±5V
LOAD RESISTANCE (R_L) = 10 kΩ

TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE of 100 mV
AMBIENT TEMPERATURE (T_A) = 25°C

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078T – I_Q = 100 μA	kΩ	pF	kΩ	μF	V/μs	kΩ	pF	kΩ	μF	V/μs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078AT – I_Q = 20 μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

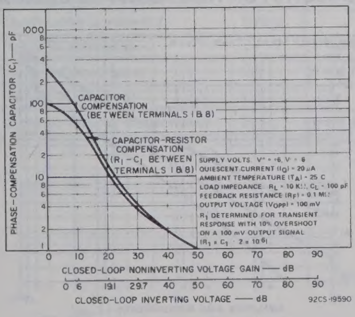


Fig.25 – Phase compensation capacitance vs. closed-loop gain – CA3078AT.

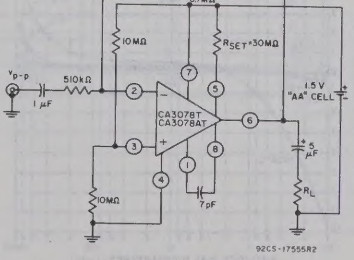


Fig.27 – Inverting 20-dB amplifier circuit.

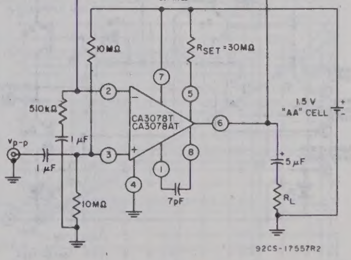


Fig.28 – Non-inverting 20-dB amplifier circuit.

CA3080, CA3080A Types

Operational Transconductance Amplifiers (OTA's)

Gatable-Gain Blocks

The RCA-CA3080 and CA3080A types are Gatable-Gain Blocks which utilize the unique operational-transconductance-amplifier(OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A types are notable for their excellent slew rate (50 V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (−55 to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA-3094, CA3094A, CA3094B).

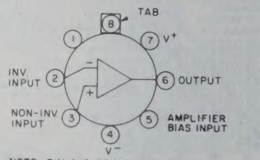
These types are supplied in the 8-lead TO-5 style package (CA3080, CA3080A), and in the 8-lead TO-5 style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080 is also supplied in the 8-lead dual-in-line plastic (MINI-DIP") package (CA3080E), and in chip form (CA3080H).

Features:

- **Slew rate (unity gain, compensated): 50 V/μs**
- **Adjustable power consumption: 10μW to 30 mW**
- **Flexible supply voltage range: ± 2 V to ± 15 V**
- **Fully adjustable gain: 0 to g_mR_L limit**
- **Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1**
- **Extended g_m linearity: 3 decades**

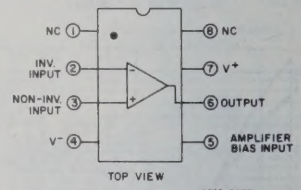
Applications:

- **Sample and hold**
- **Multiplex**
- **Voltage follower**
- **Multiplier**
- **Comparator**



NOTE: PIN 4 IS CONNECTED TO CASE
TOP VIEW 92CS-24770R1

TO-5 Style Package



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Plastic Package (CA3080E)

Fig.1 – Functional diagrams.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V+ and V− terminals)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE	V+ to V−
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA3080, CA3080E, CA3080S	0 to + 70 °C
CA3080A, CA3080AS	−55 to + 125 °C
Storage	−65 to + 150 °C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 265 °C

* Short circuit may be applied to ground or to either supply.

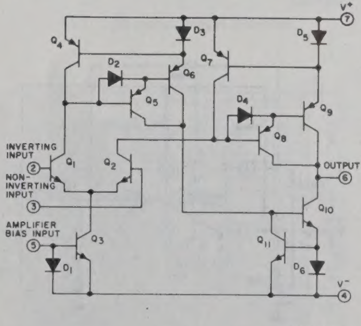


Fig.2 – Schematic diagram for CA3080 and CA3080A.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

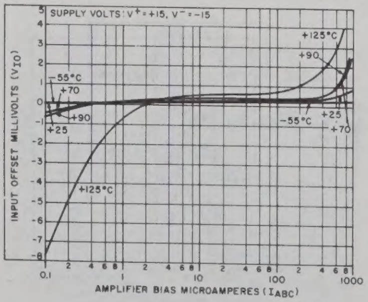


Fig.3 – Input offset voltage as a function of amplifier bias current.

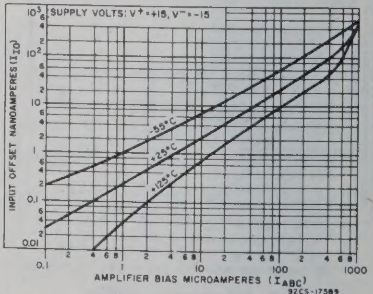


Fig.4 – Input offset current as a function of amplifier bias current.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS $V^+ = 15$ V, $V^- = -15$ V $I_{ABC} = 500\ \mu A$ $T_A = 25^oC$ (unless indicated otherwise)	CA3080 CA3080E CA3080S LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}		–	0.4	5	mV
		$T_A = 0$ to 70^oC	–	–	6	
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = 0$ to 70^oC	–	–	7	
Forward Transconductance (large signal)	g_m		6700	9600	13000	μmho
		$T_A = 0$ to 70^oC	5400	–	–	
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	350	500	650	μA
		$R_L = 0$, $T_A = 0$ to 70^oC	300	–	–	
Peak Output Voltage:						
Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	V
Negative	V^-_{OM}		–12	–14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						
Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to –12	13.6 to –14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080 CA3080E CA3080S	
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	0.3	mV
Input Offset Voltage Change	$\lvert \Delta V_{IO} \rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	0.2	mV
Peak Output Current	I_{OM}	$I_{ABC} = 5\ \mu A$	5	μA
Peak Output Voltage:				
Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$	13.8	V
Negative	V^-_{OM}		–14.5	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	0.08	nA
		$I_{ABC} = 0$, $V_{TP} = 36$ V	0.3	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4$ V	0.008	nA
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				
Maximum (uncompensated)	SR		75	V/μs
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}		2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

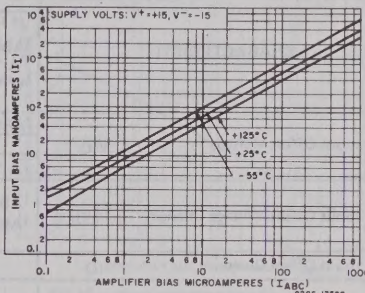


Fig.5 — Input bias current as a function of amplifier bias current.

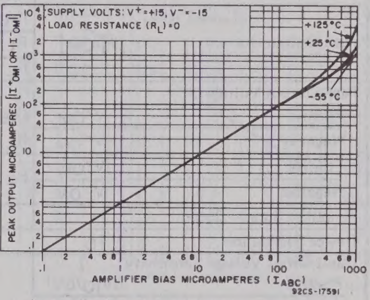


Fig.6 — Peak output current as a function of amplifier bias current.

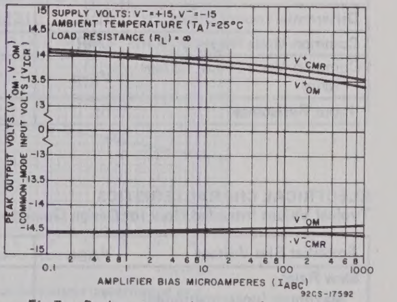


Fig.7 — Peak output voltage as a function of amplifier bias current.

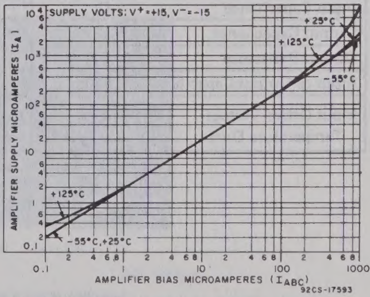


Fig.8 — Amplifier supply current as a function of amplifier bias current.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS $V^+ = 15$ V, $V^- = -15$ V $I_{ABC} = 500\ \mu A$ $T_A = 25^oC$ (unless indicated otherwise)	CA3080A CA3080AS LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	–	0.3	2	mV
			–	0.4	2	
		$T_A = -55$ to $+125^oC$	–	–	5	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	–	0.1	3	mV
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = -55$ to $+125^oC$	–	–	8	
Forward Transconductance (large signal)	g_m		7700	9600	12000	μmho
		$T_A = -55$ to $+125^oC$	4000	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$	$I_{ABC} = 5\ \mu A$, $R_L = 0$	3	5	7	μA
		$R_L = 0$	350	500	650	
		$R_L = 0$, $T_A = -55$ to $+125^oC$	300	–	–	
Peak Output Voltage:						
Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$ $R_L = \infty$	12	13.8	–	V
Negative	V^-_{OM}		–12	–14.5	–	
Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	
Negative	V^-_{OM}		–12	–14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						
Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	–	0.08	5	nA
		$I_{ABC} = 0$, $V_{TP} = 36$ V	–	0.3	5	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4$ V	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR		80	110	--	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to –12	13.6 to –14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080A CA3080AS	
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				
Maximum (uncompensated)	SR		75	V/μs
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}	–	2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	C_{I-O}	f = 1 MHz	0.024	pF
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	$I_{ABC} = 100\ \mu A$, $T_A = -55$ to $+125^oC$	3	$\mu V/^oC$

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

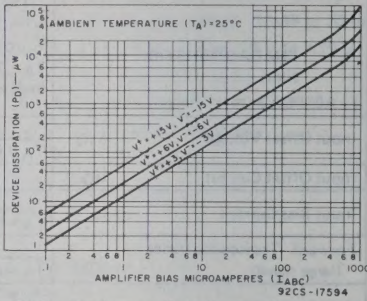


Fig.9 — Total power dissipation as a function of amplifier bias current.

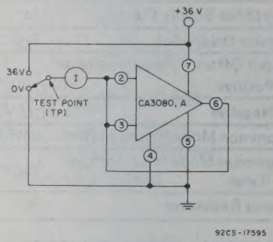


Fig.10 — Leakage current test circuit.

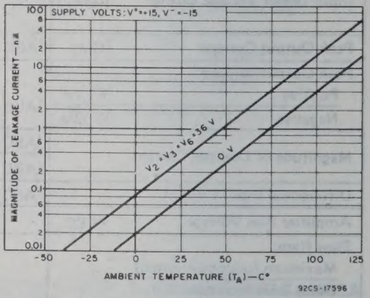


Fig.11 — Leakage current as a function of temperature.

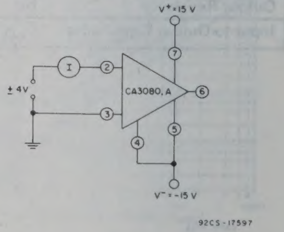


Fig.12 — Differential input current test circuit.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

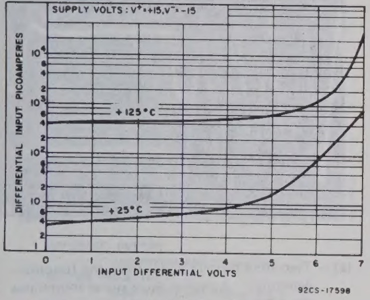


Fig.13 – Input current as a function of input differential voltage.

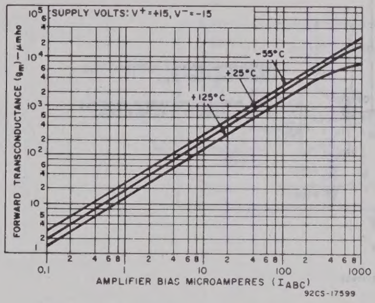


Fig.14 – Transconductance as a function of amplifier bias current.

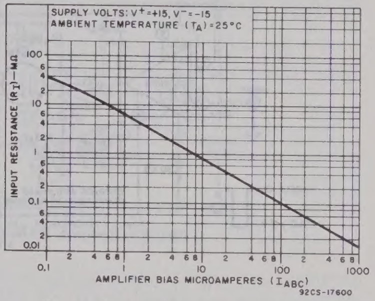


Fig.15 – Input resistance as a function of amplifier bias current.

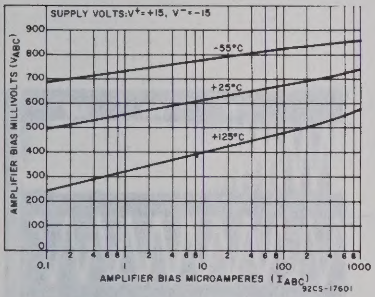


Fig.16 – Amplifier bias voltage as a function of amplifier bias current.

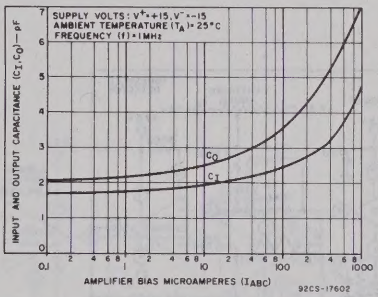


Fig.17 – Input and output capacitance as a function of amplifier bias current.

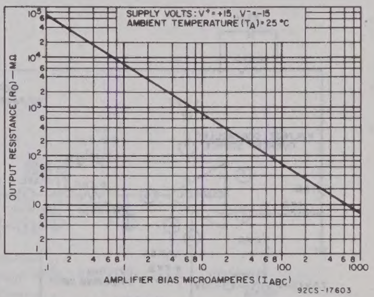


Fig.18 – Output resistance as a function of amplifier bias current.

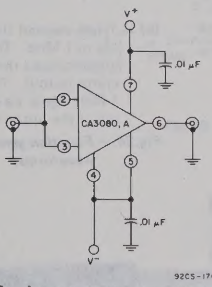


Fig.19 – Input-to-output capacitance test circuit.

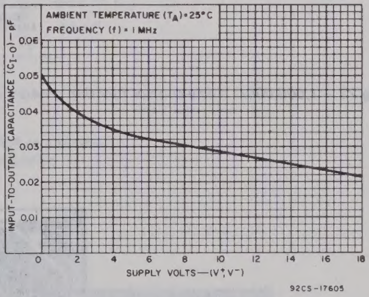


Fig.20 – Input-to-output capacitance as a function of supply voltage.

APPLICATIONS

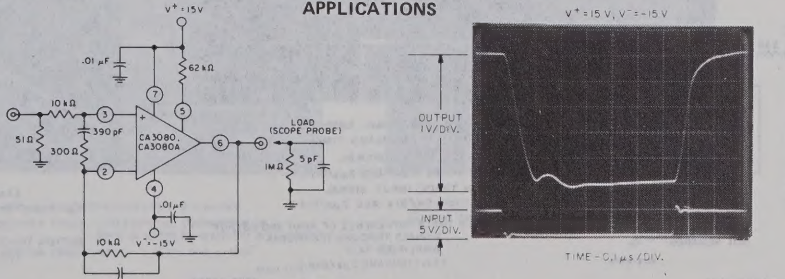
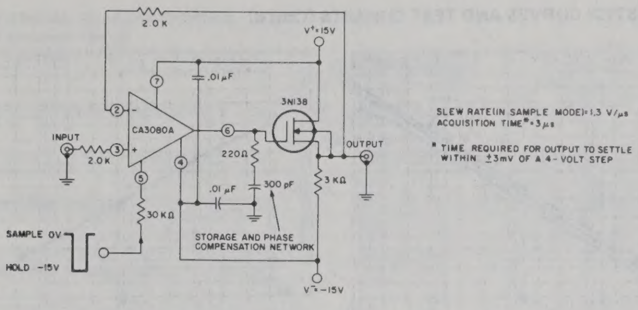
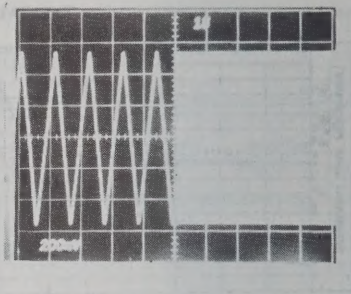


Fig.21 – Schematic diagram of the CA3080 and CA3080A in a unity-gain voltage follower configuration and associated waveform.

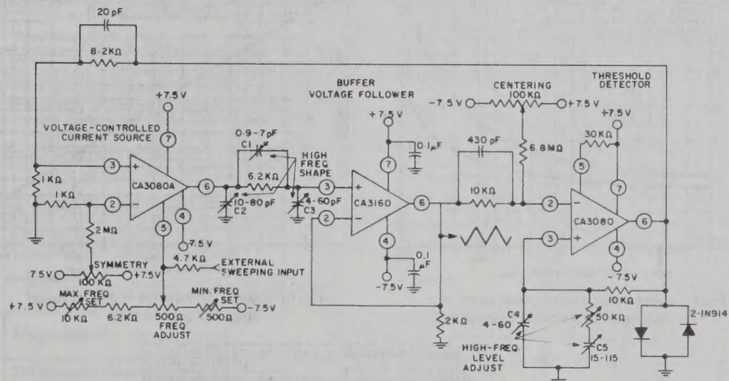

2.0 K
V+=15V
.01 µF
3N138
CA3080A
INPUT
2.0 K
220Ω
.01 µF
300 pF
3 KΩ
OUTPUT
30 KΩ
SAMPLE 0V
HOLD -15V
STORAGE AND PHASE COMPENSATION NETWORK
V−=-15V
SLEW RATE(IN SAMPLE MODE)=1.3 V/µs
ACQUISITION TIME*=3µs
* TIME REQUIRED FOR OUTPUT TO SETTLE WITHIN ±3mV OF A 4-VOLT STEP

92CS-17606

Fig.22 – Schematic diagram of the CA3080A in a sample-hold configuration.

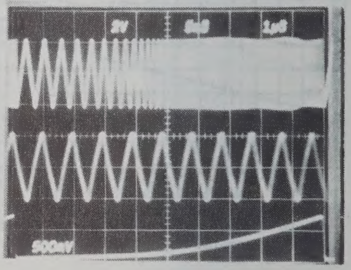


(a) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.



92CM-28586R1

Fig.23 – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



92CS-28588

(b) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Fig.24 – Function generator dynamic characteristics waveforms.

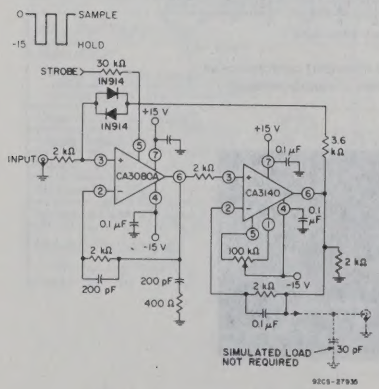
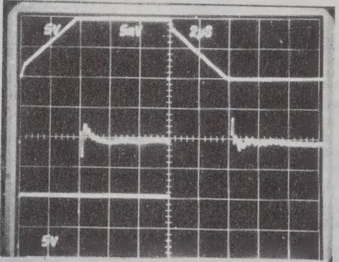


Fig.25 – Sample- and hold circuit.



LARGE-SIGNAL RESPONSE AND SETTLING TIME

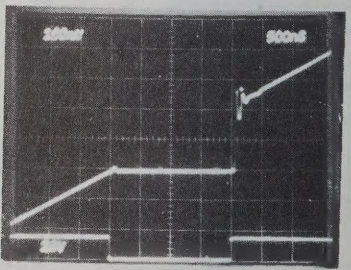
TOP TRACE: OUTPUT SIGNAL (5 V/DIV. AND 2µs/DIV.)

BOTTOM TRACE: INPUT SIGNAL (5V/DIV. AND 2µs/DIV.)

CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13 (5mV/DIV. AND 2µs/DIV.)

92CS-27884

Fig.26 – Large-signal response and settling time for circuit shown in Fig.25.



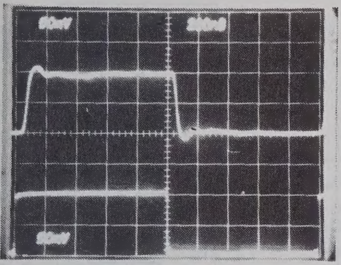
SAMPLING RESPONSE

TOP TRACE: SYSTEM OUTPUT (100 mV/DIV. AND 500 ns/DIV.)

BOTTOM TRACE: SAMPLING SIGNAL (20 V/DIV. AND 500 ns/DIV.)

92CS-27885

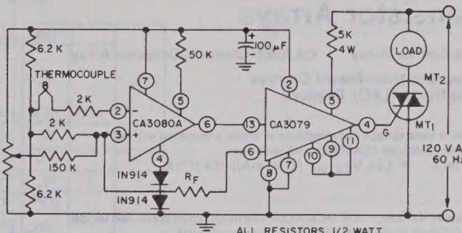
Fig.27 – Sampling response for circuit shown in Fig. 25.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)

92CS-27883

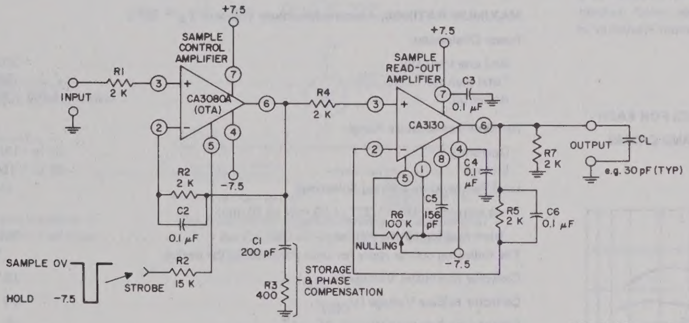
Fig.28 — Input and output response for circuit shown in Fig. 25.



ALL RESISTORS 1/2 WATT
UNLESS OTHERWISE SPECIFIED

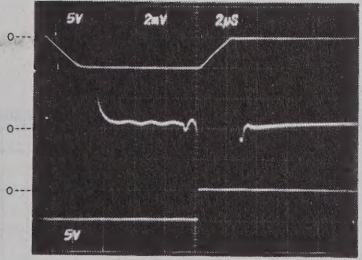
92CS-22619RI

Fig.29 — Thermocouple temperature control with CA3079 zero voltage switch as the output amplifier.



92CM-27159RI

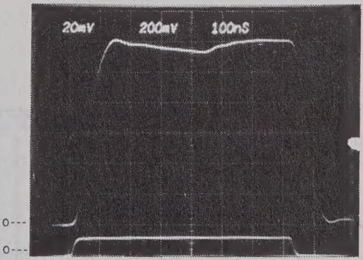
Fig.30 — Schematic diagram of the CA3080A in a sample-hold circuit with BiMos output amplifier.



TOP TRACE: OUTPUT—5 V/DIV. & 2 µs/DIV.
CENTER TRACE: DIFFERENTIAL COMPARISON OF
INPUT & OUTPUT—2 mV/DIV. & 2 µs/DIV.
BOTTOM TRACE: INPUT—5 V/DIV. & 2 µs/DIV.

92CS-27161

Fig.31 — Large-signal response for circuit shown in Fig. 30.



TOP TRACE: OUTPUT — 20 mV/DIV. & 100 ns/DIV.
BOTTOM TRACE: INPUT—200 mV/DIV. & 100 ns/DIV.

92CS-27160

Fig.32 — Small-signal response for circuit shown in Fig. 30.

CA3081, CA3082 Types

General-Purpose High-Current N-P-N Transistor Arrays

CA3081–Common-Emitter Array CA3082–Common-Collector Array

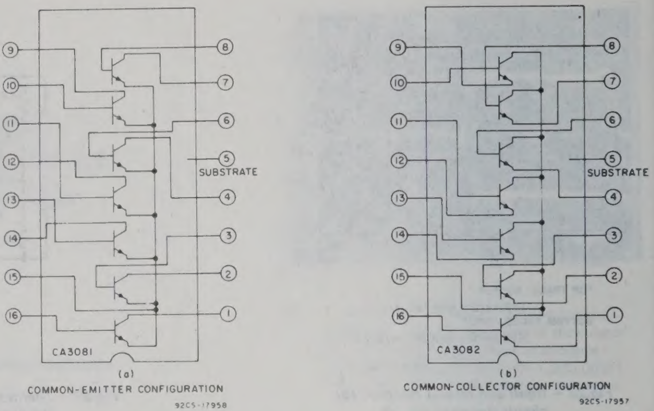
Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Displays

Features

- **7 transistors permit a wide range of applications in either a common-emitter (CA3081) or common-collector (CA3082) configuration**
- **High I_C: 100 mA max.** ■ **Low $V_{CE\ sat}$ (at 50 mA): 0.4 V typ.**

Applications

- **Drivers for:**
  - **Incandescent display devices (e.g. RCA NUMITRON DR2000 Series and lamps)**
  - **LED (e.g. RCA-SG1002 GaAs High-Efficiency Emitting Diode)**
  - **Relay control** – **Thyristor firing**



(a) COMMON-EMITTER CONFIGURATION

(b) COMMON-COLLECTOR CONFIGURATION

Fig.1–Functional diagrams of types CA3081 and CA3082.

RCA-CA3081* and CA3082* consist of seven high-current (to 100 mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common-emitter configuration and the CA3082 is connected in a common-collector configuration.

The CA3081 and CA3082 are capable of directly driving seven-segment displays, such as the RCA NUMITRON devices (DR2000 and DR2010), and light-emitting diode (LED) displays. These types are also well-suited for a variety of other driver applications, including relay control and thyristor firing.

The CA3081 and CA3082 are supplied in a 16-lead dual-in-line plastic package, and the CA3081F and CA3082F in a 16-lead dual-in-line frit-seal ceramic package, which includes a separate substrate connection for maximum flexibility in circuit design.

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

Power Dissipation:		
Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	–55 to +125	°C
Storage	–65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	16	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3081 AND CA3082

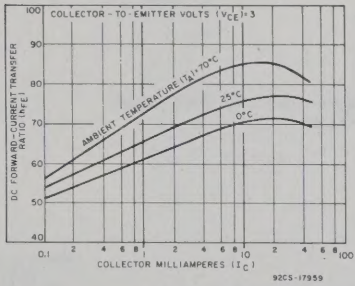


Fig.2–h_{FE} vs. I_C

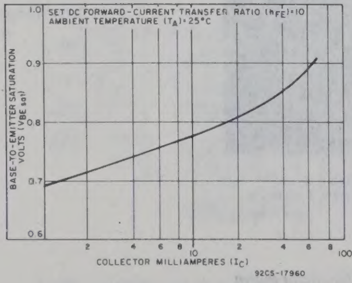


Fig.3–V_{BEsat} vs. I_C

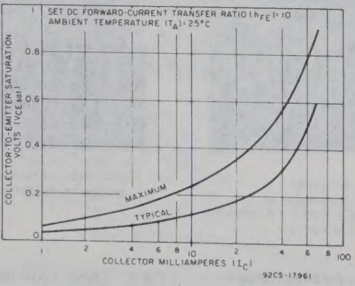


Fig.4–V_{CEsat} vs. I_C at $T_A = 25^oC$.

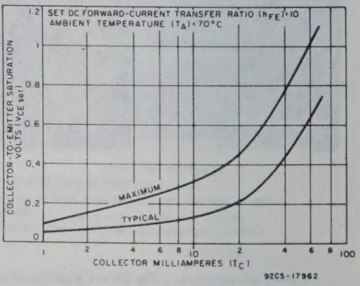


Fig.5–V_{CEsat} vs. I_C at $T_A = 70^oC$.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$
For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
			Typ. Char. Curve Fig. No.	Min.	Typ.	Max.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	$I_C = 500\ \mu A$, $I_E = 0$	–	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 500\ \mu A$, $I_E = 0$, $I_B = 0$	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	–	16	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_C = 500\ \mu A$	–	5	6.9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 0.5$ V, $I_C = 30$ mA	–	30	68	–	
		$V_{CE} = 0.8$ V, $I_C = 50$ mA	–	40	70	–	
Base-to-Emitter Saturation Voltage	$V_{BE\ sat}$	$I_C = 30$ mA, $I_B = 1$ mA	3	–	0.87	1.0	V
Collector-to-Emitter Saturation Voltage:							
CA3081, CA3082	$V_{CE\ sat}$	$I_C = 30$ mA, $I_B = 1$ mA	–	–	0.27	0.5	V
CA3081		$I_C = 50$ mA, $I_B = 5$ mA	4	–	0.4	0.7	
CA3082		$I_C = 50$ mA, $I_B = 5$ mA	4	–	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	–	–	–	10	µA
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	–	–	–	1	µA

TYPICAL READ-OUT DRIVER APPLICATIONS

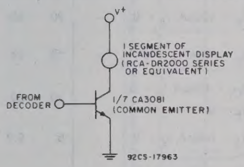
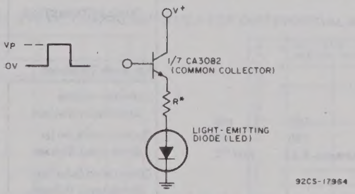

V+
I SEGMENT OF INCANDESCENT DISPLAY (RCA-DR2000 SERIES OR EQUIVALENT)
FROM DECODER
1/7 CA3081 (COMMON EMITTER)
92CS-17963

Fig.6—Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.



*THE RESISTANCE FOR R IS DETERMINED BY THE RELATIONSHIP

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I(LED)}$$

$R = 0$ FOR $V_P = V_{BE} + V_F(LED)$

WHERE: V_P = INPUT PULSE VOLTAGE

V_F = FORWARD VOLTAGE DROP ACROSS THE DIODE

Fig.7—Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

CA3083

General-Purpose High-Current N-P-N Transistor Array

RCA-CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line plastic package, and the CA3083F in a 16-lead dual-in-line frit-seal ceramic package.

Features

- High I_C: 100mA max.
- Low V_{CEsat} (at 50mA): 0.7V max.
- Matched pair (Q1 and Q2)–
  V_{IO} (V_{BE} matched): ± 5 mV max.
  I_{IO} (at 1mA): 2.5 μA max.
- 5 independent transistors plus separate substrate connection
- **The CA3083 is available in a sealed-junction Beam-Lead version (CA3083L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

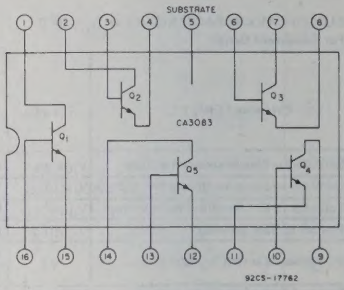


Fig.1–Functional diagram of the CA3083.

Applications

- Signal processing and switching systems operating from DC to VHF
- Lamp and relay driver
- Differential amplifier
- Temperature-compensated amplifier
- Thyristor firing
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for suggested applications

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	-55 to +125	°C
Storage	65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16" +1/32" (1.59 mm +0.79 mm) from case for 10 seconds max.	265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	2	40	76	–	
		V_{CE} = 3V, I_C = 50mA		40	75	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	4	–	0.40	0.70	V
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\|V_{IO}\|$	V_{CE} = 3V, I_C = 1mA	7	–	1.2	5	mV
Absolute Input Offset Current	$\|I_{IO}\|$		8	–	0.7	2.5	μA

TYPICAL STATIC CHARACTERISTICS
FOR EACH TRANSISTOR

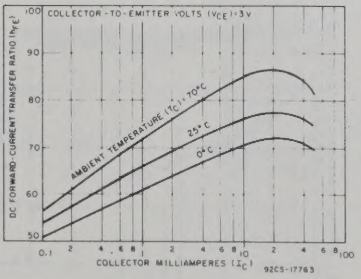


Fig.2 – h_{FE} vs I_C

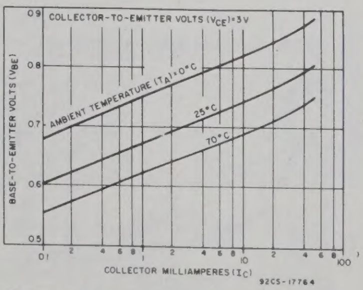


Fig.3 – V_{BE} vs I_C

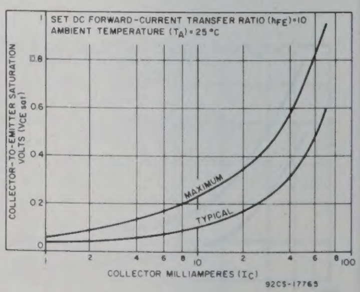


Fig.4 – V_{CEsat} vs I_C at 25°C

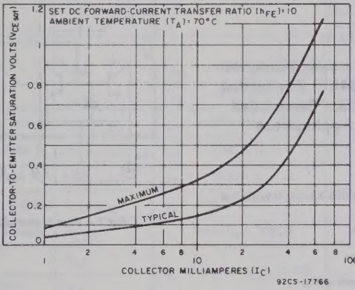


Fig.5 – V_{CEsat} vs I_C at 70°C

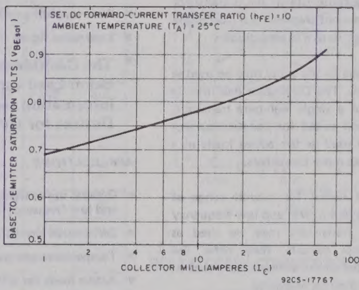


Fig.6 – V_{BEsat} vs I_C

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

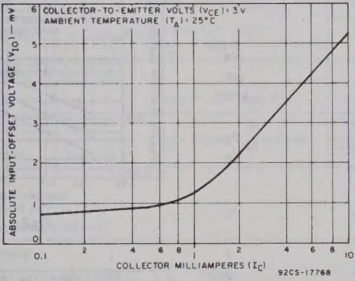


Fig.7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

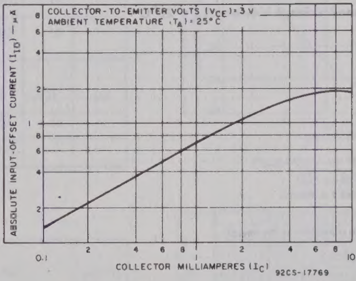


Fig.8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

CA3084

General-Purpose P-N-P Transistor Array

RCA-CA3084 is a general-purpose silicon p-n-p transistor array incorporating two independent transistors, a Darlington circuit, and a current-mirror pair with a shared diode.

The two independent transistors in the array may be used in a variety of circuit applications. The Darlington pair may be employed as the equivalent of a single high-beta transistor. The current-mirror pair is well suited for constant-current applications and can also be used as the active loads in a differential amplifier which uses n-p-n transistors.

The total array is especially useful for a wide range of applications in systems having low-power and low-frequency requirements. Although the transistors may be used as discrete units in conventional circuits, they offer the advantages inherent in integrated-circuit construction, that is, to provide close electrical and thermal matching.

The CA3084 utilizes the 14-lead dual-in-line plastic package.

FEATURES

- Matched transistor pair (Q1 and Q2)
  - V_{IO} (V_{BE} matched): ± 6mV max.
  - I_{IO} (at 100 μA): ± 0.6 μA
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz
- **The CA3084 is available in a sealed-junction Beam-Lead version (CA3084L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

APPLICATIONS

- General use in signal processing systems having low-power and low-frequency requirements
- Differential amplifiers
- Temperature compensated amplifiers
- Active loads for differential amplifiers using n-p-n transistors
- Complementary uses with RCA n-p-n transistor arrays

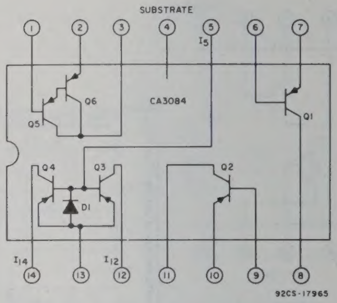


Fig.1 – Functional diagram of the CA3084.

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

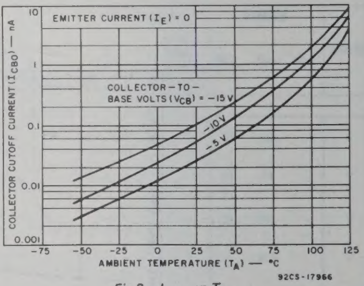


Fig.2 – I_{CBO} vs T_A.

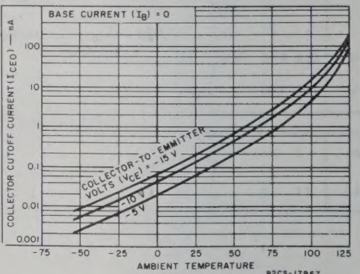


Fig.3 – I_{CEO} vs T_A.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Dissipation:		
Any one transistor	200	mW
Total package	750	mW
Above T_A = 55°C	derate linearly6.67	mW/°C
Ambient Temperature Range:		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
Lead Temperature (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	–40	V
Collector-to-Base Voltage (V_{CBO})	–40	V
Base-to-Substrate Voltage (V_{BIO})*	40	V
Emitter-to-Base Voltage (V_{EBO})	–40	V
Collector Current (I_C)	–10	mA

*The base of each transistor of the CA3084 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any base voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (4) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

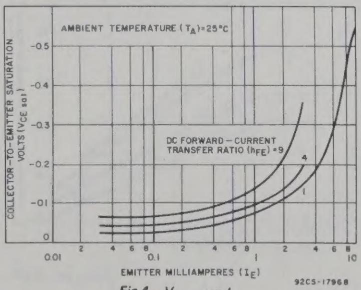


Fig.4 – V_{CEsat} vs I_E.

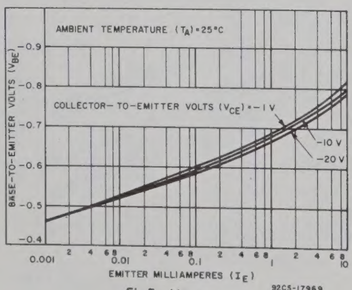


Fig.5 – V_{BE} vs I_E.

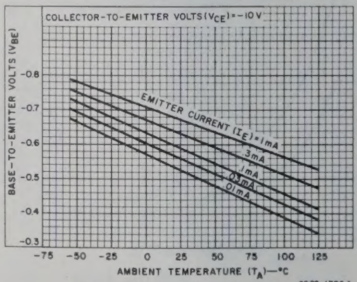


Fig.6 – V_{BE} vs T_A.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Characteristics Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-Cutoff Current	I_{CBO}	V_{CB} = −10V, I_E = 0	2	–	−0.055	−100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	3	–	−0.12	−100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_{CE} = −100μA, I_B = 0	–	−40	−70	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_{CB} = −100μA, I_E = 0	–	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_{EB} = −100μA, I_C = 0	–	−40	−100	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 100μA	–	40	100	–	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_E = 1mA, I_B = 100μA	4	–	−0.125	−0.25	V
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	5	−0.50	−0.59	−0.68	V
DC Forward-Current Transfer Ratio	h_{FE}		7	15	40	–	
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Magnitude of Input Offset Voltage	$\|V_{IO}\|$	I_E = 100μA, V_{CE} = −10V	8	–	0.422	6	mV
Input Offset Current	I_{IO}		–	−0.6	0	0.6	μA
For Transistors Q3 and Q4 (Current-Mirror Configuration):							
Collector Current (Normalized)	I_C/I_5	V_{CE} = −5V, V_{CIO} = −5V, Term. 13 = Gnd. I_5 = −100μA,	10	0.85	1.00	1.15	
Magnitude of Collector Current Ratio	$\|I_C(Q3)/I_C(Q4)\|$		11	0.90	1.00	1.10	
For Transistors Q5 and Q6 (Darlington Configuration):							
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	–	–	–	−1.0	μA
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	13	0.92	1.07	1.20	V
DC Forward-Current Transfer Ratio	h_{FE}		15	100	1230	–	

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only For Design Guidance

Magnitude of Temperature Coefficient:							
V_{BE} (for each transistor)	$\|\Delta V_{BE}/\Delta T\|$	I_E = 100μA, V_{CE} = −10V	6		−1.78		mV/°C
V_{IO} (as a differential amplifier)	$\|\Delta V_{IO}/\Delta T\|$		9		0.54		μV/°C
V_{BE} (Darlington configuration)	$\|\Delta V_{BE}/\Delta T\|$		14		−3.7		mV/°C
For Each Transistor:							
Input Resistance	R_I	f = 1kHz, V_{CE} = −10V, I_C = −100μA	19		9		kΩ
Output Resistance	R_O		20	–	600	–	kΩ
Forward Transconductance	g_m		22	–	3	–	mmho
Collector-to-Base Capacitance	C_{CBO}	I_{CB} = 0	23	–	3.3	–	pF
Collector-to-Emitter Capacitance	C_{CEO}	I_{CE} = 0	23	–	2.5	–	pF
Base-to-Substrate Capacitance	C_{BIO}	I_{CIO} = 0	23	–	4.5	–	pF

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

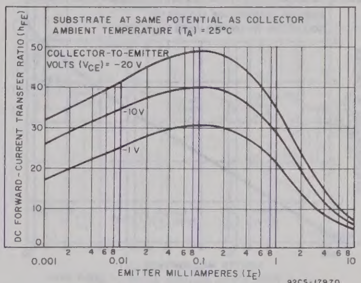


Fig.7 – h_{FE} vs I_E.

STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

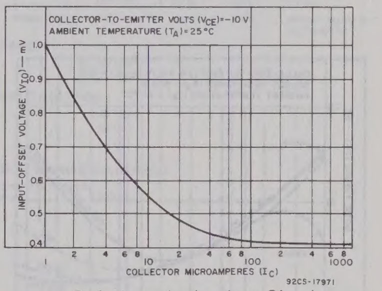


Fig.8—V_{IO} vs I_C, (transistors Q1 and Q2 as a differential amplifier).

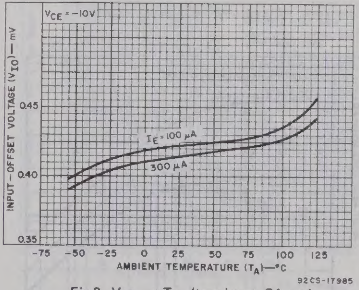


Fig.9—V_{IO} vs T_A (transistors Q1 and Q2 as a differential amplifier).

STATIC CHARACTERISTICS FOR CURRENT-MIRROR CONFIGURATION

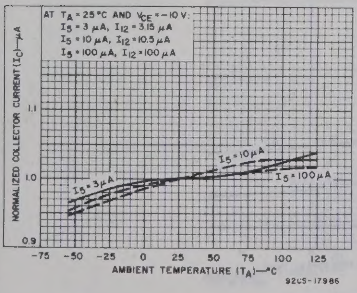


Fig.10—Normalized I_C vs T_A (transistors Q3 and Q4 in a current-mirror configuration).

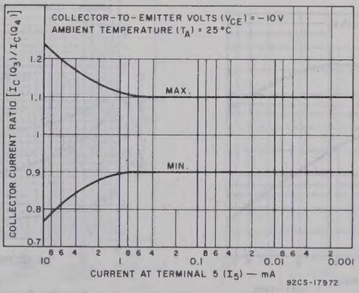


Fig.11—I_C ratio vs I_5 (transistors Q3 and Q4 in a current-mirror configuration.

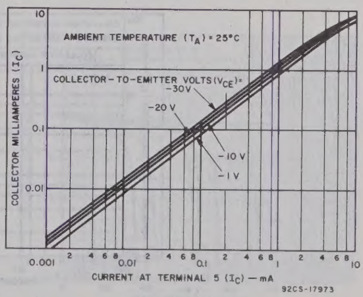


Fig.12 – I_C vs I_5 (transistors Q3 and Q4 in a current-mirror configuration).

STATIC CHARACTERISTICS FOR DARLINGTON CONFIGURATION

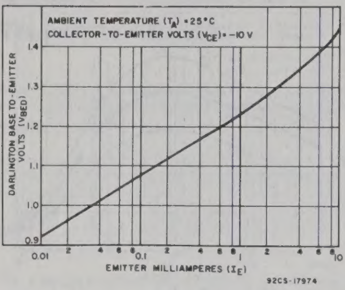


Fig.13 – V_{BE} vs I_E (transistors Q5 and Q6 in a darlingtron configuration).

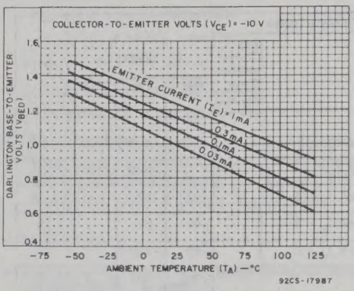


Fig.14 – V_{BE} vs T_A (transistors Q5 and Q6 in a darlington configuration).

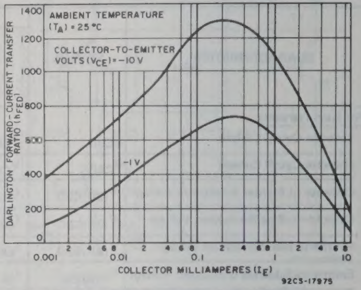


Fig.15 – h_{FE} vs. I_E (transistors Q5 and Q6 in a darlington configuration).

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

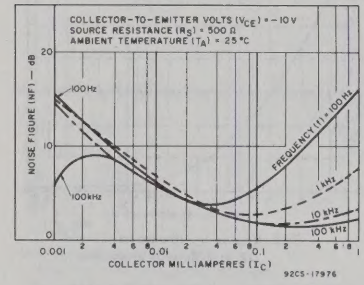


Fig.16 – NF vs I_C at R_S = 500 Ω

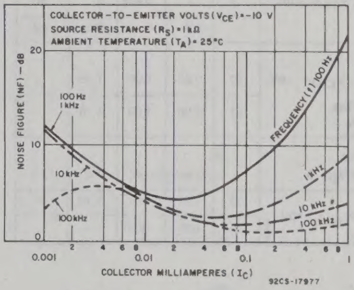


Fig.17 – NF bs I_C at R_S = 1 kΩ

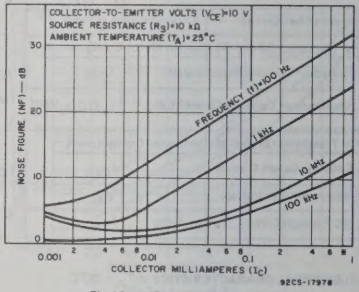


Fig.18 – NF vs I_C at R_S = 10kΩ

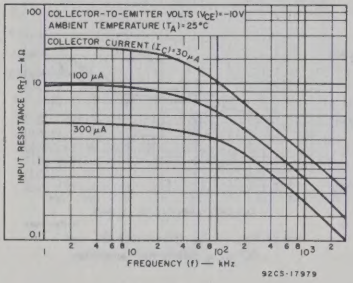


Fig.19 – R_I vs f

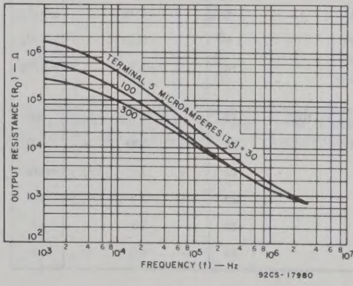


Fig.20 – R_O vs f

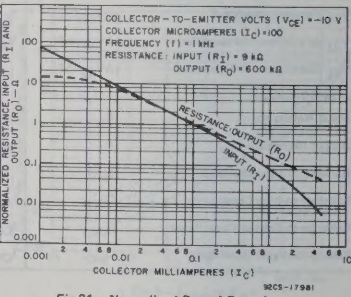


Fig.21 – Normalized R_I and R_O vs I_C

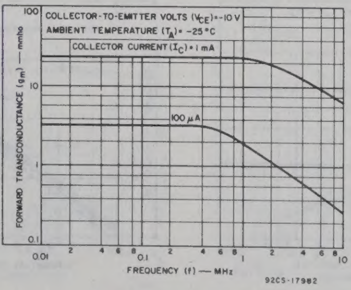


Fig.22 – g_m vs f

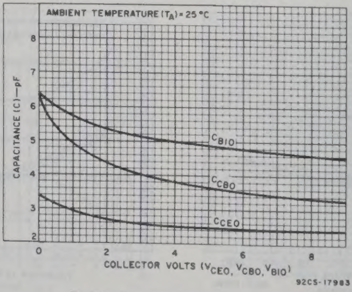


Fig.23 – Transistor capacitances vs collector voltages (V_{CEO}, V_{CBO}, V_{CIO})

Positive Voltage Regulators

For Regulated Voltages from 1.7V to 46V at Currents up to 100mA

RCA-CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30 V (CA3085), 7.5 to 40 V (CA3085A), and 7.5 to 50 V (CA3085B) and a minimum regulated output voltage of 26 V (CA3085), 36 V (CA3085A), and 46 V (CA3085B).

The CA3085A is unilaterally interchangeable with the CA3055.

The CA3085 is available in a sealed-junction Beam-Lead version (CA3085L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

Type	V_{IN} Range V	V_{OUT} Range V	Max I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

These types are supplied in the 8-lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8-lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS, CA3085BS). The CA3085 is also supplied in the 8-lead dual-in-line plastic package ("MINI-DIP", CA3085E), and in chip form (CA3085H).

Features

- **Up to 100mA output current**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.025%**
- **Pin compatible with LM100 Series**
- **Adjustable output voltage**
- Low noise

Applications

- **Shunt voltage regulator**
- **Current regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Combination positive and negative voltage regulator**
- **Dual tracking regulator**
- See Application Note ICAN-6157 "Applications of the CA3085-Series Monolithic IC Voltage Regulators".

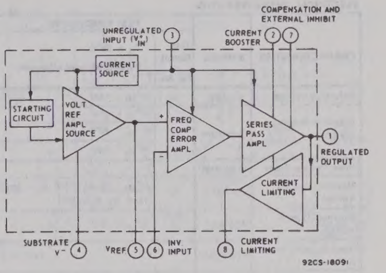


Fig.1—Block diagram of CA3085 Series.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

POWER DISSIPATION: WITHOUT HEAT SINK | WITH HEAT SINK (TO-5 ONLY)

WITHOUT HEAT SINK		WITH HEAT SINK (TO-5 ONLY)	
up to T_A = 55°C	630 mW	up to T_C = 55°C	1.6 W
above T_A = 55°C	derate linearly @6.67 mW/°C	above T_C = 55°C	derate linearly at 16.7 mW/°C

TEMPERATURE RANGE:

Operating	−55 to +125°C
Storage	−65 to +150°C

UNREGULATED INPUT VOLTAGE:

CA3085	30 V
CA3085A	40 V
CA3085B	50 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max .... +265°C

Maximum Voltage Ratings
The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	*	*	*	*	*	+10 0
6	–	–	*	*	*	*	*	*
7	–	–	–	+3 −10	+3 −10	*	*	+‡ 0
8	–	–	–	–	+5 −1	*	*	*
1	–	–	–	–	–	+10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

* Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30V for CA3085
40V for CA3085A
50V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

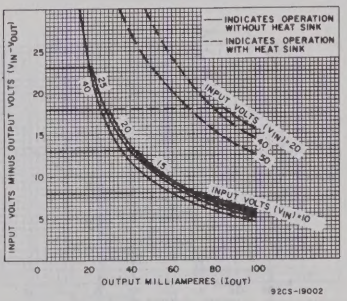


Fig.3—Dissipation limitation ($V_{IN}-V_{OUT}$ vs. I_{OUT}).

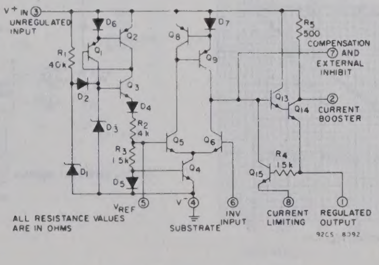


Fig.2—Schematic diagram of CA3085 Series.

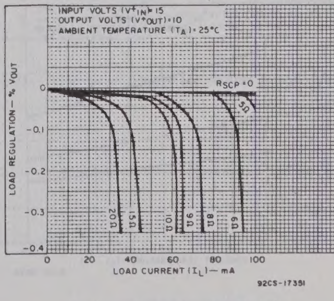


Fig.4—Load regulation characteristics.

CA3085, CA3085A, CA3085B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: Test Circuit Fig. No.	TEST CONDITIONS: $T_A = 25^\circ C$ [Unless indicated otherwise]	CA3085 MIN.	CA3085 TYP.	CA3085 MAX.	CA3085A MIN.	CA3085A TYP.	CA3085A MAX.	CA3085B MIN.	CA3085B TYP.	CA3085B MAX.	UNITS
Reference Voltage	V_{REF}	15	V^+_{IN} = 15V	1.4	1.6	1.8	1.5	1.6	1.7	1.5	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	15	V^+_{IN} = 30V	–	3.3	4.5	–	–	–	–	–	–	mA
			V^+_{IN} = 40V	–	–	–	–	3.65	5	–	–	–	
			V^+_{IN} = 50V	–	–	–	–	–	–	–	4.05	7	
Input Voltage Range	$V_{IN(range)}$	–	–	7.5	–	30	7.5	–	40	7.5	–	50	V
Maximum Output Voltage	$V_{O(max.)}$	15	V^+_{IN} = 30, 40, 50V#, R_L = 365 Ω, Term. No. 6 to Gnd.	26	27	–	36	37	–	46	47	–	V
Minimum Output Voltage	$V_{O(min.)}$	15	V^+_{IN} = 30V	–	1.6	1.8	–	1.6	1.7	–	1.6	1.7	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–	–	4	–	28	4	–	38	3.5	–	48	V
Limiting Current	I_{LIM}	16	V^+_{IN} = 16V, V^+_{OUT} = 10V, R_{SCP}* = 6 Ω	–	96	120	–	96	120	–	96	120	mA
Load Regulation●	–	–	I_L = 1 to 100mA, R_{SCP} = 0	–	–	–	–	0.025	0.15	–	0.025	0.15	%V_{OUT}
		–	I_L = 1 to 100mA, R_{SCP} = 0, T_A = 0°C to +70°C	–	–	–	–	0.035	0.6	–	0.035	0.6	
		–	I_L = 1 to 12mA, R_{SCP} = 0	–	0.003	0.1	–	–	–	–	–	–	
Line Regulation▲	–	–	I_L = 1 mA, R_{SCP} = 0	–	0.025	0.1	–	0.025	0.075	–	0.025	0.04	%/V
		–	I_L = 1mA, R_{SCP} = 0, T_A = 0°C to +70°C	–	0.04	0.15	–	0.04	0.1	–	0.04	0.08	
Equivalent Noise Output Voltage ■	V_{NOISE}	12	V^+_{IN} = 25V, C_{REF} = 0	–	0.5	–	–	0.5	–	–	0.5	–	mV p-p
			V^+_{IN} = 25V, C_{REF} = 0.22μF	–	0.3	–	–	0.3	–	–	0.3	–	
Ripple Rejection	–	13	V^+_{IN} = 25V, f = 1kHz, C_{REF} = 0	–	50	–	–	50	–	45	50	–	dB
			V^+_{IN} = 25V, f = 1kHz, C_{REF} = 2μF	–	56	–	–	56	–	50	56	–	
Output Resistance	r_o	13	V^+_{IN} = 25V, f = 1kHz	–	0.075	1.1	–	0.075	0.3	–	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	ΔV_{REF}, ΔV_o	–	I_L = 0, V_{REF} = 1.6V	–	0.0035	–	–	0.0035	–	–	0.0035	–	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	14	V^+_{IN} = 25V, +50mA Step	–	1	–	–	1	–	–	1	–	μs
Turn Off	t_{OFF}		V^+_{IN} = 25V, -50mA Step	–	3	–	–	3	–	–	3	–	μs
Line Transient Recovery Time: Turn On	t_{ON}	–	V^+_{IN} = 25V, f = 1kHz, 2V Step	–	0.8	–	–	0.8	–	–	0.8	–	μs
Turn Off	t_{OFF}	–		–	0.4	–	–	0.4	–	–	0.4	–	μs

# 30V (CA3085), 40V(CA3085A), 50V(CA3085B)

* RSCP: Short-circuit protection resistance

■ Bandwidth DC to 10 MHz.

● Load Regulation = $\dfrac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\dfrac{(\Delta V_{OUT})}{(V_{OUT(initial)})\ (\Delta V_{IN})} \times 100\%$

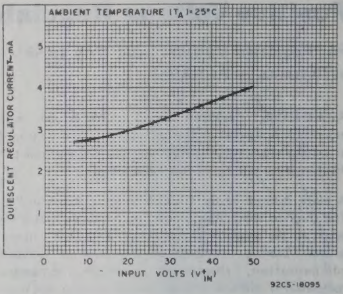


Fig.5—$I_{quiescent}$ vs. V^+_{IN}.

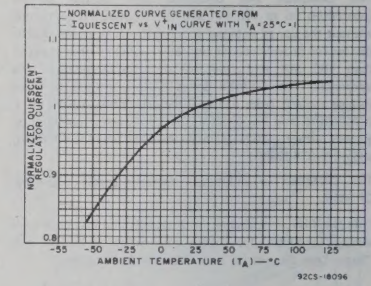


Fig.6—Normalized $I_{quiescent}$ vs. T_A.

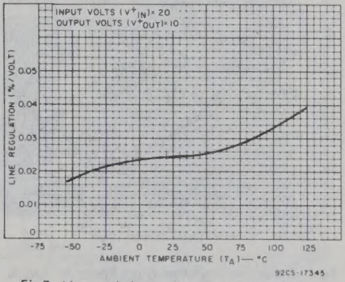


Fig.7—Line regulation temperature characteristics.

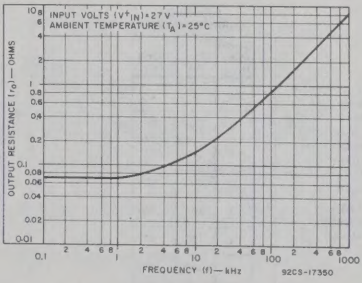


Fig.8—r_o vs. f.

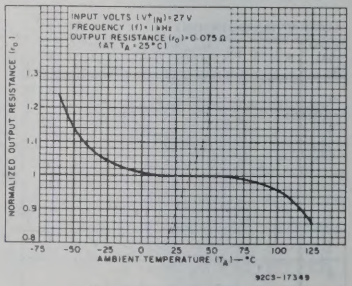


Fig.9—Normalized r_o vs. T_A.

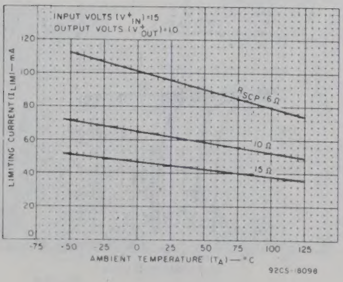


Fig.10—I_{LIM} vs. T_A.

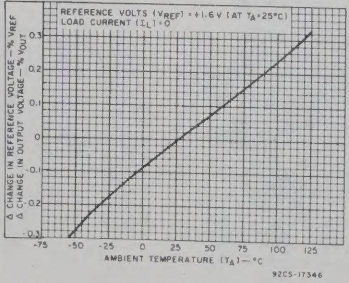


Fig.11—Temperature coefficient of V_{REF} and V_{OUT}.

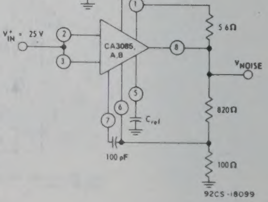


Fig.12—Test circuit for noise voltage.

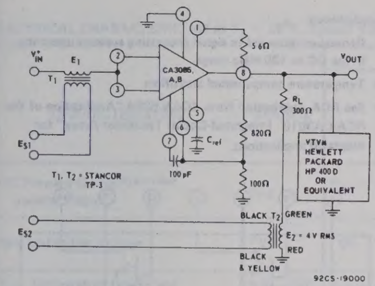


Fig.13– Test circuit for ripple rejection and output resistance.

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1 kHz so that E_2 = 4V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}\,(R_L/E_2)$

Ripple Rejection – I

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1 kHz so that E_1 = 3V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection – II

Conditions

1. Repeat Ripple Rejection I with C_{REF} = 2 μF

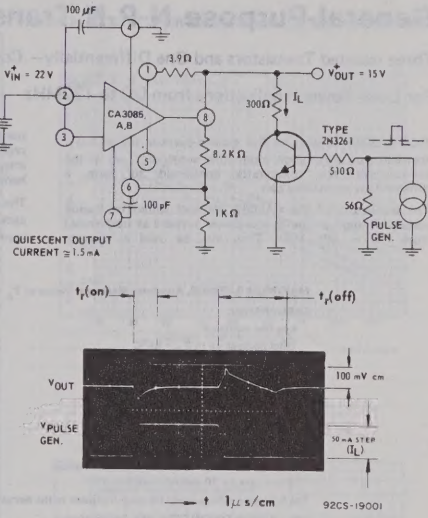
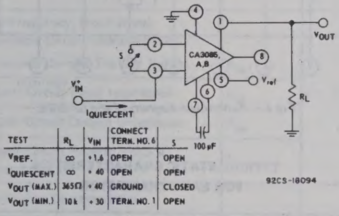
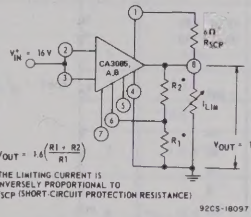


Fig.14– Turn-on and turn-off recovery time test circuit with associated waveforms.



TEST	R_L	V_{IN}	CONNECT TERM. NO. 6	S
$V_{REF.}$	∞	+1.6	OPEN	OPEN
$I_{QUIESCENT}$	∞	+40	OPEN	OPEN
V_{OUT} (MAX.)	365Ω	+40	GROUND	CLOSED
V_{OUT} (MIN.)	10 k	+30	TERM. NO. 1	OPEN

Fig.15– Test circuit for V_{REF}, $I_{quiescent}$, V_{OUT}(max.), V_{OUT}(min.).

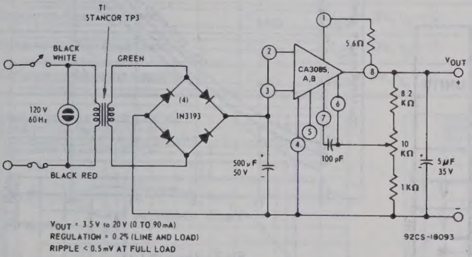


$*V_{OUT} = 1.6\left(\frac{R1 + R2}{R1}\right)$

*THE LIMITING CURRENT IS INVERSELY PROPORTIONAL TO R_{SCP} (SHORT-CIRCUIT PROTECTION RESISTANCE)

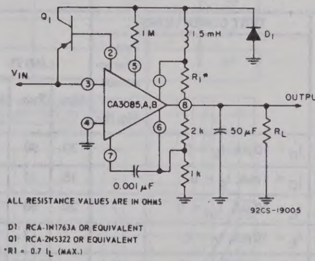
Fig.16– Test circuit for limiting current

TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES



V_{OUT} = 3.5 V to 20 V (0 TO 90 mA)
REGULATION = 0.2% (LINE AND LOAD)
RIPPLE < 0.5 mV AT FULL LOAD

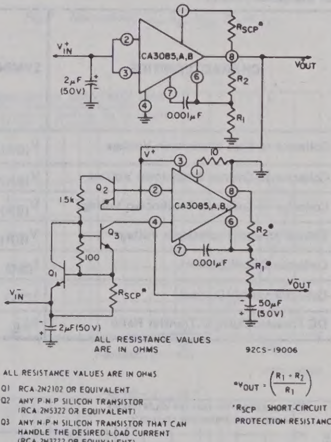
Fig.17– Application of the CA3085 Series in a typical power supply.



ALL RESISTANCE VALUES ARE IN OHMS

D1 RCA-1N1763A OR EQUIVALENT
Q1 RCA-2N5322 OR EQUIVALENT
*R1 = 0.7 I_L (MAX.)

Fig.18– Typical switching regulator circuit.



ALL RESISTANCE VALUES ARE IN OHMS

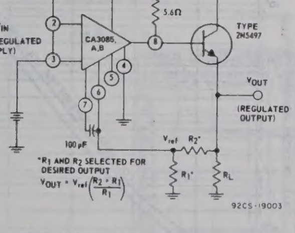
ALL RESISTANCE VALUES ARE IN OHMS

Q1 RCA-2N2102 OR EQUIVALENT
Q2 ANY P-N-P SILICON TRANSISTOR (RCA-2N5322 OR EQUIVALENT)
Q3 ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE THE DESIRED LOAD CURRENT (RCA-2N3772 OR EQUIVALENT)

$*V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)$

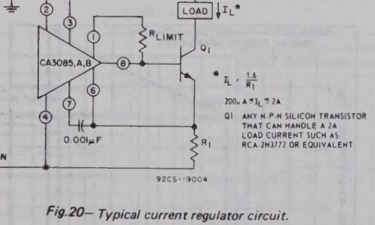
*R_{SCP} SHORT-CIRCUIT PROTECTION RESISTANCE

Fig.21– Combination positive and negative voltage regulator circuit.



*R_1 AND R_2 SELECTED FOR DESIRED OUTPUT
$V_{OUT} = V_{ref}\left(\frac{R_2 + R_1}{R_1}\right)$

Fig.19– Typical high-current voltage regulator circuit.



$* I_L = \frac{1.6}{R_1}$

200 μA ≤ I_L ≤ 2A

Q1 ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE A 2A LOAD CURRENT SUCH AS RCA-2N3772 OR EQUIVALENT

Fig.20– Typical current regulator circuit.

CA3086

General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially– Connected Transistor Pair

For Low–Power Applications from DC to 120MHz

RCA-CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

Applications

- **General-purpose use in signal processing systems operating in the DC to 120-MHz range**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

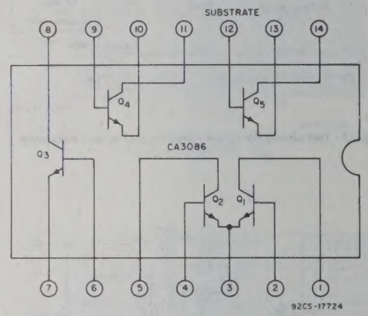


Fig.1 – Functional diagram of the CA3086.

MAXIMUM RATINGS, Absolute–Maximum Values at T_A = 25°C

DISSIPATION:		
Any one transistor	300	mW
Total package up to T_A = 55°C	750	mW
Above T_A = 55°C	derate linearly 6.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−55 to + 125	°C
Storage	−65 to + 150	°C
LEAD TEMPERATURE (During soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) From case for 10 seconds max.	+ 265	°C
The following ratings apply for each transistor in the device:		
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	20	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}*	20	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT, I_C	50	mA

* The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS			UNITS
			Typ. Characteristic Curves Fig. No.	Min.	Typ.	Max.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0	–	5	7	–	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	2	–	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	3	—	See Curve	5	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 1mA	4	40	100	–	

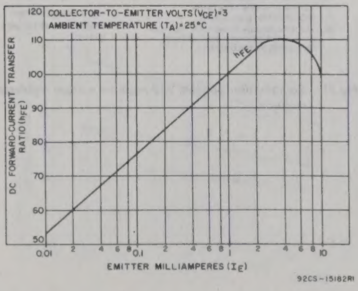


Fig.3 – h_{FE} vs I_E.

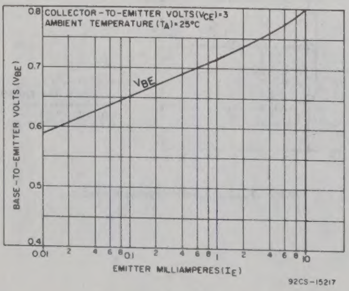


Fig.4 V_{BE} vs I_E.

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

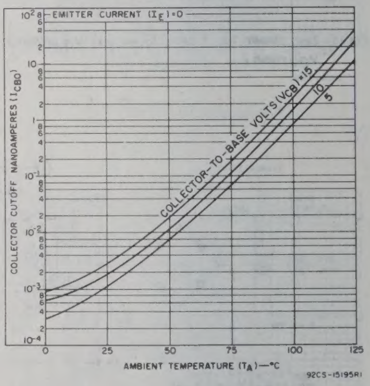


Fig.2 – I_{CBO} vs T_A.

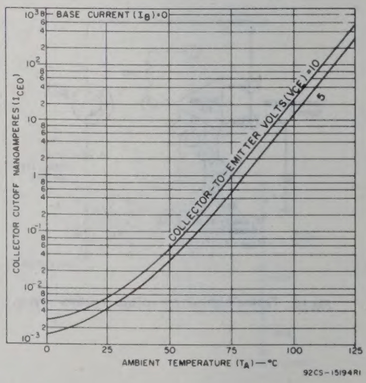


Fig.5 – I_{CEO} vs T_A.

ELECTRICAL CHARACTERISTICS at T_A = 25°C Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		–	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1 kΩ		–	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	–
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8 X 10^{-4}	–
Admittance Characteristics:						
Forward Transfer Admittance	y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 – j1.5	mmho
Input Admittance	y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	y_{re}			11	See Curve	–
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		–	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		–	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		–	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

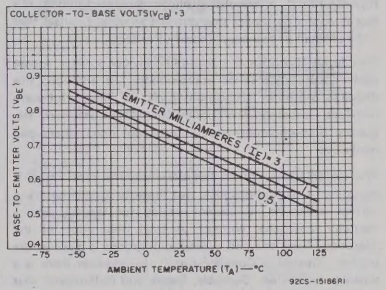


Fig.6 – V_{BE} vs T_A.

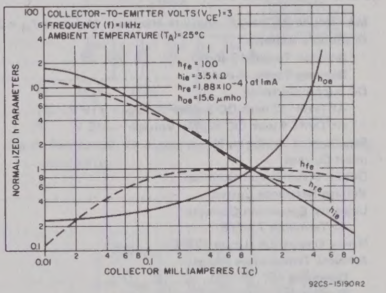


Fig.7 – Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

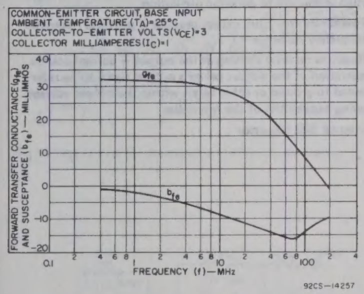


Fig.8 – y_{fe} vs f.

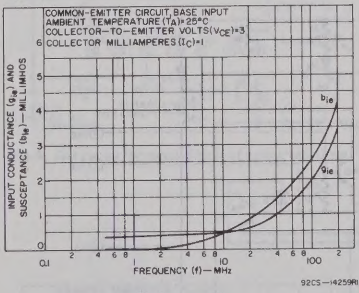


Fig.9 – y_{ie} vs f.

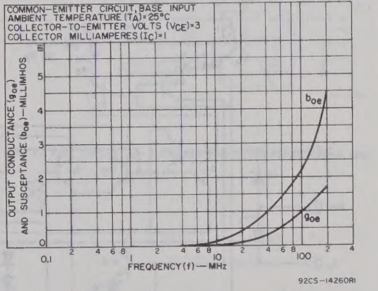


Fig.10 – y_{oe} vs f.

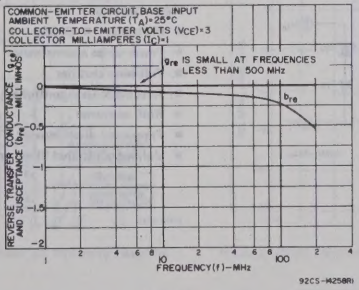


Fig.11 – y_{re} vs f.

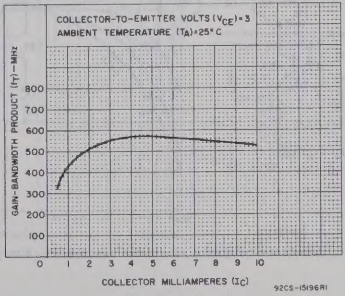


Fig.12 – f_T vs I_C.

CA3091D
Analog Multiplier

RCA-CA3091D, a monolithic silicon integrated circuit, is a four-quadrant multiplier that provides an output voltage that is the product of two input (x and y) voltages.

This device functions as a multiplier, divider, squarer, square rooter, and power-series approximator. In addition, this device is useful in applications such as ideal full-wave rectifiers, automatic level controllers, RMS converters, frequency discriminators, and voltage–controlled filters and oscillators.

The CA3091D comprises five basic circuits (See Fig. 1), including: a multiplier block, two linearity compensators, a current converter, a current source for biasing, and a regulator (reference voltage). A brief description of the operation, functions and typical applications is given in the section "Operating Considerations". In addition there is a separate section on "Symbols, Terms, and Definitions" that defines the terms and symbols used throughout the data bulletin.

The CA3091D is supplied in 14-lead dual-in-line ceramic package and operates over the full military temperature range of -55°C to +125°C.

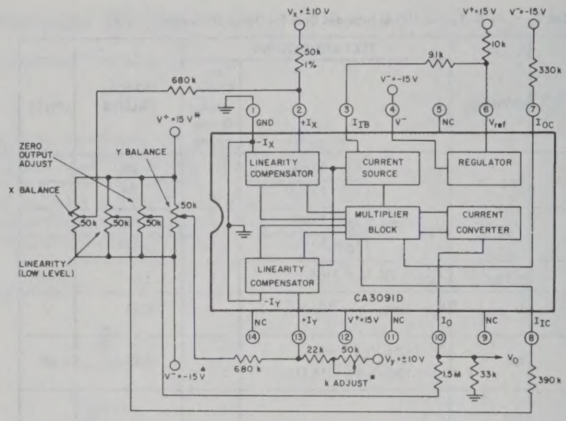


Fig.1—Functional block diagram of CA3091D with typical multiplier outboard(peripheral)circuitry.

* FROM 15-VOLT REGULATED SUPPLY

▲ FROM -15-VOLT REGULATED SUPPLY

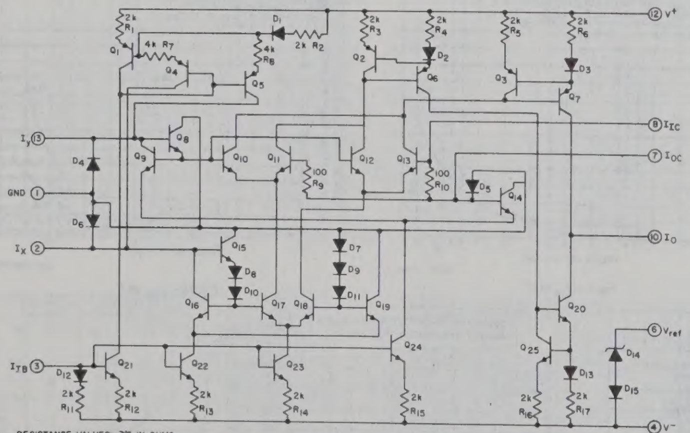
● k ADJUST IS PERFORMED BY VARYING THIS RESISTOR

RESISTANCE VALUES ARE IN OHMS

MAXIMUM RATINGS; *Absolute-Maximum Values at $T_A = 25^oC$*

DC Supply Voltages:		
Between Terms. 12 and 1	+18	V
Between Terms. 4 and 1	−18	V
DC Supply Currents:		
At Term. 12 with DC Supply Voltage = +15 V	4	mA
At Term. 4 with DC Supply Voltage = −15 V	16	mA
Bias Current (At Term. 3)	1	mA
* Input Current	±1	mA
Output Short-Circuit Duration	No limitation	
Voltage Reference Current	10	mA
Linearity Correction Currents:		
At Terminals 7 and 8	10	mA
Device Dissipation (Up to 125°C)	200	mW
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (during soldering):		
At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265	°C

* External resistance is required to limit the current to the indicated ±1 mA value.



RESISTANCE VALUE IN OHMS

Fig.2—Schematic diagram of the CA3091D.

Features: ●

- "Accuracy": ±4% (max.)
- "Linearity": 3.0% (max.)
- Feedthrough: 9 mV p-p (typ.)
- 3-db bandwidth: 4.4 MHz
- Low power operation capability: ±6.0 V, 4 mW drain
- Low power-supply sensitivity: 36 mV/V typ.
- Smooth overload characteristics – no foldback if full-scale input signal is exceeded
- Negligible warm-up drift
- Broadband operation capability (flat to 1 MHz) – both inputs have similar characteristics for reduced high-frequency phase shift between the inputs
- Low-level linearity correction circuitry minimizes low-level feedthrough for improved small-signal accuracy
- All multiplication is performed with wideband circuitry – this permits two signals of frequencies much higher than the -3 db frequency of the multiplier to produce a difference frequency that is within the multipliers bandwidth
- High immunity to parasitic oscillation
- Essentially free from excess peaking – provides improved frequency response
- Requires no level shifting at the output – current-source operation at the output permits output signal to be referenced to ground or other levels within the output voltage swing capabilities of the multiplier
- Internal bias regulator

Applications:

- Multiplier ■ Divider ■ Squarer ■ Square Rooter
- Power-series approximator
- Full-wave rectifier
- Automatic level controller
- RMS converter
- Frequency discriminator
- Voltage-controlled filters and oscillators

ELECTRICAL CHARACTERISTICS, For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C, I_{IB} = 0.5 mA V^+ = 15 V, V^- = -15 V	Circuit and/or Char. Curve	LIMITS Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
INPUT CIRCUIT							
Input Balance (Correction) Currents:							
At x Input	I_{IC}	x = 0	–	−20	−2.1	+20	μA
At y Input		y = 0	–	−20	−8.7	+20	μA
Feedthrough Linearity Balance (Correction) Current	I_{OC}		–	−34	−2.9	+34	μA
OUTPUT CIRCUIT							
Output Offset Current	I_{OO}	x & y = 0,	–	−10	−0.23	+10	μA
Output Offset Voltage	V_{OO}	I_{OO} thru R_L = 33kΩ	–	−0.330	−0.0076	+0.330	V
Output Peak Current Swing	$\lvert I_O \rvert$	Thru R_L = 24kΩ	3	0.41	0.45	–	mA
Output Peak Voltage Swing	$\lvert V_O \rvert$	Across R_L = 33kΩ	4	12	12.9	–	V
DC SUPPLIES & BIASING							
Current Drain (Idling):							
At Term. 4		V^- = -15 V	–	–	2.9	4.5	mA
At Term. 12		V^+ = +15 V	–	–	2.0	3.0	mA
Reference Voltage	V_{ref}	Measured across Terms. 6 & 4 at I = 1mA	–	5.5	6.1	6.7	V
DYNAMIC CHARACTERISTICS							
Output Current	I_O	With I = 0.2mA at each input	–	–	0.21	0.32	mA
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$			11	0.69	1.0	1.7	
Accuracy		Worst case at 25°C	–	–	2.6	4.0	% of 10 V
Linearity				–	1.7	3.0	
Feedthrough Voltage:							
At y = 20V p-p, x = 0			–	–	9	20	mV p-p
At x = 20V p-p, y = 0			–	–	9	20	

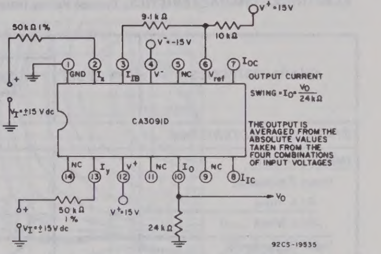


Fig.3–Test circuit for measurement of output current swing capability.

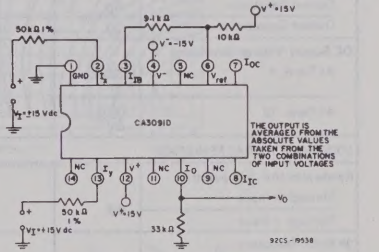


Fig.4–Test circuit for measurement of output voltage swing capability.

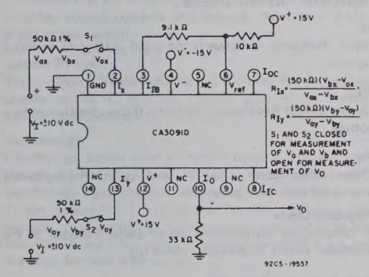
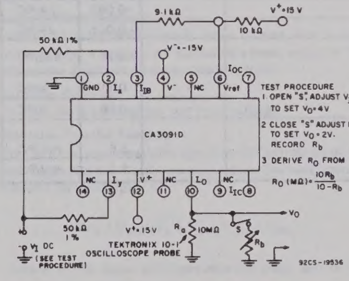


Fig.5–Test circuit for measurement of input resistance.



9.1kΩ
V+=15V
10kΩ
50kΩ 1%
V−=−15V
GND
I_x
I_{IB}
V^-
NC
V_{ref}
I_{OC}
TEST PROCEDURE
1 OPEN "S", ADJUST V_I TO SET V_O=4V
2 CLOSE "S" ADJUST R_b TO SET V_O=2V. RECORD R_b
3 DERIVE R_O FROM R_O (MΩ) = $\frac{10R_b}{10-R_b}$
CA3091D
NC
I_y
V+
I_O
I_{IC}
50kΩ 1%
V+=15V
R_a
10MΩ
S
R_b
V_O
V_I DC (SEE TEST PROCEDURE)
TEKTRONIX 10-1 OSCILLOSCOPE PROBE
92CS-19536

Fig.6–Test circuit for measurement of output resistance.

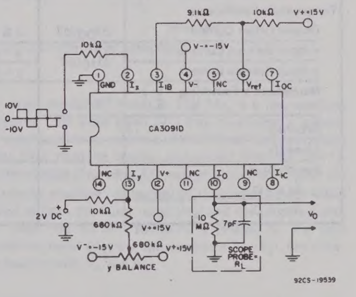


Fig.7–Test circuit for measurement of maximum slew rate.

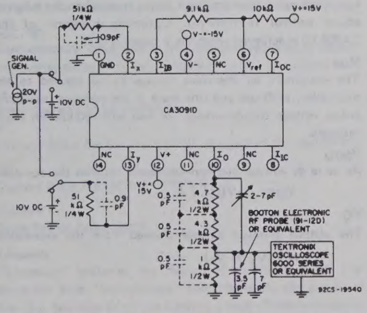


Fig.8–Test circuit for measurement of frequency response.

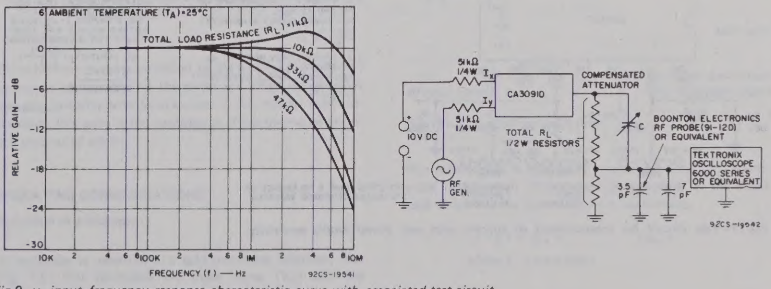
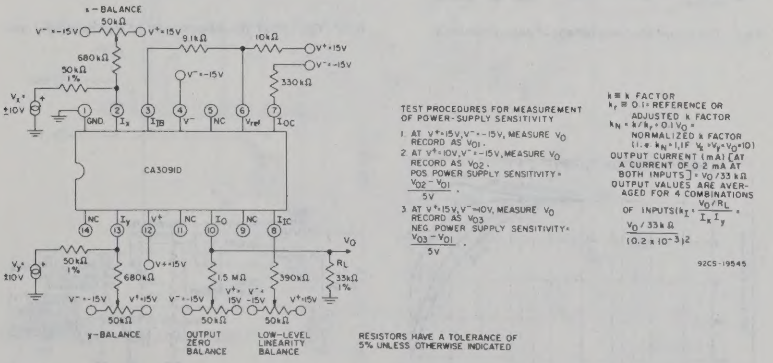


Fig.9- y–input frequency response characteristic curve with associated test circuit.

CA3091D

ELECTRICAL CHARACTERISTICS, Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
		T_A = 25°C, I_{IB} = 0.5 mA V^+ = 15 V, V^- = −15 V	Circuit and/or Char. Curve		
STATIC CHARACTERISTICS					
INPUT CIRCUIT					
Input Resistance:					
At x Input	R_I	$\lvert I_x\rvert \le 0.2$ mA	5	1.3	kΩ
At y Input		$\lvert I_y\rvert \le 0.2$ mA		0.5	kΩ
Input Capacitance:					
At x Input	C_I	at 1 MHz	–	5.8	pF
At y Input				5.8	pF
OUTPUT CIRCUIT					
Output Resistance	R_O		6	1.0	MΩ
Output Capacitance:	C_O	at 1 MHz		4.0	pF
DC Supply Voltage Sensitivity:					
At Term. 4	$\frac{\Delta V_O}{\Delta V^-}$		11	26	mV/V
At Term. 12	$\frac{\Delta V_O}{\Delta V^+}$			36	mV/V
DYNAMIC CHARACTERISTICS					
Bandwidth (At -3dB point):					
Through x Input	BW		8, 10	4.8	MHz
Through y Input			8, 9	4.4	MHz
3° Error Frequency:					
Through x Input			–	360	kHz
Through y Input				310	kHz
Maximum Slew Rate	SR	7pF in parallel with 10 MΩ load	7	27	V/μs
Temperature Coefficients:					
Output Offset Current	$\Delta I_{OO}/\Delta T$	x & y = 0	–	−0.021	μA/°C
x-Input Balance Current	$\Delta I_{IC}/\Delta T$	x = 0	–	−0.063	μA/°C
y-Input Balance Current		y = 0	–	−0.063	μA/°C
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$	k_N		–	−0.76	%/%/°C
Accuracy			–	0.11	%/°C
Linearity			–	0.06	%/°C
Feedthrough:					
At x = 0			–	5.6	mV/°C
At y = 0				5.7	mV/°C



TEST PROCEDURES FOR MEASUREMENT OF POWER-SUPPLY SENSITIVITY

1. AT V^+=15V, V^-=−15V, MEASURE V_O RECORD AS V_{O1}.
2. AT V^+=10V, V^-=−15V, MEASURE V_O RECORD AS V_{O2}. POS POWER SUPPLY SENSITIVITY = $\frac{V_{O2} - V_{O1}}{5V}$.
3. AT V^+=15V, V^-=−10V, MEASURE V_O RECORD AS V_{O3} NEG POWER SUPPLY SENSITIVITY = $\frac{V_{O3} - V_{O1}}{5V}$.

k ≡ k FACTOR
k_r ≡ 0.1 = REFERENCE OR ADJUSTED k FACTOR
k_N = k/k_r = 0.1 V_O = NORMALIZED k FACTOR (i.e. k_N = 1, IF V_x = V_y = V_O = 10)
OUTPUT CURRENT (mA) [AT A CURRENT OF 0.2 mA AT BOTH INPUTS] = V_O/33 kΩ
OUTPUT VALUES ARE AVERAGED FOR 4 COMBINATIONS OF INPUTS(k_I = $\frac{V_O/R_L}{I_x I_y}$ = $\frac{V_O/33\,k\Omega}{(0.2 \times 10^{-3})^2}$

RESISTORS HAVE A TOLERANCE OF 5% UNLESS OTHERWISE INDICATED

Fig.11–Test circuit for measurement of current gain and power-supply sensitivity.

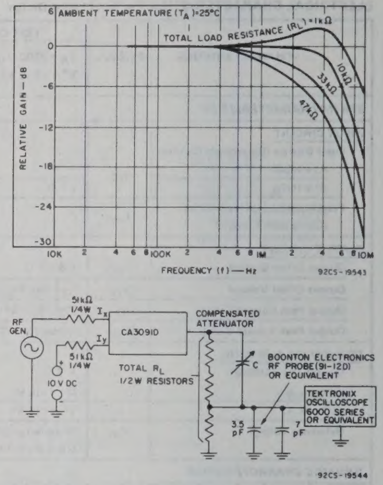


Fig.10- x–input frequency response characteristic curve with associated test circuit.

SYMBOLS, TERMS AND DEFINITIONS

Output Offset Current
The multiplier output current produced when both of the multiplier input signals are in the zero state.

Output Zero
Sets the output at the zero level when the x and y inputs are in the zero state. (It is implied that all other zeroing adjustments have been effected.)

R_I
Input Resistance – Converts the input voltage to an input current.

R_L
Output (Load) Resistance – Converts the output current to a voltage.

R_O
Output Resistance – See V_o and I_o for the equations associated with these properties.

Regulator Diode
A temperature compensated Zener diode, included in the multiplier circuit, to provide a stable I_{IB}.

Scale Factor or k factor (k)
Represents the basic gain of the multiplier as expressed in the equation $V_o = kV_xV_y$

The equation indicates the ideal transfer function for the multiplier. The normalized k factor is expressed by $k_N = k/k_{ref}$ where k_{ref} is the ideal or reference k factor. The ideal factor, k_{ref} is the value at which the k factor is set when the k-factor adjust control is trimmed. Optimum operation of the CA3091D is achieved when the k-factor is 0.1.

V_{IM}
The maximum ac sine-wave voltage to be applied to the multiplier; a 20-volt p-p sine wave is the nominal maximum swing voltage recommended for use with 50-kilohm input resistors.

V_{MID}
An ac or dc voltage that approximately satisfies the equation

$$V_{MID} = V_{IM}/\sqrt{2}.$$

V_O
The output product voltage derived from the expression

$$(kV_xV_y = V_o)$$

V_{ref}.
Temperature compensated zener connected to the −15 volt supply to provide a reference voltage as an aid in setting up a stable I_{IB}.

V_x, V_y
The input voltages to be multiplied.

x-Balance Circuit
Sets the output to the zero level when the x-input is in the zero state.

y-Balance Circuit
Sets the output to the zero level when the y-input is in the zero state.

Accuracy
Accuracy defines the degree of error encountered in the operation of the multiplier. It is portrayed on a contour map by isomers (contour lines). Isomers with the highest values indicate "less-accurate" operation of the multiplier. (See illustrative Contour Map in Fig. 12.)

Contour Map
The contour map, shown in Fig. 12, is a graphical portrayal of the multiplier errors in the x, y input plane. Each contour line, termed "isomer", connects those points whose error values (in millivolts) are equal in magnitude. For example, a −20 mV contour line with points at $V_x = 5V$ and $V_y = -3V$ indicates that the output voltage is 20 mV less than the theoretical output product (kV_xV_y). This error voltage, presented in percent of full-scale input (±10 V), defines the "accuracy" of the device. Thus, a 20-mV error voltage represents an "accuracy" of 0.2% as derived from the equation:

$$\text{Accuracy} = 20\ \text{mV}/10 \times 100\% = 0.2\%.$$

A contour map provides a true indication of multiplier performance in each of the four quadrants. Each CA3091D is comprehensively tested and must provide the specified accuracy in the four quadrants.

Current Converter
This portion of the IC combines the multiplier's differential-amplifier output currents and converts them to a single-ended output current.

Current Sources
These circuits provide the biasing currents for the various circuits in the IC. The I_{IB} terminal provides the control current for the current-source circuit.

Feedthrough
Feedthrough occurs when an output signal is produced even though one of the input signals is zero. Consequently, feedthrough signal characteristics constitute a source of error in the operation of a multiplier. In the CA3091D, for example, the feedthrough signal output is specified to be less than 20 mV p-p when either terminal is set at 20 V p-p and the other terminal is set to zero.

I_{IB}
Circuit biasing control current.

I_{IC}
See I_{OC}.

I_O
Output product current ($k_I I_x I_y = I_O$), where $k_I = kR_I^2/R_L$

I_{OC}, I_{IC}
Compensatory input and output currents required to correct unlinearity along the x axis. (Optional for low-level signal use.)

I_x, I_y
Input currents to be multiplied.

k
Voltage Scale Factor (determines the gain of the multiplier).

k_I
Current Scale Factor (k_I) = (R_I^2/R_L)k.

k adjust
Scale-Factor Adjustment.

Linearity
"Linearity" indicates the degree of multiplier error (i.e. deviation from "straight-line" characteristics) along each of the four boundaries of the input x, y field. These boundaries are formed when one input is held at one of the two maximum values (10 volts or −10 volts) and the other input is swept through the voltage range. (See Contour Map for additional information.)

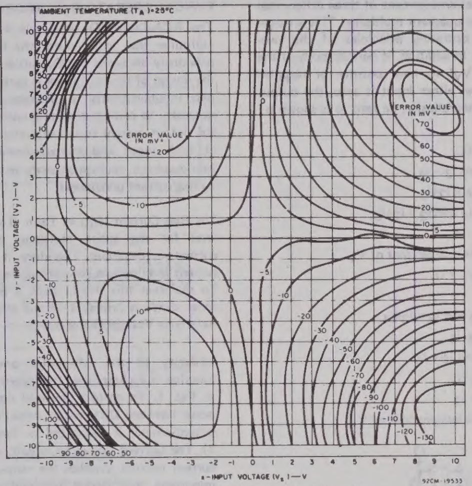


Fig.12—Contour mapping of multiplier accuracy (plotted on isomers) and linearity.

Note: See "Contour Map" in "Symbols, Terms and Definitions" Section.

Linearity Adjust
An external circuit to provide vernier adjustment for optimum linearity. This control should be adjusted before adjusting the y-balance control.

Linearity Balance Circuit (Low-Level)
This circuit makes the multiplier's transfer function linear for low-level x-input signals.

Linearity Compensator
Internal circuitry that converts input current into a non-linear voltage, a requisite for producing a linear output in the differential amplifiers of the multiplier circuit.

Multiplier Circuitry
Provides the product of the two input voltages.

Multiplier Transfer Function
This function mathematically describes the interaction of the two inputs and the resulting output signal. The basic transfer function for a multiplier is

$$k(V_x + V_{xe})\ (V_y + V_{ye}) = V_o + V_{oe}$$

where: k = k factor and represents the basic gain of the multiplier

V_x, V_y = the external inputs to be multiplied

V_o = the desired value of the product output signal

V_{xe}, V_{ye} = the "effective" errors that occur at the inputs of the multiplier and cause an output signal when either input is in a zero state.

V_{oe} = the error voltage that develops at the output of the multiplier

DC correction factors are added to the multiplier inputs and output to compensate for the errors and offset variations. A complex linearity error term appears in the transfer function; however, this term is not included in the above equation for the purpose of clarity.

OPERATING CONSIDERATIONS

Operation of a Multiplier

A multiplier is, essentially, a gain-controlled amplifier (See Fig. 13) that multiplies the input signal (V_x) with the external gain controlling signal (V_y) to produce the resultant output (V_o). The gain is externally adjustable by a coefficient (k). Stated simply, a multiplier produces an output voltage that is the linear product of two input voltages.

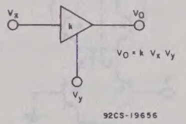
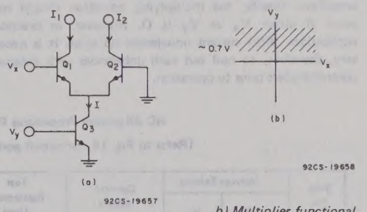


Fig.13—Gain-controlled amplifier.

The basic multiplier, shown in Fig. 14a, is a two-quadrant multiplier. The input signal (V_x) may have either a positive or negative polarity whereas, the external gain-controlling signal (V_y) must be positive and greater than the base-to-emitter voltage (Fig. 14b). The output current ($I_1 - I_2$) of the differential amplifier, comprised of transistors Q1 and Q2, is related to both the input signal (V_x) and the current source (I). Since the current source (I) is related to the gain controlling signal (V_y) the output current ($I_1 - I_2$), therefore, is related to both V_x and V_y.



a) Basic circuit.

b) Multiplier functional only in shaded region.

Fig.14—Two-quadrant multiplier.

This relationship is essentially non-linear; thus an appropriate linearization circuit must be provided in the input stage to achieve the following linear relationship:

$$I_1 - I_2 = k'\ V_x\ V_y \qquad \text{(Eq. 1)}$$

where k' is a constant

Figure 15 shows a typical arrangement of three differential amplifiers to form a four-quadrant multiplier. This arrangement incorporates the operating principles of the two-quadrant multiplier, but, in addition, it permits both of the input signals (V_x and V_y) to have positive or negative polarities (or zero). When either input is zero, the output current ($I_1 - I_2$) must, theoretically, be zero as is shown by the following:

1. Assume $V_x = 0$,
   then $i_1 = i_2$ and $i_3 = i_4$
   therefore $i_1+i_4 = i_2+i_3$.
   Since $I_1 = i_1+i_4$ and $I_2 = i_2+i_3$,
   then $I_1 = I_2$.
   This equality is independent of V_y
2. Now assume $V_y = 0$,
   then $i_5 = i_6$.
   Sine $i_5 = i_1+i_2$ and $i_6 = i_3+i_4$,
   then $i_1+i_2 = i_3+i_4$.
   Since $i_1 = i_3$ and $i_2 = i_4$
   then $i_1+i_4 = i_3+i_2$.
   Therefore $I_1 = I_2$.
   This equality is independent of V_x.

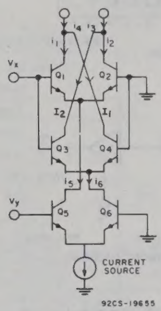


Fig.15–Basic four-quadrant multiplier.

The multiplying operation discussed in the previous section applies when neither V_x nor V_y is zero. The output current ($I_1 - I_2$) then satisfies Equation 1,

$$I_1 - I_2 = k'V_xV_y.$$

The multiplying action of the four-quadrant multiplier is dependent on current unbalance in the three differential amplifiers. Ideally, the multiplying operation should not occur if either V_x or V_y is 0. However, in practical applications slight current unbalances do exist. It is necessary, therefore, to null out such unbalances with external potentiometers prior to operation.

TYPICAL OPERATING CONSIDERATIONS

The RCA-CA3091D, shown in Fig. 2, is a four-quadrant multiplier that incorporates the basic multiplier principle, previously discussed in "Operation of a Multiplier". Because the design of this multiplier is based on the multiplication of two input currents to produce an output current it is necessary to convert the input voltages to input currents and the output current to an output voltage by inserting resistors at both input and output terminals. Fig. 1 shows the four-quadrant multiplier with its peripheral circuitry for nulling current unbalances.

The Bias Current (I_{IB}) at Term. 3 sets the operating current level for the entire multiplier circuit by means of a current-source circuit. Therefore, it is essential that this bias current level remain constant under all operating conditions. To maintain this steady state, a temperature compensated zener diode is provided on the chip and connected to the Reference Voltage (Term.6).

Linearity of the differential amplifier transconductance function is accomplished by linearity compensators as shown in Fig. 1. To correct low-level signal unbalances that may occur between Differential Amplifiers A and B, an external potentiometer is connected to Terminals 7 and 8 (See Fig. 1). The Current Converter circuit, which consists of a set of current mirrors, supplies the output current ($I_1 - I_2$). It is important that circuit unbalances be corrected prior to operation. Table I describes the alignment procedures for correcting these unbalances.

A multifunctional circuit board (Figs. 16 and 17) is available for performing the four basic applications, such as, multiplying, dividing, squaring and taking the square root.

When the CA3091D is used as a multiplier (Fig. 18) or as a squarer (Fig. 18) only the basic pheripheral circuitry on the multifunctional circuit board is utilized and the general-purpose operational amplifier (CA3741T) is disabled from operation. Follow the ac alignment procedures for these two applications before operating the circuit.

When the CA3091D is used as a divider (Fig. 20), the operational amplifier is required in order to provide the proper negative feedback. The limitations for operation as a divider are that $0 < V_y \leqslant 10V$ and $-10V \leqslant V_z \leqslant 10V$. Note, the range of V_y is limited to the positive polarity; if V_y was permitted to go negative, the feedback loop would go positive and, thereby, create an unstable operating condition.

Alignment of the divider (Fig. 19) differs from multiplier and squarer alignment because of the additional variances introduced by the operational amplifier. A coupling capacitor is provided at the output of the divider alignment circuit in order to separate the ac signal from the dc signal and, thus, avoid interaction between the calibrating potentiometers.

The alignment procedure for the square-rooter function (Fig. 21) is identical to the alignment procedure for the divider function. The input voltage range is limited to $0 < V_I \leqslant 10V$. This limitation is necessary in order to prevent the output voltage (V_O) from latching to the negative output saturation voltage of the operational amplifier. Table II describes the divider alignment procedure.

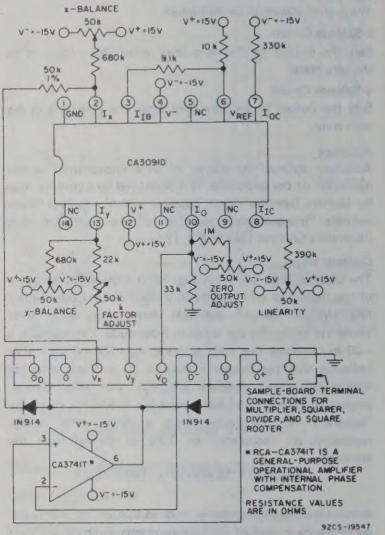
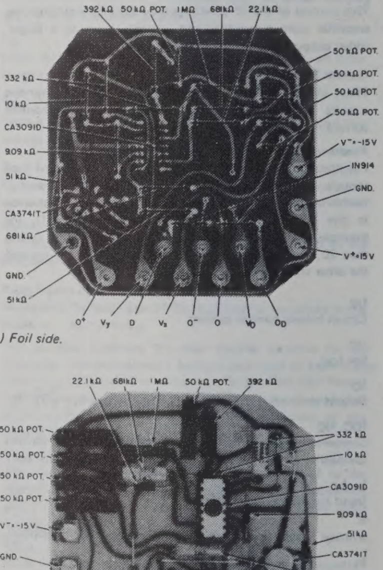
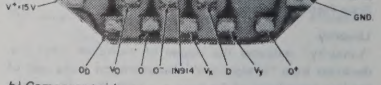


Fig.16–Typical multifunction circuit arrangement utilizing the CA3091D and CA3741T.



a) Foil side.



b) Component side.

Fig.17–Photographs of a printed-circuit board for multifunction applications (multiplier, squarer, divider, square rooter) utilizing the CA3091D and CA3741T.

Table I

AC Alignment Procedures For CA3091D, Four-Quadrant Multiplier

(Refer to Fig. 16, for circuit pertaining to following alignment procedures.)

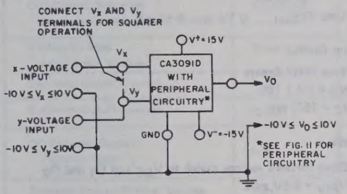
Step No.	Voltage Setting		Control Adjust	Test Equipment Used	Measure	Notes
	V_x	V_y				
1	–	–	–	–	–	Set all potentiometers to center of range.
2	O	V_{IM}	x Balance	AC VM	V_O	Adjust for a minimum reading.
3	O	V_{IM}	Linearity	AC VM	V_O	Adjust for a minimum reading.
4	–	–	–	–	–	Repeat Steps 1 and 2 until no further improvement is noted.
5	V_{IM}	O	y Balance	AC VM	V_O	Adjust for a minimum reading.
6	O	O	Zero Output	DC VM	V_O	Adjust for zero output.
7	V_{MID}	V_{MID}	R_k	AC/DC VM	V_O	Adjust for $V_{MID}^2/10$ at the output.
8	–	–	–	–	–	Check multiplier for alignment in all four quadrants.

V_{IM} – Is the maximum AC swing of the sine wave that will be applied to the multiplier. A 20-volt p-p value is the nominal maximum swing of the AC sine wave with input resistors of 50 kilohms.

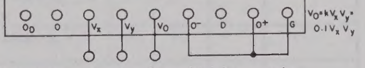
V_{MID} – An AC or DC voltage that approximately satisfies the equation $V_{MID} = V_{IM}/\sqrt{2}$. For example, if a 50-kilohm resistor is used with a 7-volt input, then R_k should be adjusted for a 4.9-volt output.

Table II — Divider Alignment Procedure

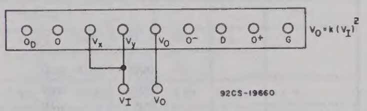
Step No.	Set		Measure	Output Coupling	Test Equipment Used	Adjust	Notes
	V_z V	V_y V					
1	–	–	–	–	–	–	Set all potentiometers to center of range.
2	0	V_S	V_O	ac	ac – VM	O_{zero}	Adjust for minimum reading.
3	0	10V dc	V_O	dc	dc – VM	$x_{balance}$	Adjust for 0V dc output.
4	V_S	V_S	V_O	ac	ac – VM	$y_{balance}$	Adjust for minimum reading.
5	5V dc	5V dc	V_O	dc	dc – VM	k_{adjust}	Adjust for 10 V dc output.



a) Circuit arrangement for multiplier or squarer operation.



b) Terminal connections for multiplying operation.



c) Terminal connections for squarer operation.

Fig.18—Multifunction circuit-board arrangement with terminal connections for multiplier and squarer operation.

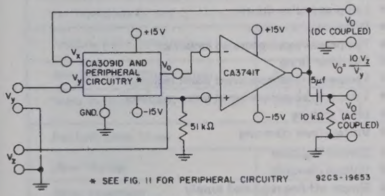


Fig.19—(a) Divider alignment circuit.

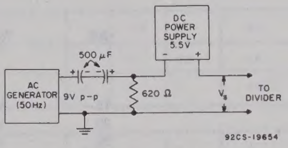
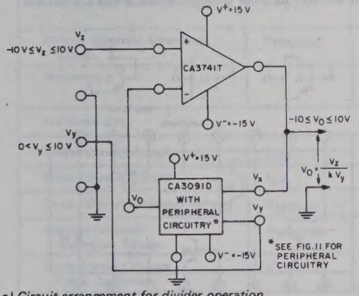
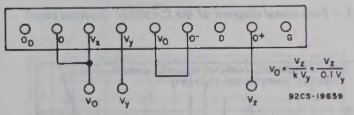


Fig.19—(b) Circuit to provide offset ac signal for use in divider alignment procedure.

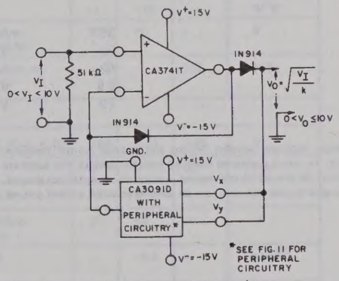


a) Circuit arrangement for divider operation.

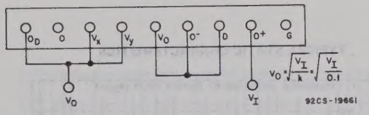


b) Terminal connections for divider operation.

Fig.20—Multifunction circuit-board arrangement with terminal connections for divider operation.



a) Circuit arrangement for square-rooter operation.



b) Terminal connections for square-rooter operation.

Fig.21—Multifunction circuit-board arrangement with terminal connections for square-rooter operation.

CA3093E

General-Purpose High-Current N-P-N Transistor-Zener Diode-Diode Array

RCA CA3093E* is a versatile array of three high-current (to 100mA) NPN transistors, two 10%-tolerance Zener diodes and one conventional diode, all on a common monolithic substrate. Two of the transistors (Q_1 and Q_2) are matched at 1 mA for applications in which offset parameters are of special importance. The combination of positive Zener voltage temperature coefficients and negative forward base-emitter voltage temperature coefficients provides a unique temperature compensation capability.

Independent connections for each transistor and diode plus a separate terminal for the substrate permit maximum flexibility in circuit design.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Power Dissipation:

Any one transistor	500	mW
Any one Zener Diode	250	mW
Total package	750	mW
Above 25°C ... Derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C

The following maximum ratings apply for each transistor

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})*	20	V
Emitter-to-Base Voltage (V_{EBO})	5.5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	35	mA

The following maximum ratings apply for each Zener Diode or Diode

Zener Diode dc Current (I_Z)	35	mA
Zener Diode-to-Substrate Voltage (V_{ZIO})*	20	V
Diode (D1) Forward Current (I_{DF})	50	mA
Diode (D1) Reverse Voltage (V_{DR})	5.5	V
Diode (D1)-to-Substrate Voltage (V_{DIO})*	20	V

*The collector of each transistor, the cathode of each Zener diode, and the anode of the diode are isolated from the substrate by an internal diode. The substrate must be connected to a voltage which is more negative than any of these isolated terminals in order to maintain isolation between devices and provide normal transistor action. To avoid undesired coupling between devices, the substrate terminal (5) should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Features:

- 6 independent devices plus separate substrate connection
- Compensating temperature coefficients – V_{BE} and V_{D1} VS. V_Z

Transistors

- High I_C (100mA max)
- Matched pair (Q1 & Q_2)
  V_{IO} = ± 5mV max, I_{IO} = 2.5 μA max } at I_C = 1mA
  $\Delta V_{IO}/\Delta T$ = 5 μV/°C typ
- h_{FE} = 40 min @ I_C = 10mA or 50mA
- Low V_{CEsat} . . . 0.7V max @ 50mA

Zener Diodes

- Two 1/4W Zeners
- V_Z = 7V ± 10%
- z_Z = 15Ω typ

Diode

- Close forward voltage match to V_{BE}'s of Q_1 and Q_2
- V_{PIV} = 5.5V min.

Applications

- Signal processing and switching systems operating from DC to VHF
- Lamp and relay driver
- Differential amplifier
- Temperature-compensated amplifier
- Thyristor firing
- Temperature-compensated shunt regulator
- Temperature-compensated series regulator
- Level shifting
- Voltage-level clamping
- Current regulator
- Voltage clamping
- Simple off-line regulated supply
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for applications in addition to those given on pages 5 & 6 of this bulletin.

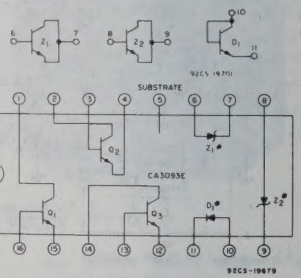


Fig. 1 – Functional diagram of the CA3093E (bottom view)

TYPICAL STATIC CHARACTERISTICS

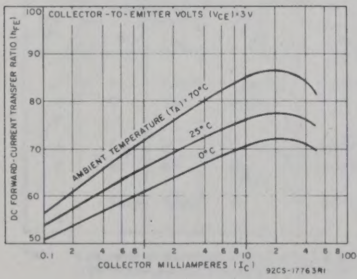


Fig. 2 – h_{FE} vs I_C

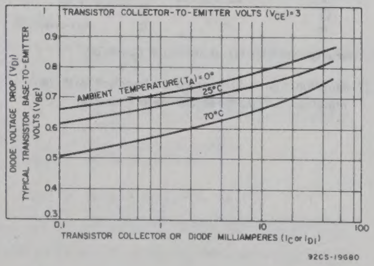


Fig. 3 – V_{BE} vs I_C and V_{D1} vs I_{D1}

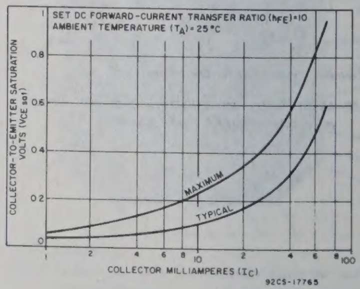


Fig. 4 – V_{CEsat} vs I_C at 25°C

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*Formerly developmental type TA6119

#Z_1, Z_2 and D1 are transistors internally connected as shown below.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100µA, I_E = 0		20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100µA, I_B = 0, I_E = 0		20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500µA, I_C = 0		5.5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0		–	–	10	µA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0		–	–	1	µA
DC Forward Current Transfer Ratio	h_{FE}	V_{CE} = 3V	I_C = 10mA	40	76	–	
			I_C = 50mA	40	75	–	
Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA		0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA		–	0.40	0.70	V
Forward Base-to-Emitter Temp. Coefficient	$\Delta V_{BE/\Delta T}$	I_E = 10mA		–	-1.9	–	mV/°C
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA		–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$			–	0.7	2.5	µA
Temp. Coefficient of Offset Voltage	$\lvert \Delta V_{IO}/\Delta T\rvert$	–		–	5	–	µV/°C
For Each Zener Diode							
Zener Voltage	V_Z	I_Z = 10mA		6.3	7	7.7	V
Zener Impedance	z_Z	I_Z = 10mA, f = 1 kHz		–	15	25	Ω
Zener Reverse Current	I_{ZR}	V_Z = +5V		–	–	1	µA
Zener Voltage Temp. Coefficient	$\Delta V_Z/\Delta T$	I_Z = 10mA		– i.e.	+3.6 +.05	–	mV/°C %/°C
Zener-to-Substrate Breakdown Voltage	$V_{(BR)ZIO}$	I_Z = 100µA (Terminals 7 & 9)		20	60	–	V
Dissipation		Refer to Example in Application "a"		–	–	250	mW
For Diode (D1)							
Diode Forward Voltage	V_{DF}	I_C = 10mA, V_{CE} = 3V		0.65	0.74	0.85	V
Diode Forward Current	I_{DF}			–	–	50	mA
Diode Reverse-Breakdown Voltage	$V_{(BR)DR}$	I_{DR} = 500µA		5.5	6.9	–	V
Diode-to-Substrate Breakdown Voltage	$V_{(BR)DIO}$	I_{Diode} = 100µA (Terminal 10)		20	60	–	V
Diode Forward-Voltage Temp. Coefficient	$\Delta V_{DF}/\Delta T$	I_{DF} = 5mA		–	-1.9	–	mV/°C

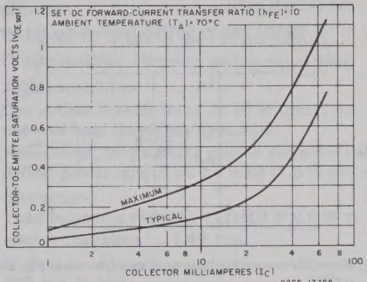


Fig. 5 – V_{CEsat} vs I_C at 70°C

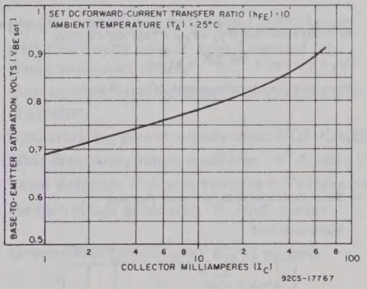


Fig. 6 – V_{BEsat} vs I_C

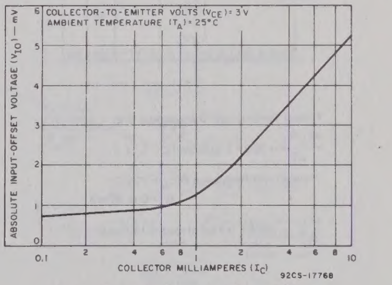


Fig. 7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

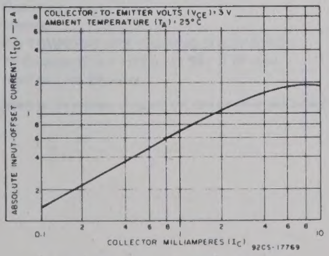


Fig. 8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

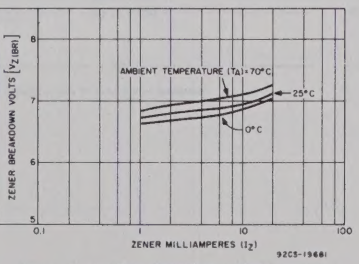


Fig. 9 – Typical Zener breakdown voltage vs current

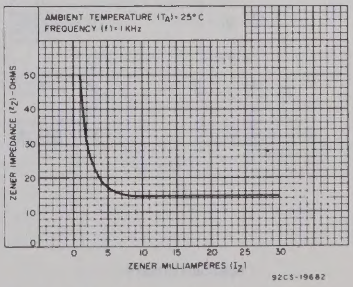
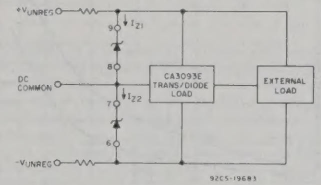


Fig. 10 – Typical Zener impedance vs current

TYPICAL APPLICATIONS

a) ±7V Regulator supplying CA3093E Transistors plus an external load.



Sample Computation for Determining Permissible Zener Dissipation at +25°C.

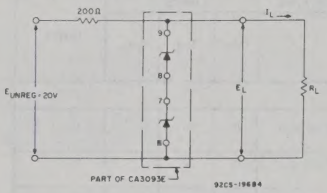
CA3093E Ratings at T_A = +25°C
Total Diss. Max = 750 mW (Derate @ 6.67 mW/°C above 25°C)
Each Zener Diss. Max = 250 mW
Max. Zener Current = 35 mA

Assume CA3093E Transistor/Diode Load Dissipation = 350 mW then max. total Zener Diss. $(P_{Z1} + P_{Z2}) = 750 - 350 = 400$ mW

$$(I_{Z1} + I_{Z2})\ \text{max} = \frac{400\ \text{mW}}{7\text{V}} = 57\ \text{mA}$$

(Note: Max. current rating on each Zener is 35 mA)

b) 14V Regulator for Q1, Q2, Q3



Typical Load Regulation for I_L = 0 to 25 mA

$\Delta E_L/E_L \times 100 \approx -6\%$ (no load to full load)

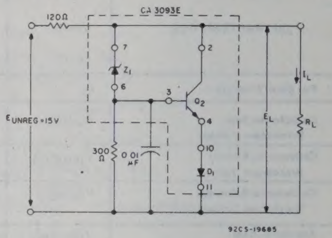
Typical Line Regulation

$$\frac{(\Delta E_L/E_L) \times 100}{\Delta E\ \text{unreg.}} \approx \pm 0.9\%/\text{V}$$

Typical Temperature Characteristic

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = +0.06\%/°\text{C}$$

c) 8.6V Temp.-Compensated Shunt Regulator



Typical Temperature Characteristic @ R_L = 330Ω

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm 0.007\%/°\text{C}$$

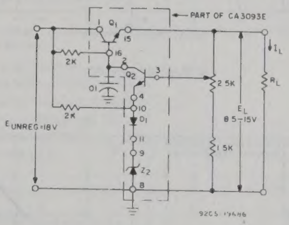
Typical Load Regulation I_L = 0 to 40 mA

$(\Delta E_L/E_L) \times 100 = -3\%$ (no load to full load)

Typical Line Regulation at R_L = 330Ω

$$\frac{\Delta E_L/E_L}{\Delta E\ \text{unreg.}} \times 100 = \pm 0.55\%/\text{V}$$

d) Temp.-Compensated Series Voltage Regulator



Typical Temperature Characteristic @ E_L = 12V

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm\ 0.009\%/°\text{C}$$

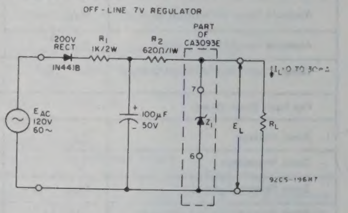
Typical Load Regulation @ E_L = 12V
I_L = 0 to 40 mA

$$\frac{\Delta E_L}{E_L} \times 100 = \pm 0.4\%\ \text{(no load to full load)}$$

Typical Line Regulation @ E_L = 12V

$$\frac{(\Delta E_L/E_L) \times 100}{\Delta E\ \text{unreg.}} = \pm 0.45\%/\text{V}$$

e) Off-Line 7V Regulator



Typical E_L Ripple Voltage = 70 $mV_{p\text{-}p}$

Typical Load Regulation $= \frac{\Delta E_L}{E_L} \times 100 = -8.5\%$ (no load to full load)
I_L = 0 to 30 mA

Typical Line Regulation $= \frac{(\Delta E_L/E_L) \times 100}{\Delta E_{AC}} = \pm .075\%/\text{V}$

Programmable Power Switch/Amplifier

For Control & General-Purpose Applications

CA3094T,S,E: For Operation Up to 24 Volts
CA3094AT,S,E: For Operation Up to 36 Volts
CA3094BT,S: For Operation Up to 44 Volts

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100 mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transistors. The CA3094 has the generic characteristics of the RCA-CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100 mA.

The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100 μA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).

The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs.28,29 and 30 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), and in chip form ("H" suffix).

Features:

- Designed for *single* or dual power supply
- Programmable: strobing, gating, squelching, AGC capabilities
- Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)
- High-power, single-ended class A amplifier will deliver power output of 0.6 watt (1.6 W device dissipation)
- Total harmonic distortion (THD) @ 0.6 W in class A operation — 1.4% typ.
- High current-handling capability — 100 mA (avg.), 300 mA (peak)
- Sensitivity controlled by varying bias current
- Output: "sink" or "drive" capability

Applications:

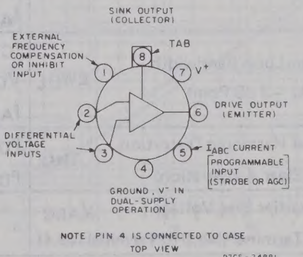
- Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor
- Over-current, over-voltage, over-temperature protectors
- Dual-tracking power supply with RCA-CA3085
- Wide-frequency-range oscillator
- Analog timer
- Level detector
- Alarm systems
- Voltage follower
- Ramp-voltage generator
- High-power comparator
- Ground-fault interrupter (GFI) circuits

MAXIMUM RATINGS, *Absolute-Maximum Values:*

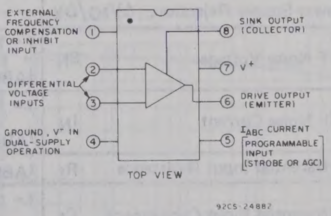
	CA3094	CA3094A	CA3094B	
DC SUPPLY VOLTAGE:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC DIFFERENTIAL INPUT VOLTAGE (Terminals 2 and 3)	± 5*			V
DC COMMON-MODE INPUT VOLTAGE	Term. 4 ≤ Term. 2 & 3 ≤ Term. 7			
PEAK INPUT SIGNAL CURRENT (Terminals 2 and 3)	± 1			mA
PEAK AMPLIFIER BIAS CURRENT (Terminal 5)	2			mA
OUTPUT CURRENT:				
Peak	300			mA
Average	100			mA
DEVICE DISSIPATION:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
THERMAL RESISTANCE (Junction to Air)	140			°C/W
AMBIENT TEMPERATURE RANGE:				
Operating	−55 to +125			°C
Storage	−65 to +150			°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

FUNCTIONAL DIAGRAMS


SINK OUTPUT (COLLECTOR)
TAB
EXTERNAL FREQUENCY COMPENSATION OR INHIBIT INPUT
1
8
7
V+
2
6
DRIVE OUTPUT (EMITTER)
DIFFERENTIAL VOLTAGE INPUTS
3
5
I_{ABC} CURRENT
PROGRAMMABLE INPUT (STROBE OR AGC)
4
GROUND, V⁻ IN DUAL-SUPPLY OPERATION
NOTE PIN 4 IS CONNECTED TO CASE
TOP VIEW
92CS-24881

TO-5 Style Package


EXTERNAL FREQUENCY COMPENSATION OR INHIBIT INPUT
1
2
DIFFERENTIAL VOLTAGE INPUTS
3
GROUND, V⁻ IN DUAL-SUPPLY OPERATION
4
8
SINK OUTPUT (COLLECTOR)
7
V+
6
DRIVE OUTPUT (EMITTER)
5
I_{ABC} CURRENT
PROGRAMMABLE INPUT (STROBE OR AGC)
TOP VIEW
92CS-24882

Plastic Package

CA3094, CA3094A, CA3094B Types

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$ For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Single Supply $V^+ = 30$ V Dual Supply $V^+ = 15$ V, $V^- = 15$ V $I_{ABC} = 100\ \mu A$ Unless Otherwise Specified	LIMITS Min.	Typ.	Max.	UNITS
INPUT PARAMETERS					
Input Offset Voltage V_{IO}	$T_A = 25^oC$	–	0.4	5	mV
	$T_A = 0$ to 70^oC	–	–	7	mV
Input-Offset-Voltage Change $\lvert\Delta V_{IO}\rvert$	Change in V_{IO} Between $I_{ABC} = 100\ \mu A$ and $I_{ABC} = 5\ \mu A$	–	1	8	mV
Input Offset Current I_{IO}	$T_A = 25^oC$	–	0.02	0.2	μA
	$T_A = 0$ to 70^oC	–	–	0.3	μA
Input Bias Current I_I	$T_A = 25^oC$	–	0.2	0.50	μA
	$T_A = 0$ to 70^oC	–	–	0.70	μA
Device Dissipation P_D	$I_{out} = 0$	8	10	12	mW
Common-Mode Rejection Ratio CMRR		70	110	–	dB
Common-Mode Input–Voltage Range V_{ICR}	$V^+ = 30$ V High	27	28.8	–	V
	$V^+ = 30$ V Low	1.0	0.5	–	V
	$V^+ = 15$ V	+12	+13.8	–	V
	$V^- = 15$ V	−14	−14.5	–	V
Unity Gain-Bandwidth	$I_C = 7.5$ mA $V_{CE} = 15$ V $I_{ABC} = 500\ \mu A$	–	30	–	MHz
Open-Loop Bandwidth At −3 dB Point BW_{OL}	$I_C = 7.5$ mA $V_{CE} = 15$ V $I_{ABC} = 500\ \mu A$	–	4	–	kHz
Total Harmonic Distortion (Class A Operation) THD	$P_D = 220$ mW	–	0.4	–	%
	$P_D = 600$ mW	–	1.4	–	%
Amplifier Bias Voltage V_{ABC} (Terminal (No.5 to Terminal No.4)		–	0.68	–	V
Input Offset Voltage Temperature Coefficient $\Delta V_{IO}/\Delta T$		–	4	–	μV/°C
Power-Supply Rejection $\Delta V_{IO}/\Delta V$		–	15	150	μV/V
1/F Noise Voltage E_N	f = 10 Hz $I_{ABC} = 50\ \mu A$	–	18	–	$\eta V/\sqrt{Hz}$
1/F Noise Current I_N	f = 10 Hz $I_{ABC} = 50\ \mu A$	–	1.8	–	$pA/\sqrt{Hz}$
Differential Input Resistance R_I	$I_{ABC} = 20\ \mu A$	0.50	1	–	MΩ
Differential Input Capacitance C_I	f = 1 MHz $V^+ = 30$ V	–	2.6	–	pF

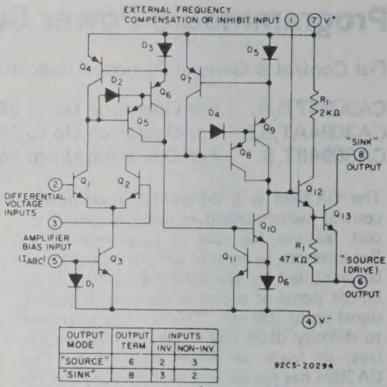


Fig. 1 – Schematic diagram of CA3094.

TYPICAL CHARACTERISTICS CURVES

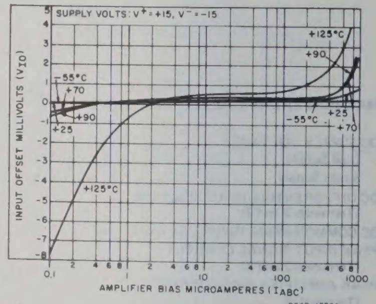


Fig.2 – Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

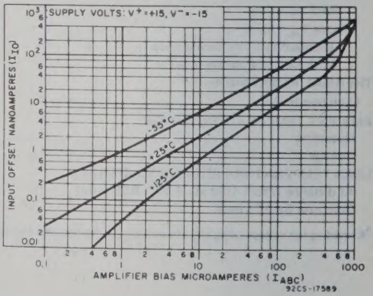


Fig.3 – Input offset current vs. amplifier bias current (I_{ABC}, terminal No.5).

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$ For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	Single Supply $V^+ = 30$ V Dual Supply $V^+ = 15$ V, $V^- = 15$ V $I_{ABC} = 100\ \mu A$ Unless Otherwise Specified	Min.	Typ.	Max.	
OUTPUT PARAMETERS (Differential Input Voltage = 1 V)					
Peak Output Voltage: (Terminal No. 6)	$V^+ = 30$ V				
With Q13 "ON" V^+OM	$R_L = 2\ k\Omega$ to ground	26	27	–	V
With Q13 "OFF" V^-OM		–	0.01	0.05	V
Peak Output Voltage: (Terminal No. 6)	$V^+ = +15$ V, $V^- = -15$ V			0.5	
Positive V^+OM	$R_L = 2\ k\Omega$ to -15 V	+11	+12	–	V
Negative V^-OM		–	−14.99	−14.95	V
Peak Output Voltage: (Terminal No. 8)	$V^+ = 30$ V				
With Q13 "ON" V^+OM	$R_L = 2\ k\Omega$ to 30 V	29.95	29.99	–	V
With Q13 "OFF" V^-OM		–	0.040	–	V
Peak Output Voltage: (Terminal No. 8)	$V^+ = 15$ V, $V^- = -15$ V				
Positive V^+OM	$R_L = 2\ k\Omega$ to + 15 V	+14.95	+14.99	–	V
Negative V^-OM		–	14.96	–	V
Collector-to-Emitter Saturation Voltage (Terminal No. 8) $V_{CE(sat)}$	$V^+ = 30$ V $I_C = 50$ mA Terminal No.6 grounded	–	0.17	0.80	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)	$V^+ = 30$ V	–	2	10	µA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13}) h_{fe}	$V^+ = 30$ V $V_{CE} = 5$ V $I_C = 50$ mA	16,000	100,000	–	
Output Capacitance:	f = 1 MHz				
Terminal No. 6 C_O	All Remaining Terminals Tied to Terminal No. 4	–	5.5	–	pF
Terminal No. 8		–	17	–	pF
TRANSFER PARAMETERS					
Voltage Gain A	$V^+ = 30$ V $I_{ABC} = 100\ \mu A$ $\Delta V_{out} = 20$ V $R_L = 2\ k\Omega$	20,000	100,000	–	V/V
		86	100	–	dB
Forward Transconductance To Terminal No. 1 g_m		1650	2200	2750	µmhos
Slew Rate: Open Loop:					
Positive Slope	$I_{ABC} = 500\ \mu A$ $R_L = 2\ k\Omega$	–	500	–	V/µs
Negative Slope		–	50	–	V/µs
Unity Gain (Non-Inverting, Compensated)	$I_{ABC} = 500\ \mu A$ $R_L = 2\ k\Omega$	–	0.7	–	V/µs

TYPICAL CHARACTERISTICS CURVES (Cont'd)

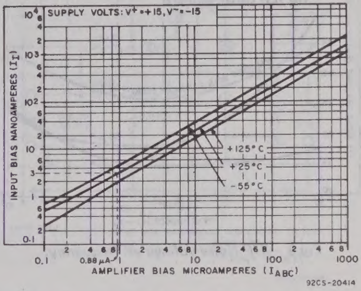


Fig.4 – Input bias current vs. amplifier bias current (I_{ABC}, terminal No.5).

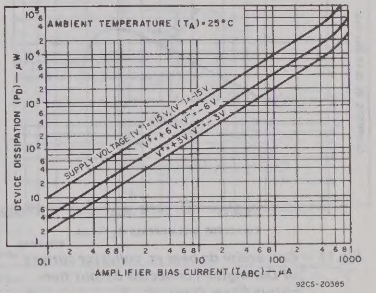


Fig.5 – Device dissipation vs. amplifier bias current (I_{ABC}, terminal No.5).

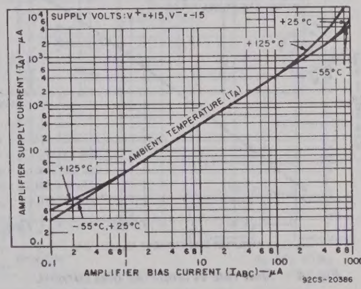


Fig.6 – Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No.5).

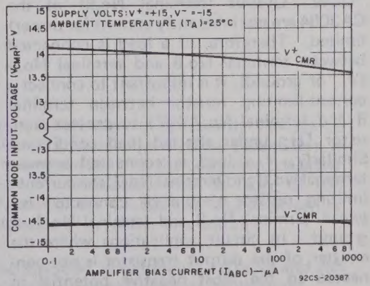


Fig.7 – Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

CA3094, CA3094A, CA3094B Types

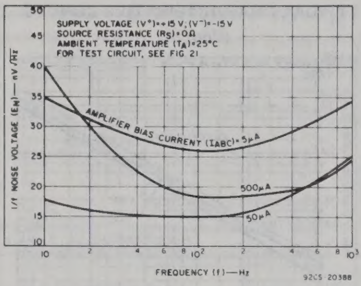


Fig.8 – I/F Noise voltage vs. frequency.

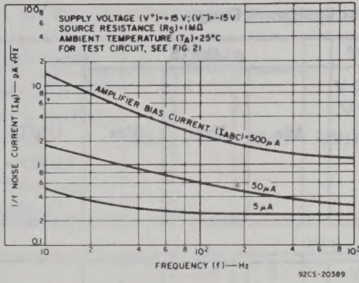


Fig.9 – I/F Noise current vs. frequency.

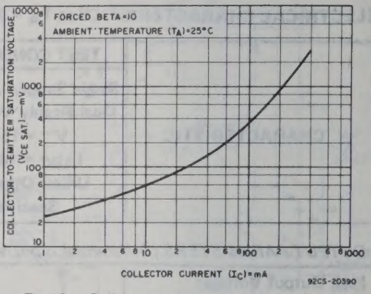


Fig.10 – Collector-emitter saturation voltage vs. collector current of output transistor Q_{13}.

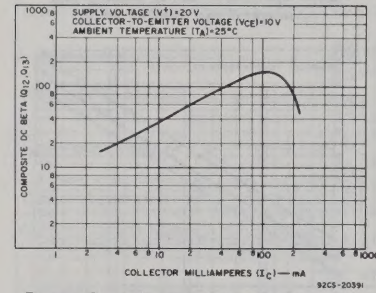


Fig.11 – Composite dc beta vs. collector current of Darlington-connected output transistors (Q_{12}, Q_{13}).

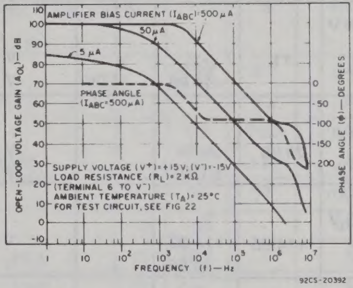


Fig.12 – Open-loop voltage gain vs. frequency.

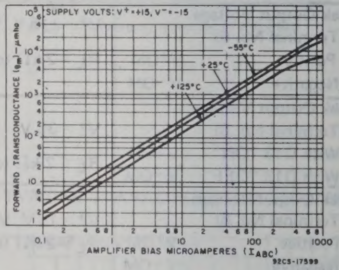


Fig.13 – Forward transconductance vs amplifier bias current.

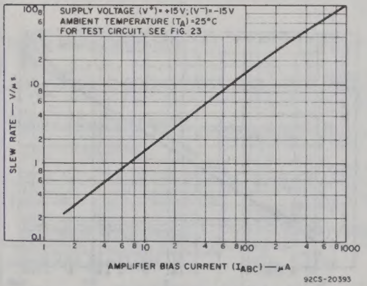


Fig.14 – Slew rate vs amplifier bias current.

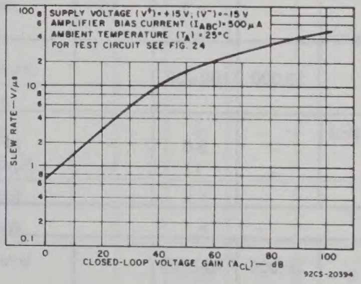


Fig.15 – Slew rate vs closed-loop voltage gain.

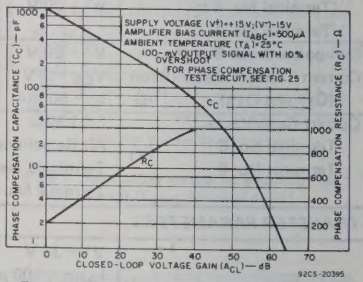


Fig.16 – Phase compensation capacitance and resistance vs closed-loop voltage gain.

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No.8) and the "Drive" Output (terminal No.6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between terminal No.6 and terminal No.4 (V^- or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No.7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No.8 and terminal No.7, the current-limiting resistor should be connected between terminal No.6 and terminal No.4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No.7 and the V^+ supply.

TEST CIRCUITS

I/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig.21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No.2 to ground. Source resistors (Rs) are set to 0.Ω or 1 MΩ for E noise and I noise measurements, respectively. These measurements are made at frequencies of 10, Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50 µA I_{ABC} are $E_n = 18\ nV/\sqrt{HZ}$ and $I_N = 1.8\ pA/\sqrt{HZ}$.

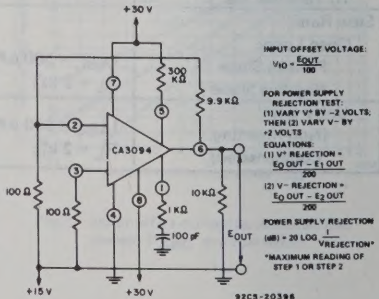
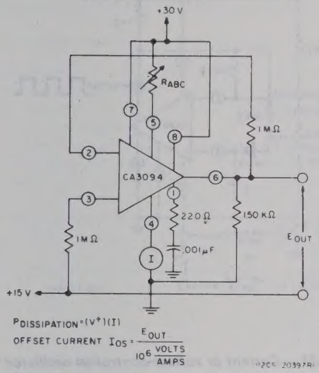

+30 V
300 KΩ
9.9 KΩ
7
5
2
3
6
1
8
4
CA3094
100 Ω
100 Ω
1 KΩ
100 pF
10 KΩ
EOUT
+15 V
+30 V
INPUT OFFSET VOLTAGE:
VIO = EOUT/100
FOR POWER SUPPLY REJECTION TEST:
(1) VARY V+ BY −2 VOLTS; THEN (2) VARY V− BY +2 VOLTS
EQUATIONS:
(1) V+ REJECTION = (E0 OUT − E1 OUT)/200
(2) V− REJECTION = (E0 OUT − E2 OUT)/200
POWER SUPPLY REJECTION (dB) = 20 LOG 1/VREJECTION*
*MAXIMUM READING OF STEP 1 OR STEP 2
92CS-20396

Fig.17 – Input offset voltage and power-supply rejection test circuit.

TEST CIRCUITS (Cont'd)



$P_{DISSIPATION} = (V^+)(I)$

OFFSET CURRENT $I_{OS} = \frac{E_{OUT}}{10^6 \frac{VOLTS}{AMPS}}$

Fig.18 – Input offset current test circuit.

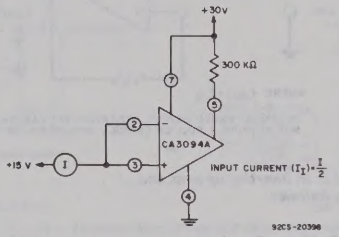
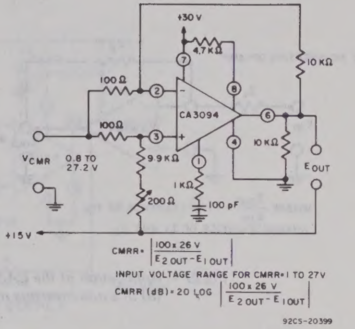


Fig. 19 – Input bias current test circuit.

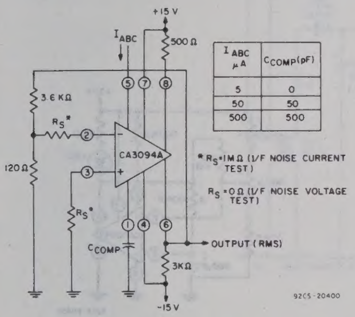


$CMRR = \left| \frac{100 \times 26\ V}{E_{2\ OUT} - E_{1\ OUT}} \right|$

INPUT VOLTAGE RANGE FOR CMRR = 1 TO 27V

$CMRR\ (dB) = 20\ LOG \left| \frac{100 \times 26\ V}{E_{2\ OUT} - E_{1\ OUT}} \right|$

Fig.20 – Common-mode range and rejection ratio test circuit.

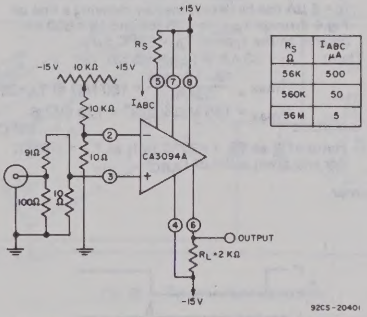


I_{ABC} μA	C_{COMP}(pF)
5	0
50	50
500	500

*R_S = 1MΩ (1/F NOISE CURRENT TEST)

R_S = 0 Ω (1/F NOISE VOLTAGE TEST)

Fig.21 – 1/F noise test circuit.



R_S Ω	I_{ABC} μA
56K	500
560K	50
56M	5

Fig.22 – Open-loop gain vs frequency test circuit.

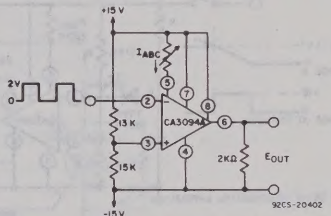


Fig.23 – Open-loop slew rate vs I_{ABC} test circuit.

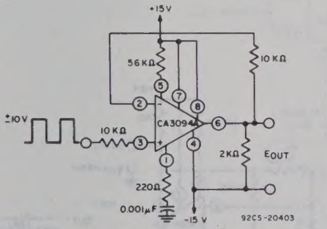
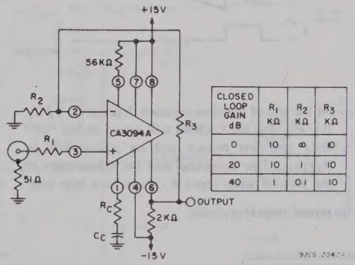
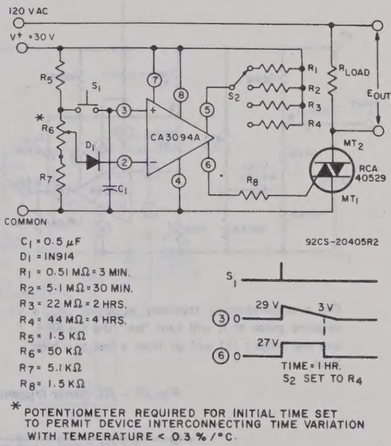


Fig.24 – Slew rate vs. non-inverting unity gain test circuit.



CLOSED LOOP GAIN dB	R_1 KΩ	R_2 KΩ	R_3 KΩ
0	10	∞	10
20	10	1	10
40	1	0.1	10

Fig.25 – Phase compensation test circuit.



C_1 = 0.5 μF
D_1 = 1N914
R_1 = 0.51 MΩ = 3 MIN.
R_2 = 5.1 MΩ = 30 MIN.
R_3 = 22 MΩ = 2 HRS.
R_4 = 44 MΩ = 4 HRS.
R_5 = 1.5 KΩ
R_6 = 50 KΩ
R_7 = 5.1 KΩ
R_8 = 1.5 KΩ

* POTENTIOMETER REQUIRED FOR INITIAL TIME SET TO PERMIT DEVICE INTERCONNECTING TIME VARIATION WITH TEMPERATURE < 0.3 %/°C.

Fig.26 – Presettable analog timer.

TYPICAL APPLICATIONS

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/Switch Amplifier IC".

Design Considerations

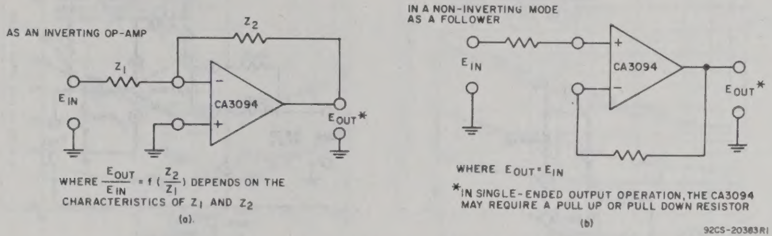
The selection of the optimum amplifier bias current (I_{ABC}) depends on –

1. The Desired Sensitivity – the higher the I_{ABC}, the higher the sensitivity – i.e., a greater-drive current capability at the output for a specific voltage change at the input.
2. Required Input Resistance – the lower the I_{ABC}, the higher the input resistance.

If the desired sensitivity and requred input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100 μA, since the CA3094 is characterized at this value of amplifier bias current.

The CA3094 is extremely versatile and can be used in a wide variety of applications.

TYPICAL APPLICATIONS (Cont'd)

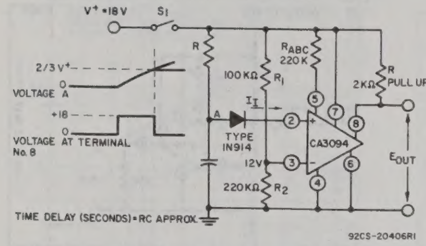


WHERE $\frac{E_{OUT}}{E_{IN}} = f\left(\frac{Z_2}{Z_1}\right)$ DEPENDS ON THE CHARACTERISTICS OF Z_1 AND Z_2

WHERE $E_{OUT} = E_{IN}$

*IN SINGLE-ENDED OUTPUT OPERATION, THE CA3094 MAY REQUIRE A PULL UP OR PULL DOWN RESISTOR

Fig.27 – Application of the CA3094: (a) as an inverting op-amp, and (b) in a non-inverting mode, as a follower.



Problem: To calculate the maximum value of R required to switch a 100-mA output current comparator

Given: $I_{ABC} = 5\ \mu A$, $R_{ABC} = 3.6\ M\Omega \approx \frac{18\ V}{5\ \mu A}$

$I_I = 500\ nA$ @ $I_{ABC} = 100\ \mu A$ (from Fig.4)

$I_I = 5\ \mu A$ can be determined by drawing a line on Fig.4 through $I_{ABC} = 100\ \mu A$ and $I_B = 500\ nA$ parallel to the typical $T_A = 25^oC$ curve.

Then: $I_I = 33\ nA$ @ $I_{ABC} = 5\ \mu A$

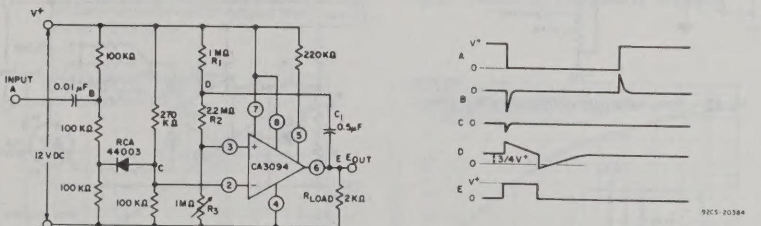
$$R_{max} = \frac{18-12\ \text{volts}}{33nA} = 180\ M\Omega \text{ @ } T_A = 25^oC$$

$$R_{max} = 180\ M\Omega \times 2/3^* = 120\ M\Omega \text{ @ } T_A = -55^oC$$

---

* Ratio of I_I at $T_A = +25^oC$ to I_I at $T_A = -55^oC$ for any given value of I_{ABC}.

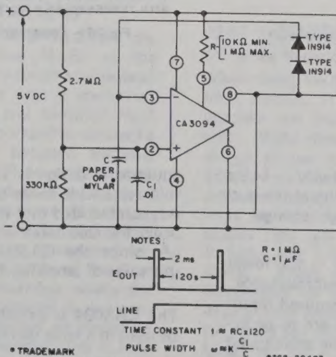
Fig.28 – RC timer.



On a negative-going transient at input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.

At the end of the time constant determined by C_1, R_1, R_2, R_3, the CA3094 will return to the "off" state and the output will be pulled low by R_{LOAD}. This condition will be independent of the interval when input A returns to a high level.

Fig.29 – RC timer triggered by external negative pulse.



* TRADEMARK
E.I. DUPONT DE NEMOURS

Fig.30 – Free-running pulse generator.

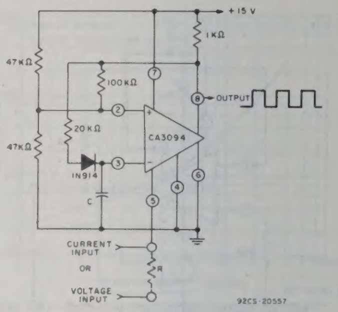


Fig.31 – Current or voltage-controlled oscillator.

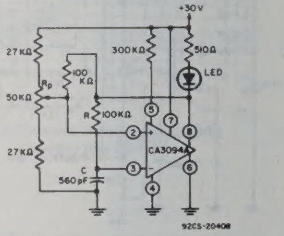
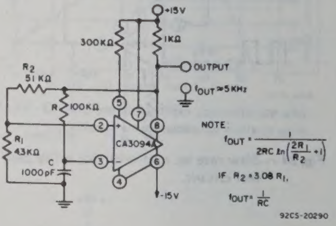


Fig.32 – Single-supply astable multivibrator.



NOTE:

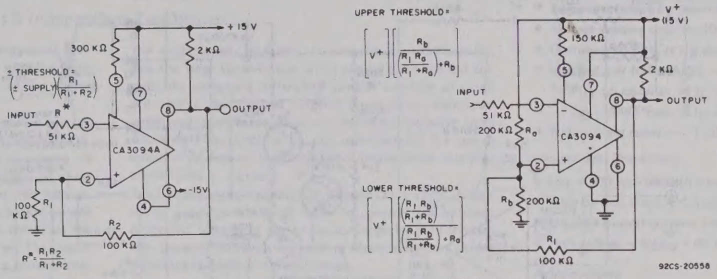
$$f_{OUT} = \frac{1}{2RC\,\ln\left(\frac{2R_1}{R_2}+1\right)}$$

IF $R_2 = 3.08\ R_1$,

$$f_{OUT} = \frac{1}{RC}$$

Fig.33 – Dual-supply astable multivibrator.

TYPICAL APPLICATIONS (Cont'd)


+15 V
300 KΩ
2 KΩ
± THRESHOLD = (± SUPPLY)(R1/(R1 + R2))
INPUT
R*
51 KΩ
CA3094A
OUTPUT
-15V
100 KΩ
R1
R2
100 KΩ
R* = R1R2/(R1+R2)
UPPER THRESHOLD = [V+][(Rb)/((R1 Ra)/(R1 + Ra) + Rb)]
LOWER THRESHOLD = [V+][((R1 Rb)/(R1+Rb))/((R1 Rb)/(R1+Rb) + Ra)]
V+ (15 V)
150 KΩ
2 KΩ
INPUT
51 KΩ
200 KΩ
Ra
CA3094
OUTPUT
Rb
200 KΩ
R1
100 KΩ
92CS-20558

(a) DUAL SUPPLY (b) SINGLE SUPPLY

Fig.34 – Comparators (threshold detectors) –dual- and single-supply types.

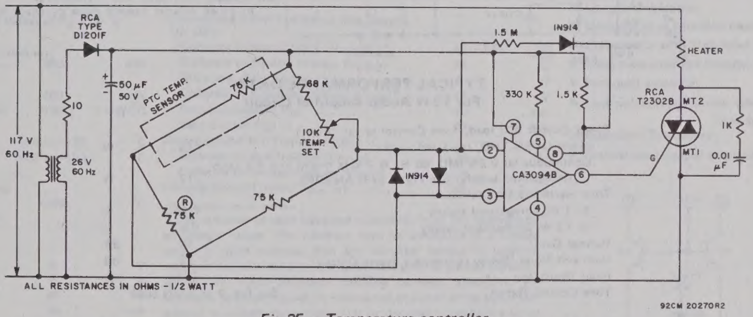
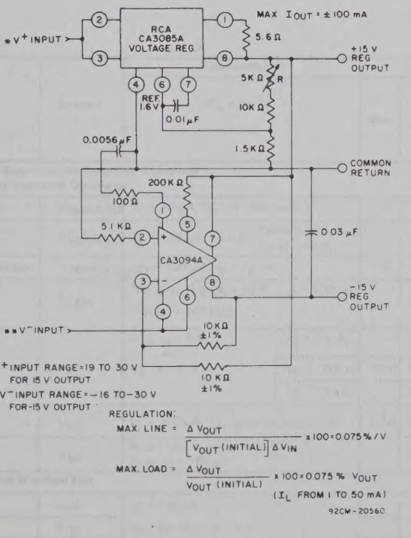


Fig.35 – Temperature controller.



*V+ INPUT RANGE = 19 TO 30 V FOR 15 V OUTPUT

**V− INPUT RANGE = −16 TO −30 V FOR −15 V OUTPUT

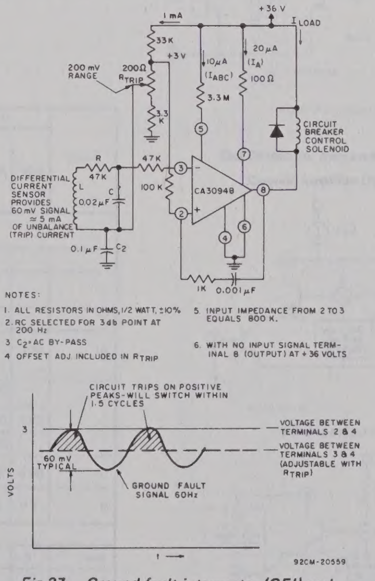
REGULATION:

$$\text{MAX. LINE} = \frac{\Delta V_{OUT}}{\left[V_{OUT}\,(\text{INITIAL})\right]\Delta V_{IN}} \times 100 = 0.075\,\%/V$$

$$\text{MAX. LOAD} = \frac{\Delta V_{OUT}}{V_{OUT}\,(\text{INITIAL})} \times 100 = 0.075\,\%\ V_{OUT}$$

(I_L FROM 1 TO 50 mA)

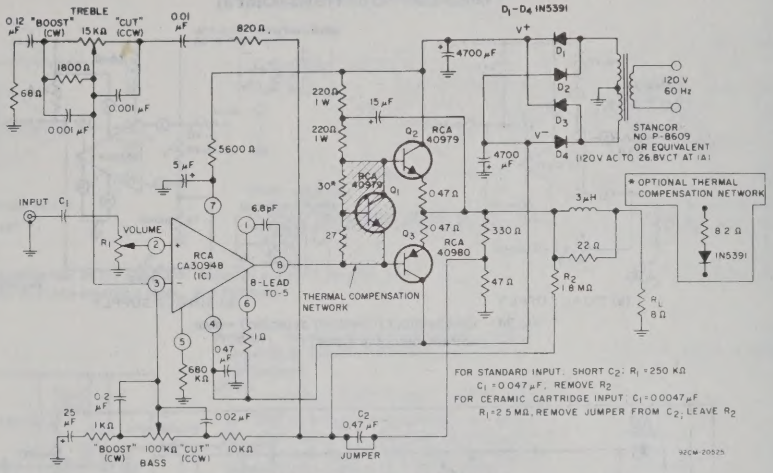
Fig.36 – Dual-voltage tracking regulator.


+36 V
I LOAD
1 mA
33K
+3V
200 mV RANGE
200Ω
RTRIP
3.3 K
10 μA (IABC)
20 μA (IA)
100 Ω
3.3 M
CIRCUIT BREAKER CONTROL SOLENOID
DIFFERENTIAL CURRENT SENSOR PROVIDES 60 mV SIGNAL ≈ 5 mA OF UNBALANCE (TRIP) CURRENT
R
47K
L
C
0.02 μF
47K
100 K
CA3094B
0.1 μF
C2
1K
0.001 μF
CIRCUIT TRIPS ON POSITIVE PEAKS-WILL SWITCH WITHIN 1.5 CYCLES
3
60 mV TYPICAL
VOLTS
GROUND FAULT SIGNAL 60Hz
VOLTAGE BETWEEN TERMINALS 2 & 4
VOLTAGE BETWEEN TERMINALS 3 & 4 (ADJUSTABLE WITH RTRIP)
t →
92CM-20559

NOTES:

1. ALL RESISTORS IN OHMS, 1/2 WATT, ±10%
2. RC SELECTED FOR 3db POINT AT 200 Hz
3. C_2 = AC BY-PASS
4. OFFSET ADJ. INCLUDED IN R_{TRIP}
5. INPUT IMPEDANCE FROM 2 TO 3 EQUALS 800 K.
6. WITH NO INPUT SIGNAL TERMINAL 8 (OUTPUT) AT +36 VOLTS

Fig.37 – Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.



FOR STANDARD INPUT: SHORT C_2; R_1 = 250 KΩ
C_1 = 0.047 μF, REMOVE R_2
FOR CERAMIC CARTRIDGE INPUT: C_1 = 0.0047 μF
R_1 = 2.5 MΩ, REMOVE JUMPER FROM C_2; LEAVE R_2

TYPICAL PERFORMANCE DATA
For 12-W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")		
Music (at 5% THD, regulated supply)	15	W
Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8 In ICAN-6048	12	W
Total Harmonic Distoration		
At 1 W, unregulated supply	0.05	%
At 12 W, unregulated supply	0.57	%
Voltage Gain	40	dB
Hum and Noise (Below continuous Power Output)	83	dB
Input Resistance	250	kΩ
Tone Control Range	See Fig. 9 In ICAN-6048	

Fig.38 — 12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.

Super-Beta Transistor Array

Differential Cascode Amplifier Plus 3 Independent Transistors

RCA-CA3095E is a monolithic array of transistors connected as a super-beta differential cascode amplifier with three independent n-p-n transistors. (Refer to Fig. 1 for following description.)

The differential cascode amplifier incorporates two cascode amplifiers consisting of transistors Q1, Q3 and Q2, Q4, respectively, plus a voltage-limiting circuit, consisting of diodes D1, D2 and p-n-p transistor Q5. Two of these transistors, Q1 and Q2, are super-beta types that have an $h_{FE} > 1000$ and are capable of operating over a wide current range of 1 μA to 2 mA. Each of these types comprises the input section of its respective cascode amplifier. The output section of each cascode amplifier employs a conventional n-p-n transistor, Q3, Q4, respectively. The output signal is obtained at the collectors of these transistors. See Operating Considerations for bias considerations of the differential cascode amplifier.

The exceptionally high-beta characteristics of Q1 and Q2, plus the large signal-voltage swing capability of Q3 and Q4, make the composite differential cascode amplifier an excellent choice for a broad range of small-signal, high-input-impedance amplifier applications including low-noise video amplifiers. This amplifier is also recommended for use in long-interval timers, oscillators, and long-duration one-shot applications.

The independent transistors, Q6, Q7 and Q8, are high-voltage silicon n-p-n conventional types for general use in signal processing systems in the frequency range from dc through vhf. Separate terminals for each of these transistors permit maximum flexibility in circuit design.

The CA3095E is supplied in a 16-lead dual-in-line plastic package and operates over the ambient temperature range of −55°C to +125°C

Features

- Two super-beta n-p-n transistors – $h_{FE} > 1000$
- Voltage-limiting circuitry (D1, D2, Q5)
- Operation possible at I_{IB} down to < 1 nA
- Matched pair (Q1 and Q2) –
  $V_{IO} = 5$ mV max. at $I_C = 100$ μA dc
  $I_{IO} = 20$ nA max. at $I_C = 100$ μA dc
- Wide current range – < 1 μA to 2 mA

Independent Transistors:

- $h_{FE} = 300$ typ. for each transistor
- Wide current range – < 1 μA to 10 mA
- Matched general-purpose transistors
- High voltage – $V_{CBO} = 45$ V max.

Applications

Differential Cascode Amplifier:

- Super-beta pre-amplifier for op-amp
- High-impedance dc meter amplifier
- Low-noise video amplifier
- Piezoelectric transducer amplifier
- Long-interval timer
- Long-duration one-shot multivibrator
- Comparator with high-input impedance
- Long-time-constant integrator
- Photocell amplifier
- Low-noise amplifier–for operation from high-source impedances

Independent Transistors:

- General use in signal processing systems in dc through vhf range

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25\ ^\circ C$*

Power Dissipation:		
Any One Transistor	300	mW
Total Package–		
Up to 25 °C	750	mW
Above 25 °C .... derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−55 to +150	°C
Lead Temperature (During Soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C
Voltage and Current Ratings Apply for Each Specified Transistor:		
Super-Beta Transistors (Q1, Q2)–		
Collector-to-Base Voltage (V_{CBO})	6	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional N-P-N Transistors (Q3, Q4, Q6, Q7, Q8)–		
Collector-to-Base Voltage (V_{CBO})	45	V
Collector-to-Emitter Voltage (V_{CEO})	35	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional P-N-P Transistor (Q5)–		
Collector-to-Base Voltage (V_{CBO})	−45	V
Collector-to-Emitter Voltage (V_{CEO})	−35	V
Limiting Circuit Current ($I_{Pin\ 11}$)	20	mA

---

* The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

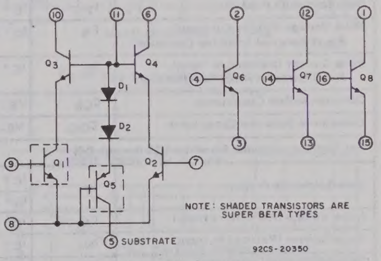


Fig.1–Functional diagram.

STATIC CHARACTERISTICS

Characteristics	Symbol	Test Conditions $T_A = 25\ ^\circ C$		Limits Min.	Limits Typ.	Limits Max.	Units
Characteristics Apply for Each Super-Beta Cascode Amplifier Transistor Pair (Q1, Q3) and (Q2, Q4), Unless Indicated Otherwise							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ μA, $I_E = 0$ See Note 1		6	–	–	V
Emitter-to-Base Breakdown Voltage (Applies only to Q1 & Q2)	$V_{(BR)EBO}$	$I_E = 100$ μA, $I_C = 0$	Term. 9 to 8 or Term. 7 to 8	6	8		V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100$ μA, $I_B = I_E = 0$		45	–	–	V
Collector Cutoff Current	I_{CER}	V_{6-8} or $V_{10-8} = 10$ V, $I_{11} = 100$ μA $R_{BE} = 100$ MΩ		–	–	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{10-8} = 5$ V or $V_{6-8} = 5$ V	$I_C = 1$ mA	–	1500	–	
			$I_C = 100$ μA	1000	2000	5000	
			$I_C = 10$ μA	–	1500	–	
Base-to-Emitter Voltage (Applies only to Q1 & Q2)	V_{BE}	$I_C = 100$ μA, V_{6-8} or $V_{10-8} = 5$ V		0.50	0.59	0.68	V
Saturation Voltage	V_{sat}	I_6 or $I_{10} = 1$ mA, $I_{11} = 100$ μA, I_7 or $I_9 = 100$ μA		–	0.22	0.7	V
For Cascode Amplifiers as a Differential Matched Pair							
Magnitude of Input-Offset Voltage	$\lvert V_{IO}\rvert$	$I_C = 100$ μA $V_{6-8} = V_{10-8} = 5$ V		–	1	5	mV
Magnitude of Input-Offset Current	$\lvert I_{IO}\rvert$			–	4	20	nA
Magnitude of Input-Offset Voltage Drift (Temp. Coeff.)	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			–	3.3	–	μV/°C
Magnitude of Input-Offset Current Drift (Temp. Coeff.)	$\frac{\lvert\Delta I_{IO}\rvert}{\Delta T}$			–	0.05	–	nA/°C

Note 1: Terminal No. 9 to terminals 10 and 11 connected or terminal No. 7 to terminals 6 and 11 connected.

Test Circuits for Measurement of Super-Beta Cascode Amplifier Characteristics

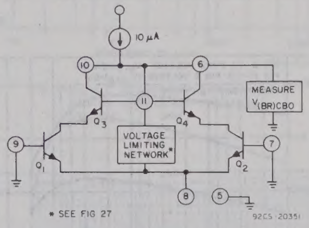


Fig.2–$V_{(BR)CBO}$ test circuit.

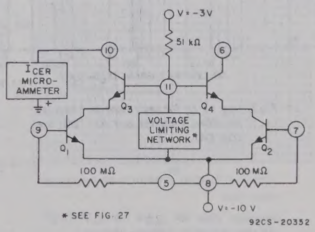


Fig.3–I_{CER} test circuit

STATIC CHARACTERISTICS (Cont'd)

Characteristics	Symbol	Test Conditions T_A = 25 °C		Limits Min.	Limits Typ.	Limits Max.	Units
For Each Conventional n-p-n Transistor (Q3, Q4, Q6, Q7, Q8)							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		45	95	--	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		35	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 100 μA, I_C = 0		6	8	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100 μA, I_B = I_E = 0		45	95	–	V
Collector Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	100	nA
Collector Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	10	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 5 V	I_C = 10 mA	–	210	–	
			I_C = 1 mA	150	300	500	
			I_C = 10 μA	–	180	–	
Base-to-Emitter Voltage	V_{BE}	I_C = 1 mA, V_{CE} = 6 V		0.60	0.69	0.78	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10 mA, I_B = 1 mA		–	0.22	0.7	V

Dynamic Characteristics

Characteristics	Symbol	Test Conditions T_A = 25 °C	Limits Min.	Limits Typ.	Limits Max.	Units
Characteristics Apply for Each Super-Beta Cascode Amplifier Transistor Pair (Q1, Q3), Unless Indicated Otherwise						
Gain-Bandwidth Product	f_T	I_C = 100 μA, V_{6-8} = V_{10-8} = 5 V,	–	78	–	MHz
Noise Voltage (Referred to Input) For Differential Amplifier Operation	E_N	I_C = 50 μA, f = 10 Hz	–	13	–	nV/ $\sqrt{Hz}$
Noise Current (Referred to Input) For Differential Amplifier Operation	I_N	I_C = 5 μA, f = 10 Hz	–	0.12	–	pA/ $\sqrt{Hz}$
Collector-to-Base Capacitance	C_{CB}	V_{6-7} = V_{10-9} = 5 V, I_E = 0	–	0.3		pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{6-5} = V_{10-5} = 5 V, I_B = 0	–	3.0	–	pF
For Each Conventional Transistor (Q3 through Q8)						
Gain-Bandwidth Product	f_T	I_C = 100 μA, V_{CE} = 5 V	–	100	–	MHz
		I_C = 3 mA, V_{CE} = 5 V	–	320	–	
Noise Voltage (Referred to Input)	E_N	I_C = 100 μA, V_{CE} = 5 V, f = 10 Hz	–	5	–	nV/ $\sqrt{Hz}$
Noise Current (Referred to Input)	I_N	I_C = 10 μA, V_{CE} = 5 V, f = 10 Hz	–	0.8	–	pA/ $\sqrt{Hz}$
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5 V, I_E = 0	–	0.4	–	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 5 V, I_B = 0	–	2	–	pF

* Curve plotted for I_{CEO} characteristic.

Test Circuits for Measurement of Super-Beta Cascode Amplifier Characteristics

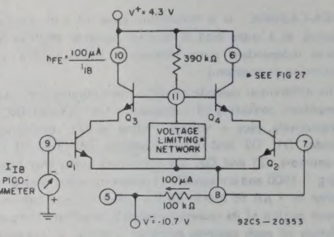


Fig.4—DC Beta (h_{FE}) test circuit.

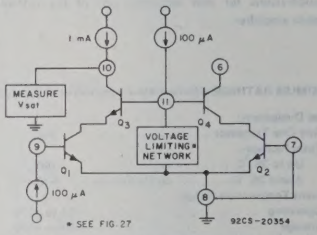


Fig.5—V_{sat} test circuit for super-beta cascode pairs.

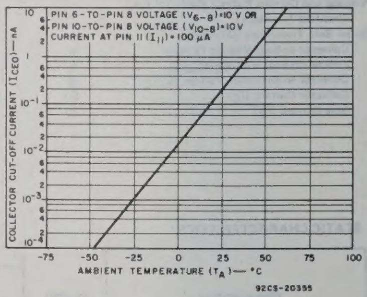


Fig.6—Collector cut-off current vs ambient temperature for super-beta cascode pairs.

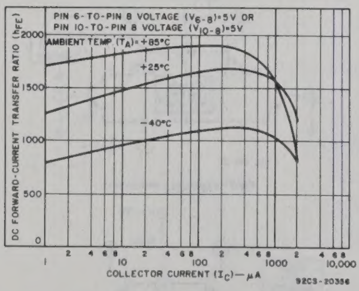


Fig.7—h_{FE} vs. I_C for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

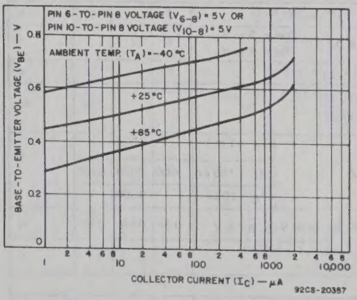


Fig.8—V_{BE} vs. I_C for each super-beta transistor (Q1 and Q2).

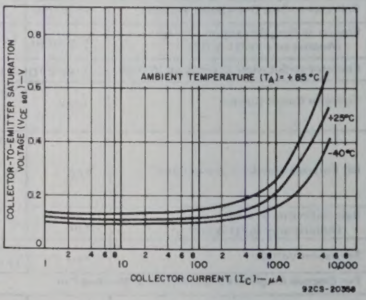


Fig.9—$V_{CE(sat)}$ vs. I_C for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

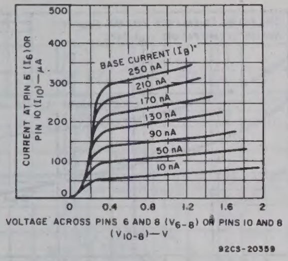


Fig.10—I-V characteristics for the super-beta cascode pairs.

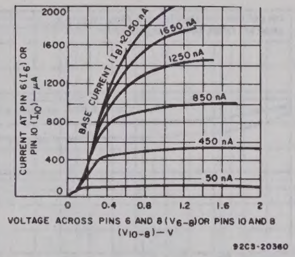


Fig.11—I-V characteristics for the super-beta cascode pairs.

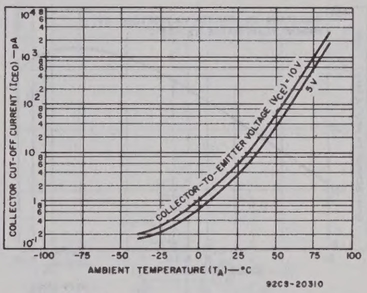


Fig.12—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CE} = 5 V, 10 V).

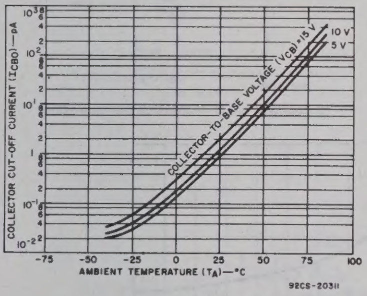


Fig.13—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CB} = 5 V, 10 V, 15 V).

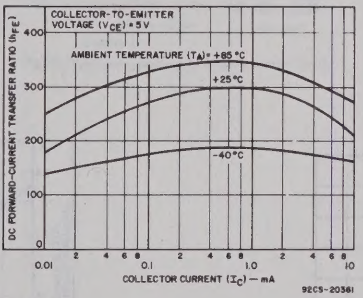


Fig.14—h_{FE} vs. I_C for each conventional transistor (Q6, Q7, Q8).

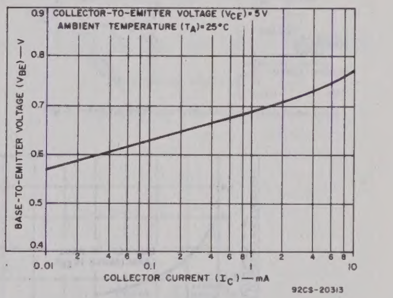


Fig.15—V_{BE} as a function of collector current for the conventional transistors.

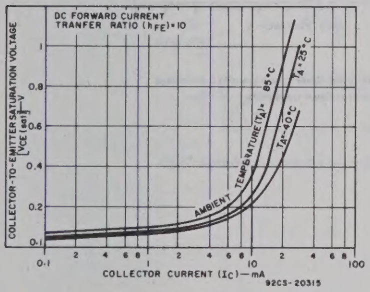


Fig.16—$V_{CE(sat)}$ as a function of collector current for the conventional transistors.

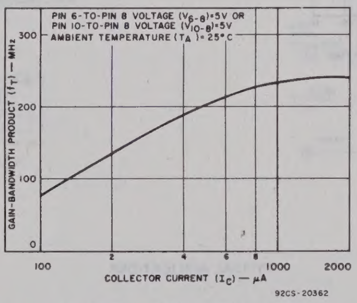


Fig.17—Gain bandwidth product vs collector current for the super-beta cascode pairs.

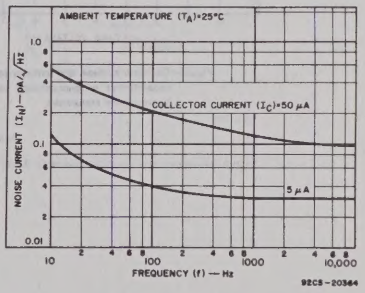


Fig.18—I_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

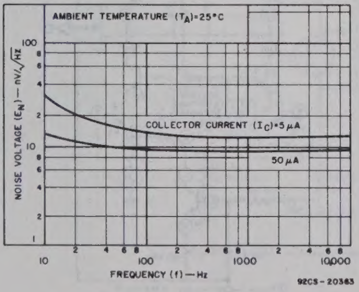


Fig.19—E_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

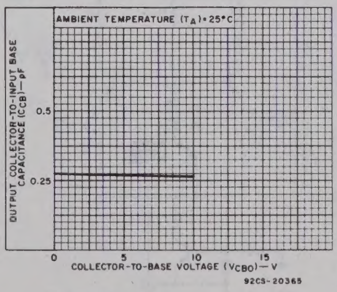


Fig.20—C_{CB} vs. V_{CBO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

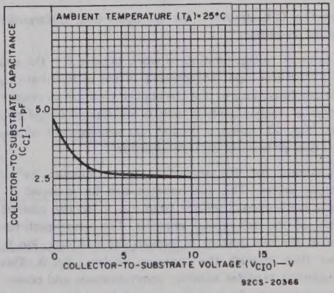


Fig.21—C_{CI} vs. V_{CIO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

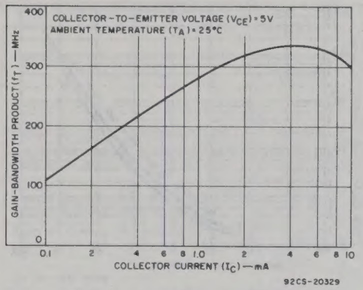


Fig.22—Gain bandwidth product vs collector current for the conventional transistors.

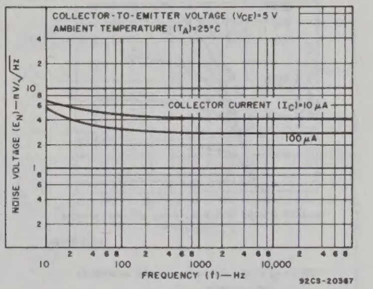


Fig.23—Noise voltage vs frequency for the conventional transistors.

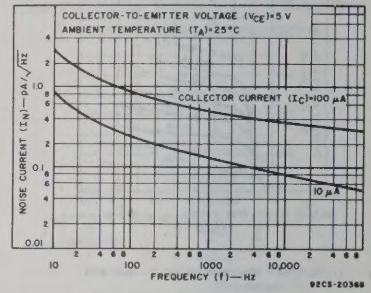


Fig.24—I_N vs. f for each conventional transistor (Q6, Q7, Q8).

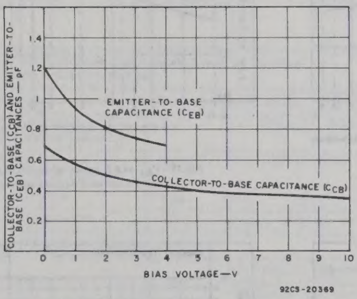


Fig.25—Collector-to-base and emitter-to-base capacitances vs bias voltage for the conventional transistors.

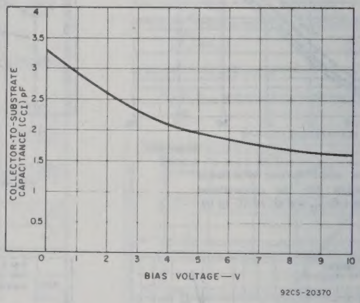


Fig.26—Collector-to-substrate capacitance vs bias voltage for the conventional transistors.

TYPICAL APPLICATIONS

Operating Considerations

Operation Considerations for the Super-Beta Differential Cascode Amplifier

An internal voltage-limiting network (diodes D1, D2 and p-n-p transistor Q5) incorporated in the differential cascode amplifier, assures that the applied collector-to-emitter voltage of each super-beta unit is maintained below two volts. Fig. 27 shows a typical bias arrangement of the super-beta differential cascode amplifier.

Bias current for this network must be supplied by an external source. This bias current can be obtained by simply connecting a resistor from Pin 11 to the positive supply of the differential amplifier. The return path for most of the bias current is through the substrate, Pin 5, rather than through the common emitter, Pin 8. This arrangement provides superior common-mode and power-supply rejection. As a general rule-of-thumb, the current supplied into Pin 11 should be approximately 0.04 to 0.1 times the value of the quiescent current of Pin 8.

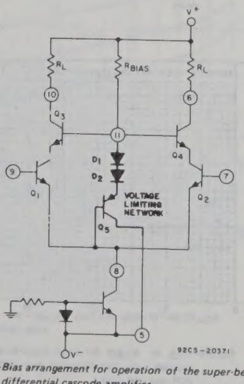


Fig.27—Bias arrangement for operation of the super-beta differential cascode amplifier.

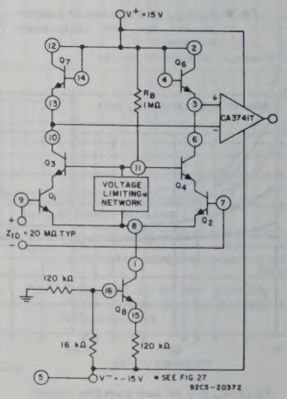


Fig.28—Super-beta Op-Amp with diode drive network.

TYPICAL APPLICATIONS (Cont'd)

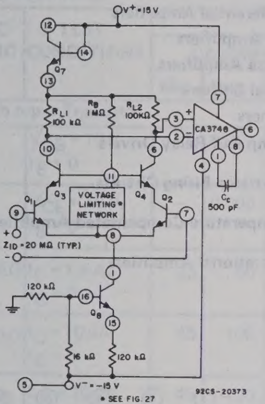


Fig.29—Super-beta Op-Amp with resistor drive network.

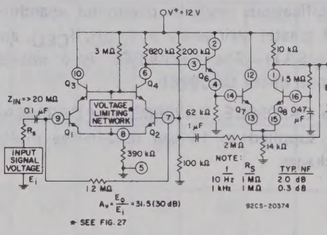


Fig.30—High-input-impedance, low-noise amplifier circuit.

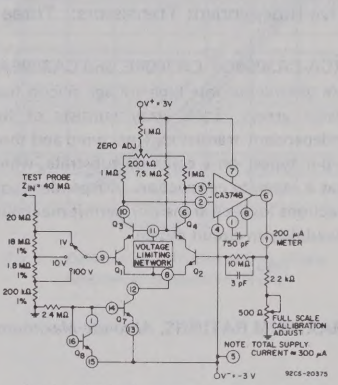


Fig.31—Typical high-input-impedance dc voltmeter circuit.

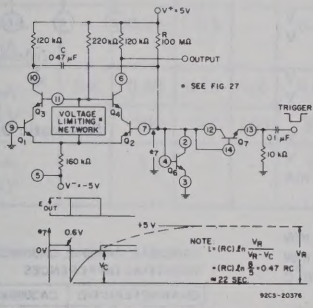


Fig.32—Long-delay monostable multivibrator circuit.

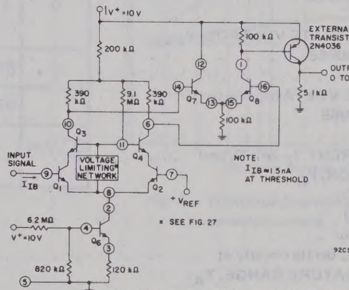


Fig.33—Low input-bias current comparator circuit.

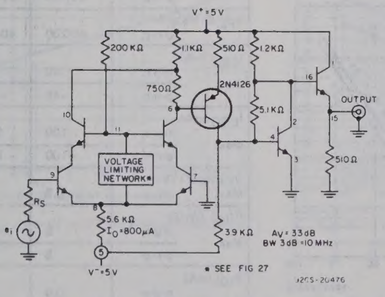


Fig.34—CA3095E wideband amplifier.

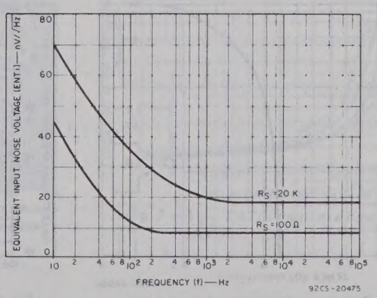


Fig.35—Equivalent input noise voltage vs. frequency for circuit of figure 34.

CA3096, CA3096A, CA3096C

N-P-N/P-N-P Transistor-Array

Five-Independent Transistors: Three n-p-n and Two p-n-p

RCA-CA3096CE, CA3096E, and CA3096AE are general-purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096AE, CA3096E, and CA3096CE are identical, except that the CA3096AE specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and V_{CE}(SAT). The CA3096CE is a relaxed version of the CA3096E.

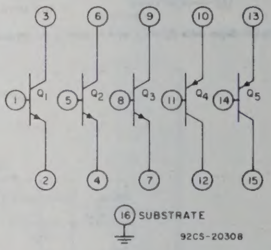
The CA3096CE, CA3096E, and CA3096AE are supplied in 16-lead dual-in-line plastic packages.

Applications:

- **Differential Amplifiers**
- **DC Amplifiers**
- **Sense Amplifiers**
- **Level Shifters**
- **Timers**
- **Lamp and Relay Drivers**
- **Thyristor Firing Circuits**
- **Temperature-Compensated Amplifiers**
- **Operational Amplifiers**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	EACH N-P-N	EACH P-N-P	
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}:			
CA3096AE, CA3096E	35	−40	V
CA3096CE	24	−24	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}:			
CA3096AE, CA3096E	45	−40	V
CA3096CE	30	−24	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}:			
CA3096AE, CA3096E	45	–	V
CA3096CE	30	–	V
EMITTER-TO-SUBSTRATE VOLTAGE, V_{EIO}:			
CA3096AE, CA3096E	–	−40	V
CA3096CE	–	−24	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}:			
CA3096E, CA3096E	6	−40	V
CA3096CE	6	−24	V
COLLECTOR CURRENT, I_C (All Types)	50	−10	mA
POWER DISSIPATION, P_D:			
Up to T_A = 55°C:			
Device (Total)	750		mW
Each Transistor	200		mW
Above T_A = 55°C derate linearly at	6.67		mW/°C
AMBIENT-TEMPERATURE RANGE, T_A:			
Operating		−55 to +125	°C
Storage		−65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.			265°C



Schematic Diagram

CA3096AE, CA3096E, CA3096CE
ESSENTIAL DIFFERENCES

CHARACTERISTIC		CA3096AE	CA3096E	CA3096CE
$V_{(BR)CEO}$ (V) Min.	n-p-n	35	35	24
	p-n-p	−40	−40	−24
$V_{(BR)CBO}$ (V) Min.	n-p-n	45	45	30
	p-n-p	−40	−40	−24
h_{FE} @ 1 mA	n-p-n	150-500	150-500	100-670
	p-n-p	20-150	20-150	15-200
h_{FE} @ 100 µA	p-n-p	40-200	40-200	30-300
I_{CBO} (nA) Max.	n-p-n	40	100	100
	p-n-p	−40	−100	−100
I_{CEO} (nA) Max.	n-p-n	100	1000	1000
	p-n-p	−100	−1000	−1000
V_{CE}(SAT) (V) Max.	p-n-p	0.5	0.7	0.7
$\lvert V_{IO} \rvert$ (mV) Max.	n-p-n	5	–	–
	p-n-p	5	–	–
$\lvert I_{IO} \rvert$ (µA) Max.	n-p-n	0.6	–	–
	p-n-p	0.25	–	–

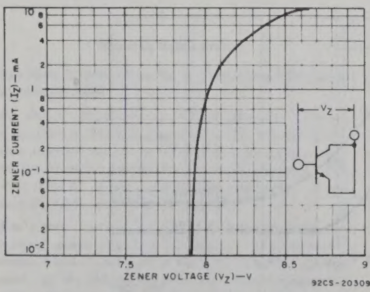


Fig. 1 – Base-to-emitter zener characteristic (n-p-n).

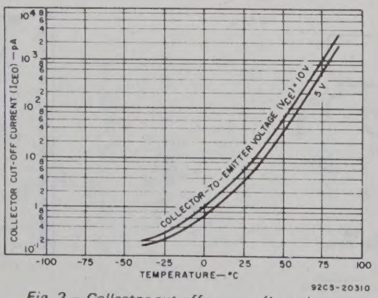


Fig. 2 – Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each n-p-n Transistor											
I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	–	0.001	40	–	0.001	100	–	0.001	100	nA
I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	–	0.006	100	–	0.006	1000	–	0.006	1000	nA
$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	35	50	–	35	50	–	24	35	–	V
$V_{(BR)CBO}$	$I_C = 10\,\mu A$, $I_E = 0$	45	100	–	45	100	–	30	80	–	V
$V_{(BR)CIO}$	$I_{CI} = 10\,\mu A$, $I_B = I_E = 0$	45	100	–	45	100	–	30	80	–	V
$V_{(BR)EBO}$	$I_E = 10\,\mu A$, $I_C = 0$	6	8	–	6	8	–	6	8	–	V
V_Z	$I_Z = 10\,\mu A$	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE(SAT)}$	$I_C = 10$ mA, $I_B = 1$ mA	–	0.24	0.5	–	0.24	0.7	–	0.24	0.7	V
V_{BE}	$I_C = 1$ mA, $V_{CE} = 5$ V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE}		150	390	500	150	390	500	100	390	670	
$\lvert \Delta V_{BE}/\Delta T \rvert$	$I_C = 1$ mA, $V_{CE} = 5$ V	–	1.9	–	–	1.9	–	–	1.9	–	mV/°C

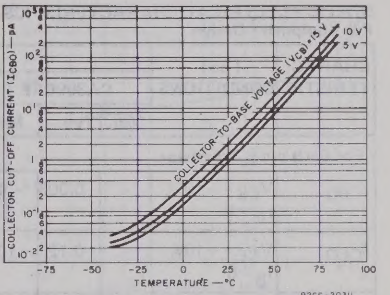


Fig. 3 – Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

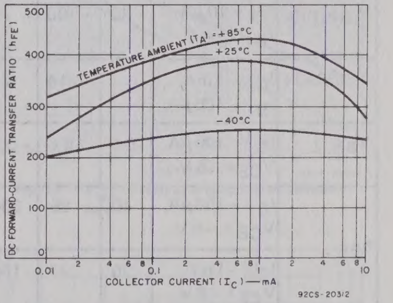


Fig. 4 – Transistor (n-p-n) h_{FE} as a function of collector current.

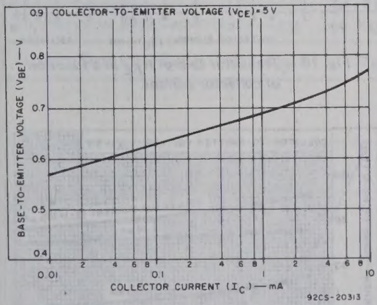


Fig. 5 – V_{BE} (n-p-n) as a function of collector current.

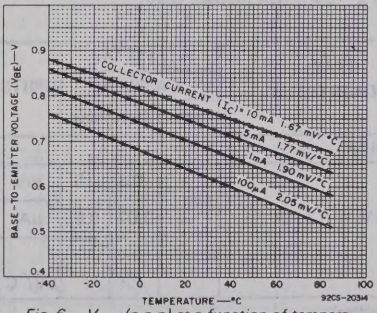


Fig. 6 – V_{BE} (n-p-n) as a function of temperature.

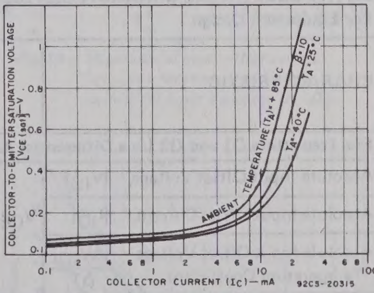


Fig. 7 – $V_{CE}(SAT)$ (n-p-n) as a function of collector current.

CA3096, CA3096A, CA3096C

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (Cont'd)
For Equipment Design

CHARAC-TERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each p-n-p Transistor											
I_{CBO}	$V_{CB} = -10$ V, $I_E = 0$	–	–0.006	–40	–	–0.06	–100	–	–0.06	–100	nA
I_{CEO}	$V_{CE} = -10$V, $I_B = 0$	–	–0.12	–100	–	–0.12	–1000	–	–0.12	–1000	nA
$V_{(BR)CEO}$	$I_C = -100\,\mu$A, $I_B = 0$	–40	–75	–	–40	–75	–	–24	–30	–	V
$V_{(BR)CBO}$	$I_C = -10\,\mu$A, $I_E = 0$	–40	–80	–	–40	–80	–	–24	–60	–	V
$V_{(BR)EBO}$	$I_E = -10\,\mu$A, $I_C = 0$	–40	–100	–	–40	–100	–	–24	–80	–	V
$V_{(BR)EIO}$	$I_{EI} = 10\,\mu$A, $I_B = I_C = 0$	–40	–100	–	–40	–100	–	–24	–80	–	V
$V_{CE(SAT)}$	$I_C = -1$ mA, $I_B = -100\,\mu$A	–	–0.16	–0.4	–	–0.16	–0.4	–	–0.16	–0.4	V
V_{BE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	–0.5	–0.6	–0.7	–0.5	–0.6	–0.7	–0.5	–0.6	–0.7	V
h_{FE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	40	85	200	40	85	200	30	85	300	
	$I_C = -1$ mA, $V_{CE} = -5$ V	20	47	150	20	47	150	15	47	200	
$\lvert\Delta V_{BE}/\Delta T\rvert$	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	–	2.2	–	–	2.2	–	–	2.2	–	mV/°C

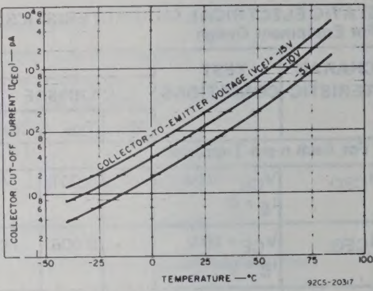


Fig. 8 – Collector cut-off current (I_{CEO}) as a function of temperature (p-n-p).

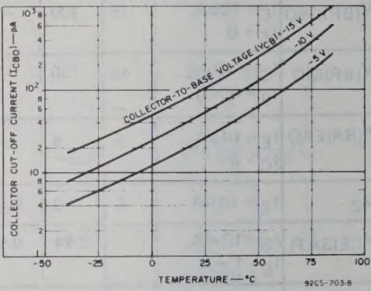


Fig. 9 – Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

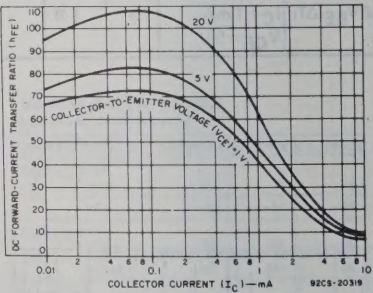


Fig. 10 – Transistor (p-n-p) h_{FE} as a function of collector current.

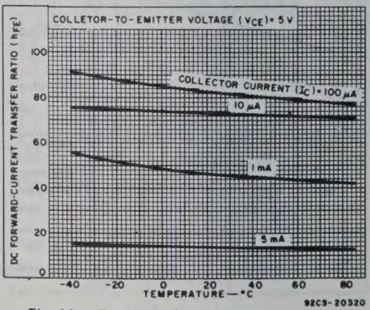


Fig. 11 – Transistor (p-n-p) h_{FE} as a function of temperature.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (CA3096AE Only)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		CA3096AE			
		Min.	Typ.	Max.	
For Transistors Q1 and Q2 (as a Differential Amplifier)					
Absolute Input Offset Voltage, $\lvert V_{IO}\rvert$	$V_{CE} = 5$ V, $I_C = 1$ mA	–	0.3	5	mV
Absolute Input Offset Current, $\lvert I_{IO}\rvert$		–	0.07	0.6	µA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	1.1	–	µV/°C
For Transistors Q4 and Q5 (As a Differential Amplifier)					
Absolute Input Offset Voltage, $\lvert V_{IO}\rvert$	$V_{CE} = -5$ V, $I_C = -100\,\mu$A $R_S = 0$	–	0.15	5	mV
Absolute Input Offset Current, $\lvert I_{IO}\rvert$		–	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	0.54	–	µV/°C

DYNAMIC
ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$
Typical Values Intended Only for Design Guidance

CHARACTERISTICS		TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor				
Noise Figure (low frequency), NF		$f = 1\ kHz$, $V_{CE} = 5\ V$, $I_C = 1\ mA$, $R_S = 1\ k\Omega$	2.2	dB
Low-Frequency, Input Resistance, R_i		$f = 1.0\ kHz$, $V_{CE} = 5\ V$, $I_C = 1\ mA$	10	kΩ
Low-Frequency Output Resistance, R_o			80	kΩ
Admittance Characteristics:				
Forward Transfer Admittance, y_{fe}	g_{fe}	$f = 1\ MHz$, $V_{CE} = 5\ V$, $I_C = 1\ mA$	7.5	mmho
	b_{fe}		−j13	
Input Admittance, y_{ie}	g_{ie}		2.2	mmho
	b_{ie}		j3.1	
Output Admittance, y_{oe}	g_{oe}		0.76	mmho
	b_{oe}		j2.4	
Gain-Bandwidth Product, f_T		$V_{CE} = 5\ V$, $I_C = 1.0\ mA$	280	MHz
		$V_{CE} = 5\ V$, $I_C = 5\ mA$	335	
Emitter-to-Base Capacitance, C_{EB}		$V_{EB} = 3\ V$	0.75	pF
Collector-to-Base Capacitance, C_{CB}		$V_{CB} = 3\ V$	0.46	pF
Collector-to-Substrate Capacitance, C_{CI}		$V_{CI} = 3\ V$	3.2	pF
For Each p-n-p Transistor				
Noise Figure (low frequency), NF		$f = 1\ kHz$, $I_C = 100\ \mu A$, $R_S = 1\ k\Omega$	3	dB
Low-Frequency Input Resistance, R_i		$f = 1\ kHz$, $V_{CE} = 5\ V$,	27	kΩ
Low-Frequency Output Resistance, R_o		$I_C = 100\ \mu A$	680	kΩ
Gain Bandwidth Product, f_T		$V_{CE} = 5\ V$, $I_C = 100\ \mu A$	6.8	MHz
Emitter-to-Base Capacitance, C_{EB}		$V_{EB} = -3\ V$	0.85	pF
Collector-to-Base Capacitance, C_{CB}		$V_{CB} = -3\ V$	2.25	pF
Base-to-Substrate Capacitance, C_{BI}		$V_{BI} = 3\ V$	3.05	pF

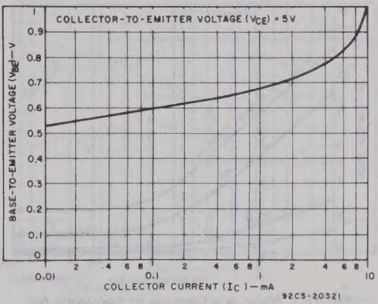


Fig. 12 – V_{BE} (p-n-p) as a function of collector current.

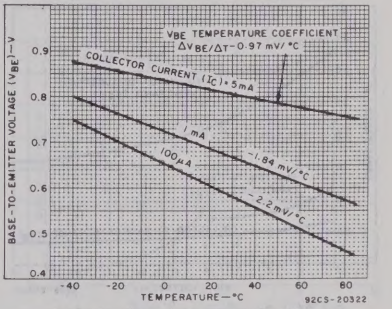


Fig. 13 – V_{BE} (p-n-p) as a function of temperature.

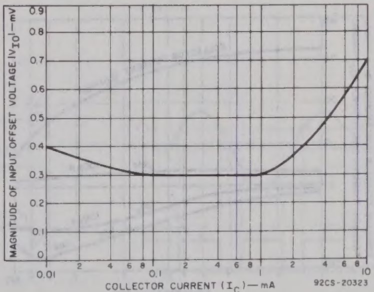


Fig. 14 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor $Q_1–Q_2$.

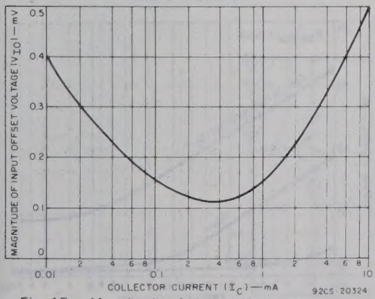


Fig. 15 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistor $Q_4–Q_5$

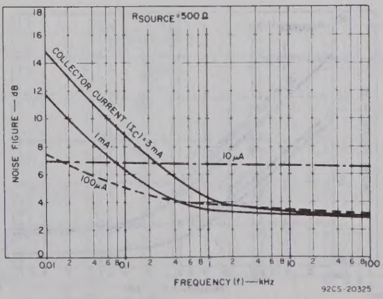


Fig. 16 – Noise figure as a function of frequency for n-p-n transistors.

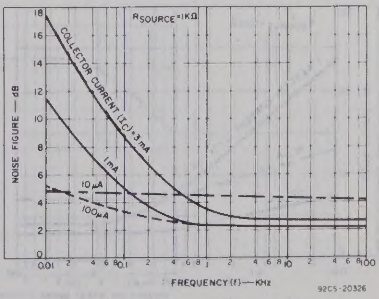


Fig. 17 – Noise figure as a function of frequency for n-p-n transistors.

CA3096, CA3096A, CA3096C

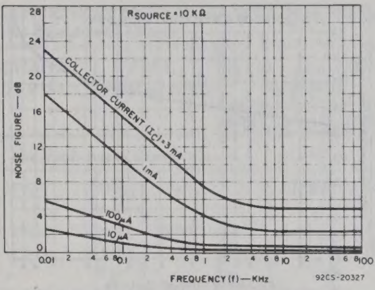


Fig. 18 — Noise as a function of frequency for n-p-n transistors.

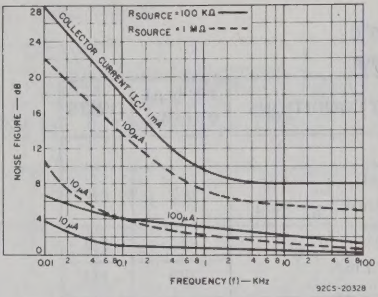


Fig. 19 — Noise figure as a function of frequency for n-p-n transistors.

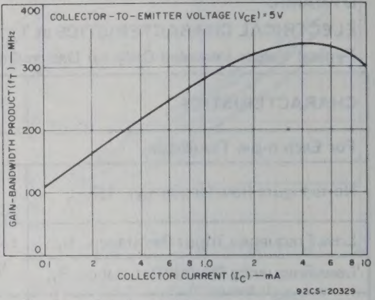


Fig. 20 — Gain-bandwidth product as a function of collector current (n-p-n).

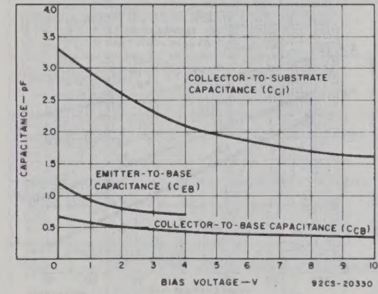


Fig. 21 — Capacitance as a function of bias voltage (n-p-n).

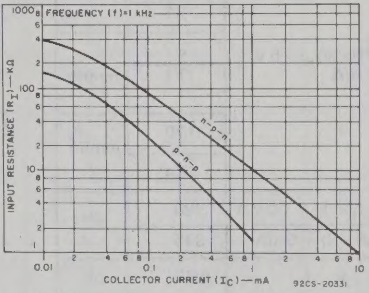


Fig. 22 — Input resistance as a function of collector current.

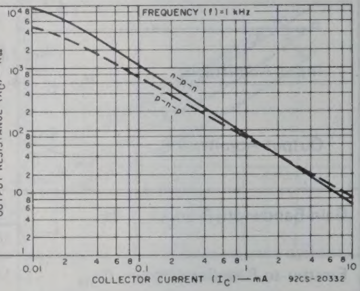


Fig. 23 — Output resistance as a function of collector current.

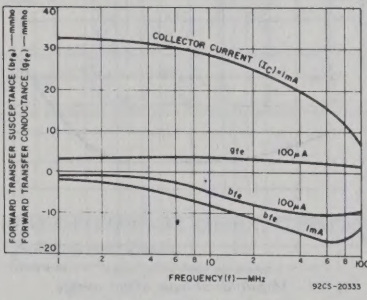


Fig. 24 — Forward transconductance as a function of frequency.

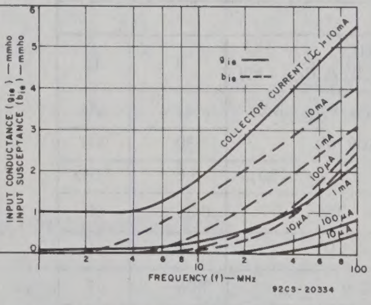


Fig. 25 — Input admittance as a function of frequency.

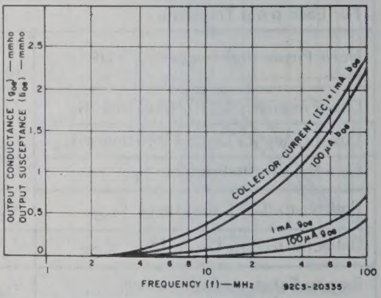


Fig. 26 — Output admittance as a function of frequency.

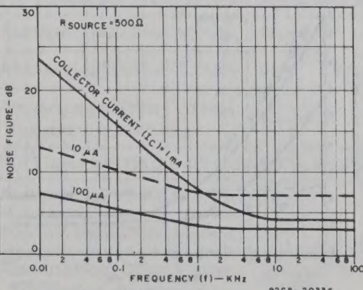


Fig. 27 — Noise figure as a function of frequency (p-n-p).

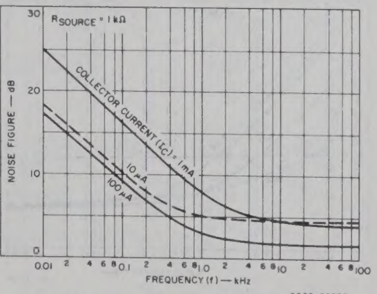


Fig. 28 — Noise figure as a function of frequency (p-n-p).

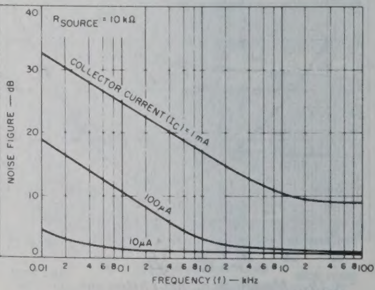


Fig. 29 — Noise figure as a function of frequency (p-n-p).

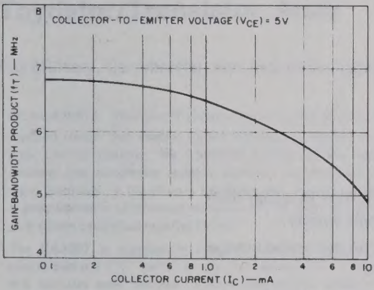


Fig. 30 – Gain-bandwidth product as a function of collector current (p-n-p).

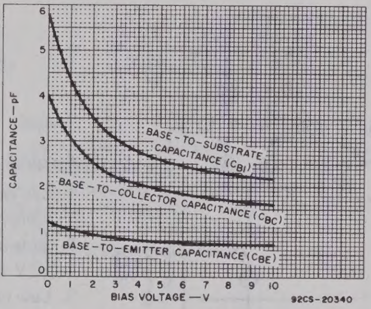


Fig. 31 – Capacitance as a function of bias voltage (p-n-p).

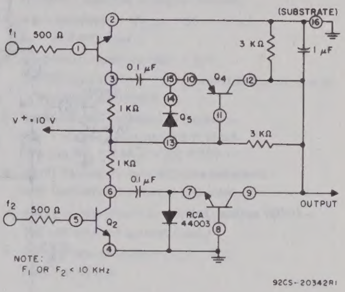


Fig. 32 – Frequency comparator using CA3096E.

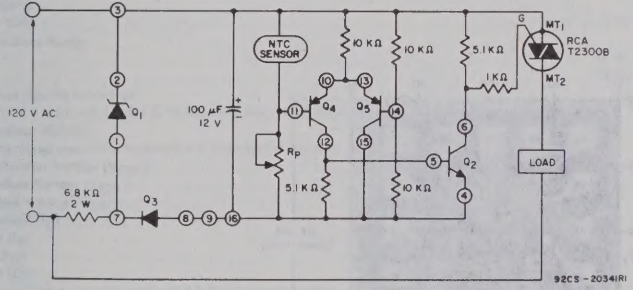


Fig. 33 – Line-operated level switch using CA3096AE or CA3096E.

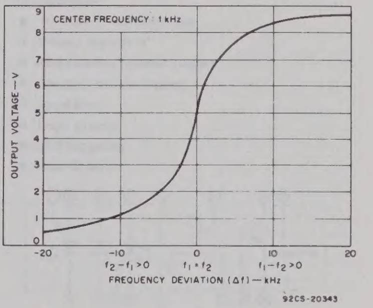


Fig. 34 – Frequency comparator characteristics.

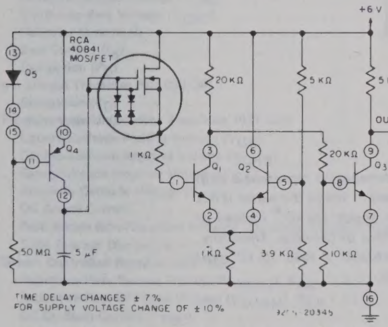


Fig. 35 – One-minute timer using CA3096AE and a MOS/FET.

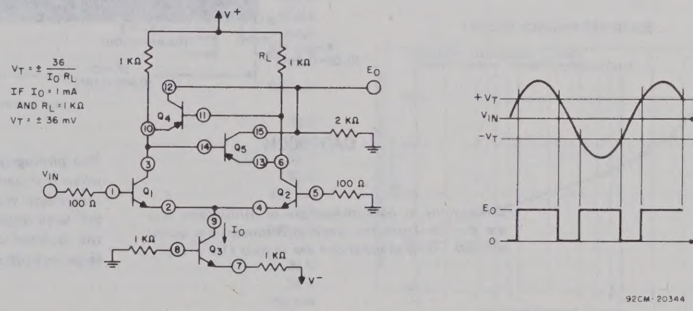


Fig. 36 – CA3096AE small-signal zero-voltage detector having noise immunity.

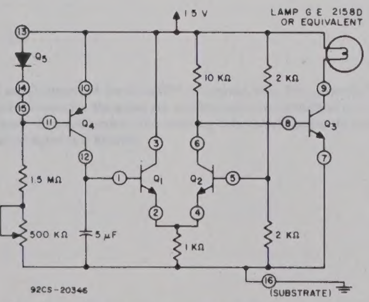


Fig. 37 – Ten-second timer operated form 1.5-volt supply using CA3096E.

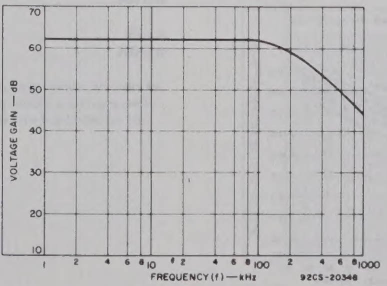
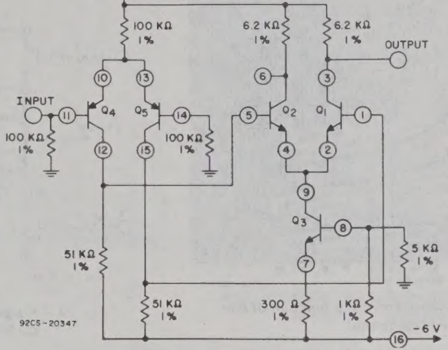


Fig. 38 – Gain-frequency characteristics.

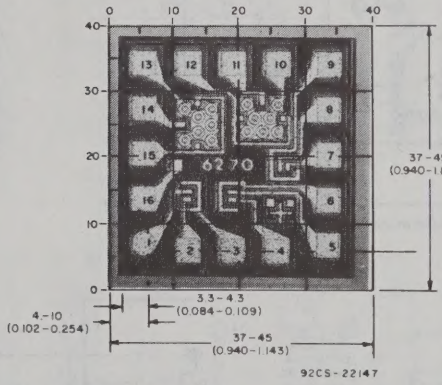
CA3096, CA3096A, CA3096C



Features:

1. Can be operated with either dual supply or single supply.
2. Wide-input common-mode range +5 V to −5 V.
3. Low bias current: <1 μA.

Fig. 39 – Cascade of differential amplifiers using CA3096AE.



CA3096CH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3097E

Thyristor/Transistor Array

For Military, Commercial, and Industrial Applications

RCA-CA3097E Thyristor/Transistor Array is a monolithic integrated circuit that enables circuit designers to further integrate control systems. The CA3097E consists of five independent and completely isolated elements on one chip: an n-p-n transistor, a p-n-p/n-p-n transistor pair, a zener diode, a programmable unijunction transistor (PUT), and a sensitive-gate silicon controlled rectifier (SCR).

The CA3097 is supplied in either the 16-lead dual-in-line plastic package ("E" suffix) or the chip version ("H" suffix), and operates over the full military-temperature range of −55 to +125°C.

Includes:

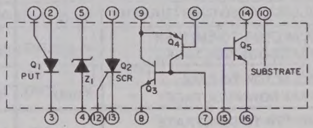
- **Uncommitted n-p-n Transistor**
- **Sensitive-Gate Silicon Controlled Rectifier**
- **Programmable Unijunction Transistor (PUT)**
- **p-n-p/n-p-n Transistor Pair**
- **Zener Diode**
- **Separate Substrate Connection**

Features:

- **Complete isolation between elements**
- **n-p-n transistor — V_{CEO} = 30 V (min.) I_C = 100 mA (max.)**
- **p-n-p/n-p-n transistor pair — beta ≥ 8000 (typ.) @ I_C = 10 mA, individual p-n-p, n-p-n, or transistor pair operation**
- **Programmable unijunction transistor (PUT) — peak-point current = 15 nA (typ.) at R_G = 1 MΩ; V_{AK} = ±30 V**
- **(PUT) Extremely long RC time constants with low value of external capacitor**
- **Sensitive-gate silicon controlled rectifier (SCR) — 150 mA forward current (max.)**
- **Zener-diode impedance (Z_Z) = 15Ω (typ.) at 10 mA**

Applications:

- **Timers**
- **Light dimmers/motor controls**
- **Oscillators**
- **"One-shot" multivibrators**
- **Voltage regulators**
- **Comparators, Schmitt triggers**
- **Constant-current sources**
- **Amplifiers**
- **Logic circuits**
- **SCR triggering**
- **Pulse Circuits**



92CS-21935

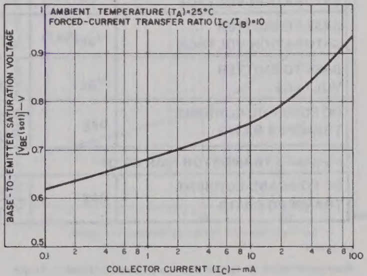
Fig. 1 — Schematic diagram of CA3097E.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Isolation Voltage, any terminal to substrate*	+50 V
Dissipation, Total Package:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly at 6.67 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C
Each n-p-n Transistor (Q3,Q5)	
The following ratings apply with terminals 6 & 9 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	30 V
Collector-to-Base Voltage (V_{CBO})	50 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	100 mA
Base Current (I_B)	20 mA
Dissipation (P_D)	500 mW
p-n-p Transistor (Q4)	
The following ratings apply with terminals 7 & 8 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	−40 V
Collector-to-Base Voltage (V_{CBO})	−50 V
Emitter-to-Base Voltage (V_{EBO})	−40 V
Collector Current (I_C)	−10 mA
Base Current (I_B)	−3 mA
Dissipation (P_D)	200 mW
p-n-p/n-p-n Transistor Pair (Q3,Q4)	
Dissipation (P_D)	500 mW
Programmable Unijunction Transistor, PUT (Q1)	
Gate-to-Cathode Positive Voltage (V_{GK})	30 V
Gate-to-Cathode Negative Voltage (V_{GKR})	5 V
Gate-to-Anode Negative Voltage (V_{GA})	30 V
Anode-to-Cathode Voltage (V_{AK})	±30 V
DC Anode Current	150 mA
Peak Anode Non-Recurrent Forward (On-State) Current (10 μs pulse)	2 A
Total Average Dissipation	300 mW
Silicon Controlled Rectifier, SCR (Q2)	
Repetitive Peak Reverse Voltage (V_{RRXM}), R_{GK} = 1 KΩ	30 V
Repetitive Peak Off-State Voltage (V_{DRXM}), R_{GK} = 1 kΩ	30 V
DC On-State Current (I_{TDC})	150 mA
Peak Surge (Non-Repetitive) On-State Current (10 μs pulse)	2 A
Forward Peak Gate Current (I_{GFM})	20 mA
Peak Gate-to-Cathode Reverse Voltage (V_{GRM})	5 V
Total Average Dissipation	300 mW
Zener Diode, (Z1)	
DC Current (I_Z)	25 mA
Dissipation (P_D)	250 mW

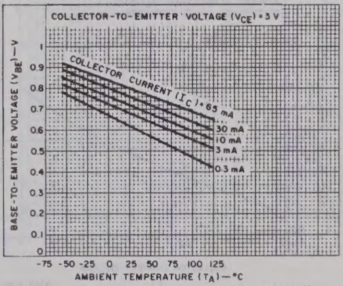
* One or more of the terminals of each element of the CA3097E is isolated from the substrate by a junction diode. In order to maintain electrical isolation between elements, the substrate terminal must be connected to a voltage which is no more positive than that of any other terminal. To avoid undesirable coupling between elements, the substrate terminal (terminal 10) should be maintained at either dc or signal (ac) ground.

TYPICAL CHARACTERISTICS



92CS-21902

Fig.2 — Base-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.



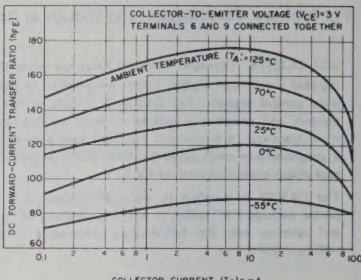
92CS-21903

Fig.3 — Base-to-emitter voltage vs. ambient temperature for n-p-n transistors Q3 & Q5.

ELECTRICAL CHARACTERISTICS

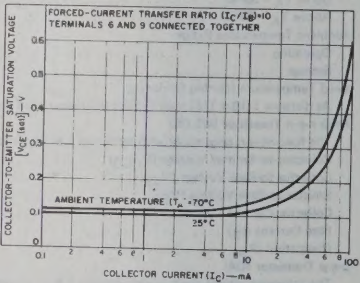
CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
n-p-n TRANSISTORS Q3, Q5 (TERMINALS 6 and 9 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = 100μA, I_B = 0		30	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0		50	–	–	V
COLLECTOR-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0		50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0		5	7.5	10	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE}(SAT)$	I_C = 50mA, I_B = 5mA	5	–	–	0.65	V
		I_C = 10mA, I_B = 1 mA		–	0.10	–	
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE}(SAT)$	I_C = 10mA, I_B = 1mA	2	–	0.76	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.73	0.85	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = 3V, I_C = 10mA	4	100	130	–	
		V_{CE} = 3V, I_C = 50mA		80	120	–	
p-n-p TRANSISTOR Q4 (TERMINALS 7 and 8 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = -10 V, I_E = 0		–	–	–1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = -10 V, I_B = 0		–	–	–10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = -100μA, I_B = 0		–40	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = -10μA, I_E = 0		–50	–	–	V
EMITTER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)EIO}$	I_{EI} = 10μA, I_B = 0, I_E = 0		–50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = –10μA, I_C = 0		–40	–	–	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE}(SAT)$	I_C = -1mA, I_B = -100μA	6	–	–	–0.33	V
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE}(SAT)$	I_C = -1mA, I_B = –100μA-	7	–	–0.7	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = -3 V, I_C = –100μA	8	–0.5	–0.6	–0.7	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = – 3 V, I_C = –100μA V_{CE} = –3 V, I_C = –1 mA	9	30 40	60 –	– –	
n-p-n/p-n-p TRANSISTOR PAIR Q3, Q4							
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} (n-p-n) = 3V, I_C = 10mA	10	–	8000	–	
		V_{CE} (n-p-n) = 3V, I_C = 50mA	10	–	6500	–	

TYPICAL CHARACTERISTICS (CONT'D)



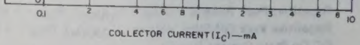
92CS-21904

Fig.4 – DC forward-current transfer ratio vs. collector current for n-p-n transistors Q3 & Q5.



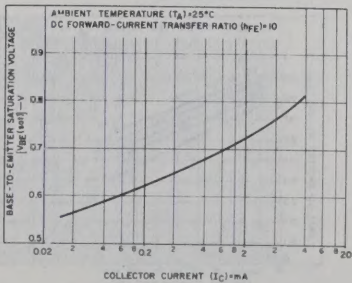
92CS-21905

Fig.5 – Collector-to-amitter saturation voltage vs. collector for n-pn- transistors Q3 & Q5.



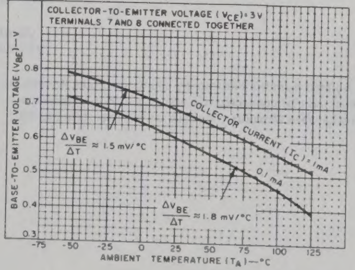
92CS-21906

Fig.6 – Collector-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.



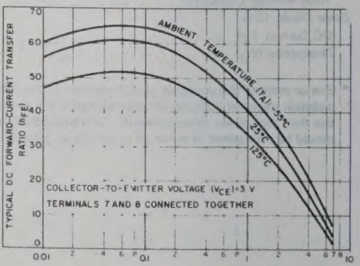
92CS-21907

Fig.7 – Base-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.



92CS-21908

Fig.8 – Base-to-emitter voltage vs. ambient temperature for p-n-p transistor Q4.



92CS-21909

Fig.9 – DC forward-current transfer ratio vs. collector current for p-n-p transistor Q4.

ELECTRICAL CHARACTERISTICS (Cont'd.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature $(T_A) = 25^oC$ Unless Otherwise Specified	FIG. NO.	LIMITS			UNITS
				Min.	Typ.	Max.	
PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT), Q1							
OFFSET VOLTAGE	V_T*	$V_S = 10V$, $R_G = 10k\Omega$	11,22[a]	0.2	–	0.7	V
		$V_S = 10V$, $R_G = 1M\Omega$		0.2	–	0.7	
ANODE-TO-CATHODE ON-STATE VOLTAGE	V_F	$I_F = 50mA$	12	–	0.90	1.5	V
		$I_F = 100mA$		–	1	–	
PEAK OUTPUT VOLTAGE	V_{OM}	$C = 0.22\mu F$ Anode Supply Voltage = 20V	13,23	–	10	–	V
PEAK-POINT CURRENT	I_P	$V_S = 10V$, $R_G = 10k\Omega$	14,22[a]	–	0.55	1	μA
		$V_S = 10V$, $R_G = 1M\Omega$	–	–	0.015	0.15	
VALLEY-POINT CURRENT	I_V	$V_S = 10V$, $R_G = 10k\Omega$	17,15	4	40	–	μA
		$V_S = 10V$, $R_G = 1M\Omega$	16	–	–	25	
GATE REVERSE CURRENT	I_{GAO}	$V_S = 30V$	22[c]	–	0.02	–	nA
GATE REVERSE CURRENT	I_{GKS}	Anode-To-Cathode Short, V_S, = 30V	22[d]	–	0.2	–	nA
OUTPUT PULSE RISETIME	t_r	Anode-Supply Voltage = 20V $C = 0.22\ \mu F$	23	–	60	–	ns
SILICON CONTROLLED RECTIFIER (SCR), Q2							
PEAK OFF-STATE CURRENT:							
FORWARD	I_{DXM}	$V_{DRXM} = 30V$, $R_{GK} = 1k\Omega$	24	–	–	2	μA
REVERSE	I_{RXM}	$V_{RRXM} = 30V$, $R_{GK} = 1k\Omega$	24	–	–	2	
FORWARD DC VOLTAGE DROP	V_T	$I_T = 50\ mA$	18	–	0.90	1.5	V
GATE-TO-SOURCE TRIGGER CURRENT	I_{GS}	$T_A = 25^oC$	26	–	33	100	μA
		$T_A = -55^oC$	26	–	50	–	
DC GATE-TRIGGER VOLTAGE	V_{GT}	$V_L = 10V$, $R_L = 100\Omega$	19	–	0.55	0.75	V
HOLDING CURRENT	I_{HO}	$R_{GK} = 1k\Omega$	20,24	–	1.2	–	mA
CRITICAL RATE-OF-RISE OF OFF-STATE VOLTAGE	dv/dt	EXPONENTIAL RISE, $R_{GK} = 1k\Omega$, $V_{DRXM} = 30V$	25	–	150	–	V/μs
GATE-CONTROLLED TURN-ON TIME	t_{gt}	See Fig. 33	33	–	50	–	ns
CIRCUIT-COMMUTATED TURN-OFF TIME	t_q	See Fig. 33	33	–	10	–	μs
ZENER DIODE, Z1							
ZENER VOLTAGE	V_Z	$I_Z = 10mA$	21	7.2	8	8.8	V
ZENER IMPEDANCE	Z_Z	$I_Z = 10mA$, $f = 1kHz$		–	15	25	Ω
ZENER VOLTAGE TEMPERATURE COEFFICIENT	$(\Delta V_Z/V_Z)/\Delta T$	$I_Z = 10mA$		–	+0.05	–	%/°C
	$\Delta V_Z/\Delta T$			–	+4	–	mV/°C
ZENER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)ZIO}$	$I_Z = 100\mu A$ TERM. 5 TO SUBSTRATE		50	80	–	V

* $V_T = V_P - V_S$ (Fig. 22)

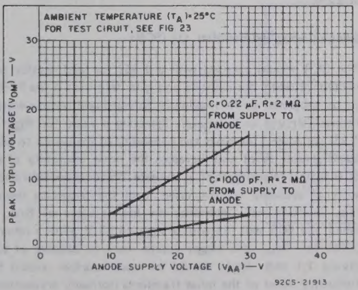


Fig.13 – Peak output voltage vs. anode supply voltage for Q1 (PUT).

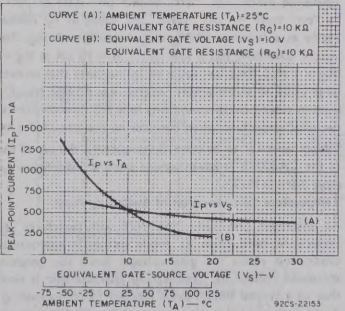


Fig.14 – Peak-point current vs. gate-source voltage and ambient temperature for Q1 (PUT).

TYPICAL CHARACTERISTICS (CONT'D)

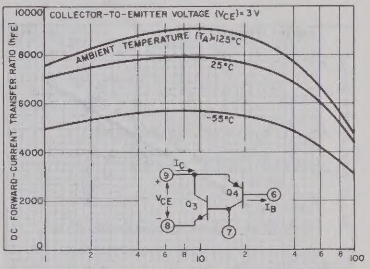


Fig.10 – DC forward-current transfer ratio vs. collector current for transistor pair Q3, Q4.

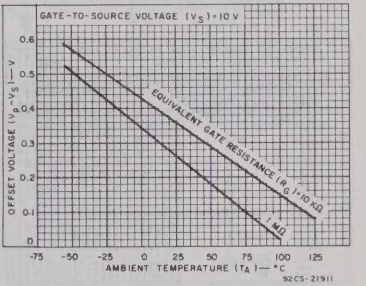


Fig.11 – Offset voltage vs. ambient temperature for Q1 (PUT).

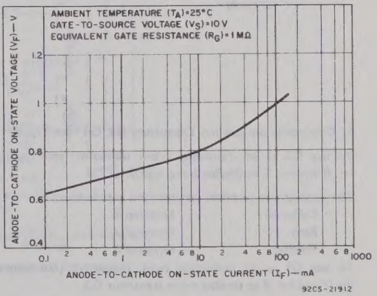


Fig.12 – Anode-to-cathode on-state voltage vs. anode-to-cathode on-state current for Q1 (PUT).

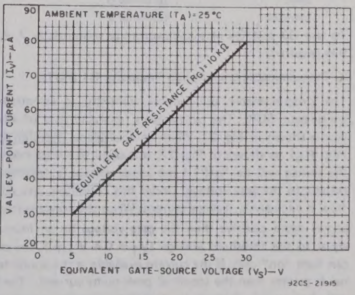


Fig.15 – Valley-point current vs. gate-source voltage for Q1 (PUT).

TYPICAL CHARACTERISTICS (CONT'D)

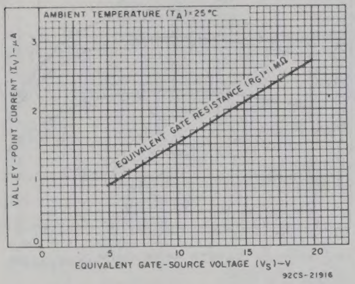


Fig.16 – Valley-point current vs. gate-source voltage for Q1 (PUT).

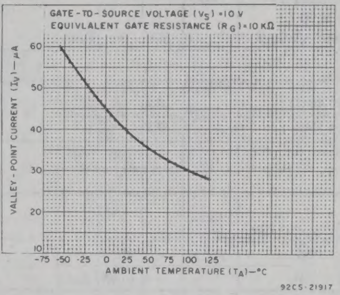


Fig.17 – Valley-point current vs. ambient temperature for Q1 (PUT).

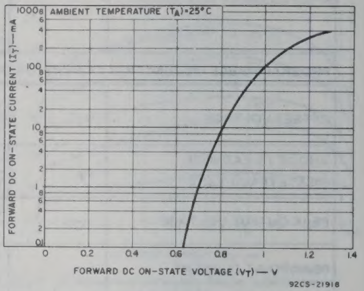


Fig.18 – Forward DC on-state current vs. on-state voltage for Q2 (SCR).

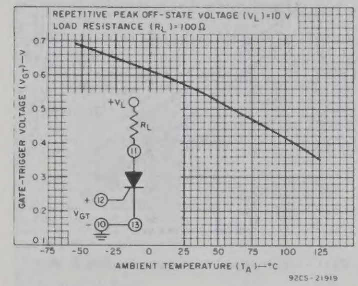


Fig.19 – Gate-trigger voltage vs. ambient temperature for Q2 (SCR).

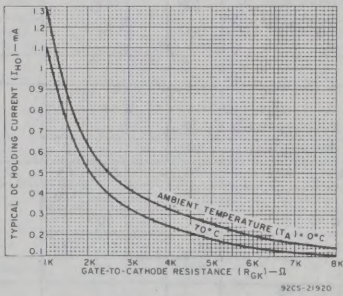


Fig.20 – Typical DC holding current vs. gate-to-cathode resistance for Q2 (SCR).

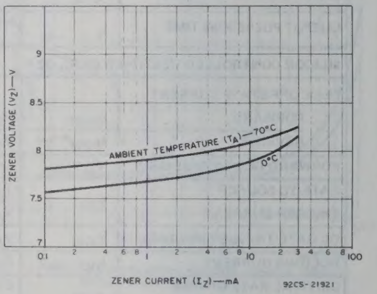


Fig.21 – Zener voltage vs. zener current for Z1.

OPERATING CONSIDERATIONS FOR CA3097E

1. Composite p-n-p/n-p-n Transistors Q3, Q4 (See Fig. 3)

To use Q3 as an individual n-p-n transistor, join terminals no. 6 and no. 9 to disable p-n-p transistor Q4.

The appropriate terminal connections are then:

Collector........... terminal 9
Base .... terminal 7
Emitter............ terminal 8

To use Q4 as an individual p-n-p transistor, join terminals no. 7 and no. 8 to disable n-p-n transistor Q3.

The appropriate terminal connections are then:

Collector........... terminal 7
Base .... terminal 6
Emitter............ terminal 9

To use Q3 and Q4 as a composite use terminals 6, 7, 8, and 9 as required.

2. Programmable Unijunction Transistor Q1 (PUT)

The programmable unijunction transistor is essentially an anode-gate SCR. The volt-ampere characteristic of the device is shown in Fig. 22. When an equivalent Thevenin source (V_S, R_G), as shown in Fig. 22, is applied to the gate terminal the device will be "off" if the anode-voltage is negative with respect to the gate voltage. Under this condition, any current flow is exclusively leakage current. When the anode voltage becomes more positive than the gate voltage by an increment equal to the threshold voltage (V_T = 0.4 V typ.), the device can turn "on" only if the current available at the anode terminal is greater than the specified peak-point current. The PUT will then switch through its negative-resistance region to the "on" state (low anode-to-gate voltage). It should be noted that I_P is not the maximum current allowed through the device, but is the current required at the peak of the V-I curve. I_P is typically a very low value of current.

After the PUT has switched to its low-impedance state, the device will remain "on" if the anode-current (I_A) exceeds the valley-point current (I_V). If $I_A<I_V$, the PUT will switch back to its high-impedance "off" state. Thus, the PUT can be made to "latch" or recover, depending on I_V. Since I_V is a function of the "on"-state gate current (which depends on R_G and V_S) a choice of R_G and/or V_S will determine the operating mode, i.e., "off" state→"on" state or "off" state → "on" state → "off" state. The value of I_V increases directly as a function of V_G and inversely with R_G. The PUT in the CA3097E has a low I_P.......I_P = 15 nA at V_S = 10 V, R_G = 1 MΩ. This low value of I_P indicates that an extremely large value of anode-supply resistor, e.g. 60 MΩ (typ.), can be used in timing circuits requiring long RC time constants. This becomes important when considering the size of the external timing capacitor to be used. Consequently, the use of the PUT in the CA3097E is advantageous since it has a lower I_P than most discrete PUT's.

Temperature Compensation of Switching Point

As described previously, the PUT will switch to its low-impedance state when its anode voltage is approximately a diode-drop above the gate voltage. Since the anode-to-gate threshold voltage vs. temperature characteristic is similar to that of a typical silicon-diode junction, a compensating series diode such as used in the circuit of Fig. 29 (Z1 connected as forward-biased diode) considerably reduces the effect of temperature on the switching point.

Bypassing Anode Current

If the PUT gate equivalent source is such that $I_A>I_V$, the PUT will remain "on". A method for turning the PUT off is by shunting current away from the anode until $I_A<I_V$. An example of this technique is the oscillator circuit of Fig. 29. Q3 transistor is turned "on" after the PUT fires and shunts current away from the anode, thereby forcing $I_A<I_V$. The PUT then turns "off" allowing C_T to recharge through R_T, to repeat the cycle.

Protecting The PUT Against Discharge Current Of The Capacitor

A current-limiting resistor in series with the PUT is normally required to dissipate capacitive discharge energy (see Figs. 23 and 29).

Silicon Controlled Rectifier, Q2 (SCR)

The SCR should be used with a 1 kΩ (or less) resistor connected between the cathode and gate terminals if the SCR is to be subjected to its maximum forward and reverse voltage ratings (V_{DXM} and V_{RXM}). Selecting a value for R_{GK} of 1 kΩ (or lower) increases the capability of the device to withstand greater dv/dt and increases the noise immunity of the SCR against false triggering at the gate. Practical considerations such as available current drive from the triggering devices (e.g., a PUT) will determine the lowest value of R_{GK} at which the SCR will fire with a V_{GK}≈0.55 V. With a value of 500Ω for R_{GK}, the trigger source must be capable of supplying 1.1 mA. R_{GK} should be non-inductive within the frequency band of the noise transients normally encountered in a particular application.

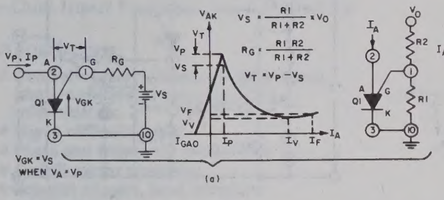


Fig. 22 – General anode characteristics for Q1 (PUT).

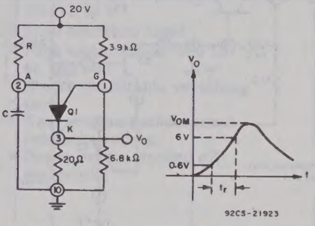


Fig. 23 – Output pulse characteristics for Q1 (PUT).

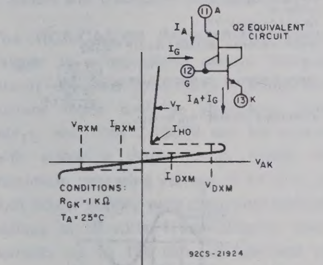


Fig. 24 – Principle voltage-current characteristics for Q2 (SCR).

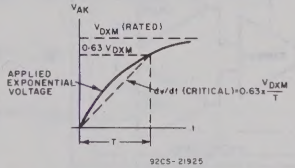
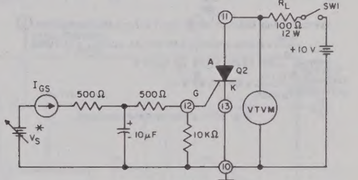


Fig. 25 – Definition of critical rate of rise of off-state voltage for Q2 (SCR).



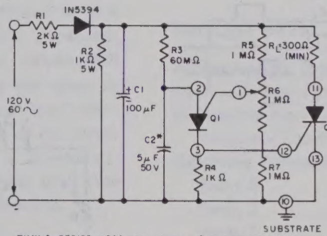
WITH SW1 CLOSED, INCREASE V_S UNTIL SCR FIRES (VTVM DROPS FROM 10V TO APPROXIMATELY 1V). I_{GS} (TRIGGER) IS MEASURED JUST PRIOR TO THIS TRIGGERING POINT. NOTE THAT I_{GS} MAY DECREASE AS V_S IS INCREASED DUE TO CURRENT DRAWN OUT OF THE GATE TERMINAL OF THE SCR AS IT TURNS ON. TO UNLATCH THE SCR OPEN SW1.

* V_S SHOULD BE CAPABLE OF SUPPLYING MILLIVOLT INCREMENTS NEAR THE TRIGGER POINT

92CS-21926

Fig. 26 – Test circuit for determining I_{GS} in Q2 (SCR).

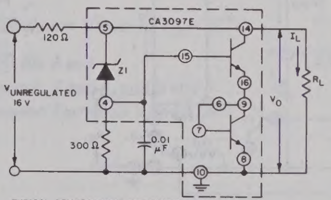
APPLICATIONS CIRCUITS



TIMING PERIOD ≈ 200 SEC WITH 1 MΩ POT CENTERED
TIMING CYCLE BEGINS WHEN AC IS APPLIED
* SPRAGUE TYPE 430B, 5μF AT 50 V
SPRAGUE TYPE 630B, 5μF AT 50 V
OR EQUIVALENT

92CS-21927

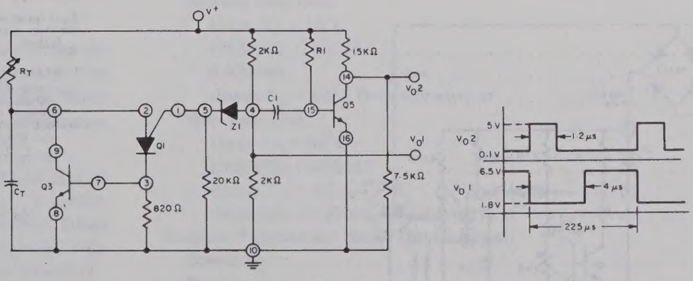
Fig. 27 – AC line-operated one-shot timer.



TYPICAL TEMPERATURE CHARACTERISTIC
@ $R_L = 330\,\Omega, \frac{\Delta V_O/V_O}{\Delta T} \times 100 = \pm 0.01\,\%/°C$
TYP LOAD REGULATION @ I_L = 0 TO 40 mA, $(\Delta V_O/V_O) \times 100 =$ −3% (NO LOAD TO FULL LOAD)
TYP LINE REGULATION @ $R_L = 330\,\Omega, \frac{\Delta V_O/V_O}{\Delta V_{UNREG}} \times 100 = \pm 0.55\,\%/V$

92CS-21928

Fig. 28 – Temperature-compensated shunt regulator.



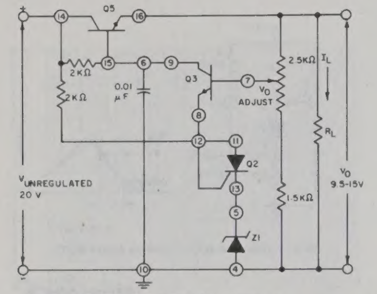
PULSE RATE ADJUSTED BY VARYING R_T OR C_T.
OUTPUT PULSE WIDTH ADJUSTED BY R_1C_1 DIFFERENTIATING TIME CONSTANT

TYPICAL OPERATION FOR:
$V^+ = 15$ V, $C_T = 0.1\,\mu F$, $R_T = 4.3\,K\Omega$
$C_1 = 82$ pF, $R_1 = 60\,K\Omega$

92CM-21929

Fig. 29 – Pulse generator.

APPLICATIONS CIRCUITS (CONT'D)



TYPICAL LOAD REGULATION @ $V_O = 12$ V, $I_L = 0$ TO 40 mA

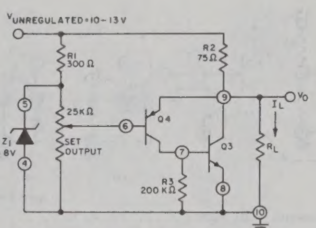
$$\frac{\Delta V_O}{V_O} \times 100 = \pm 0.4\ \% \text{ (NO LOAD TO FULL LOAD)}$$

TYPICAL LINE REGULATION @ $V_O = 12$ V

$$\frac{\Delta V_O / V_O}{\Delta V_{UNREG}} \times 100 = \pm 0.45\ \% / V$$

92CS-21930

Fig. 30 – Series voltage regulator.



TYPICAL LOAD REGULATION @ $V_O = 7$ V, $I_L = 0$ TO 40 mA

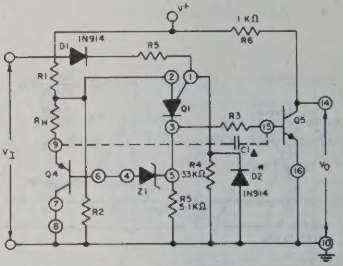
$$\frac{\Delta V_O}{V_O} \times 100 = -1.1\ \%$$

TYPICAL LINE REGULATION @ $V_O = 7$ V, $I_L = 20$ mA

$$\frac{\frac{\Delta V_O}{V_O}}{\Delta V_{UNREGULATED}} = \pm 0.85\ \% / \text{VOLT}$$

92CS-21931

Fig. 31 – 5 to 7.5 V shunt regulator.

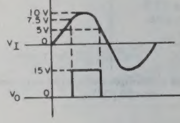


▲ OPTIONAL SPEED-UP CAPACITOR
* REQUIRED IF V_I SWINGS BELOW GROUND

TYPICAL OPERATING CONDITIONS:
FREQUENCY IN = 0-10 KHz
SUPPLY VOLTAGE (V^+) = 15 V
R1, R2, R_H = 5.1 KΩ
R3 = 6.2 KΩ, R_S = 300 Ω
C_1 = 820 pF
$V_{TH}U$ = 7.5 V, $V_{TH}L$ = 5 V
HYSTERESIS VOLTAGE = 2.5 V
UPPER THRESHOLD VOLTAGE ($V_{TH}U$) $\approx V^+ \frac{R2}{R1+R2}$

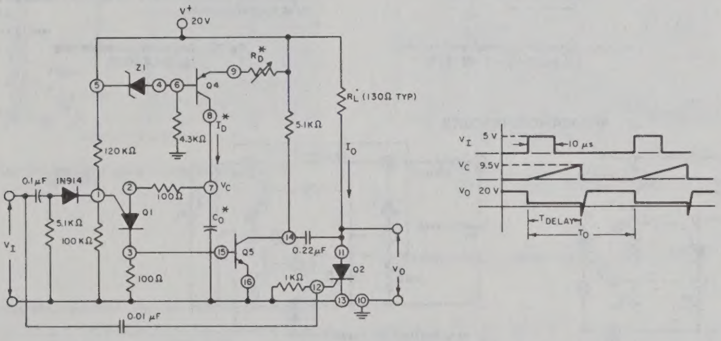
LOWER THRESHOLD VOLTAGE ($V_{TH}L$) $\approx \dfrac{(V^+)\left(\frac{R2\ R_H}{R2+R_H}\right)}{\frac{R2\ R_H}{R2+R_H} + R1}$

HYSTERESIS VOLTAGE = $V_{TH}U - V_{TH}L$



92CM-21932

Fig. 32 – Schmitt trigger.

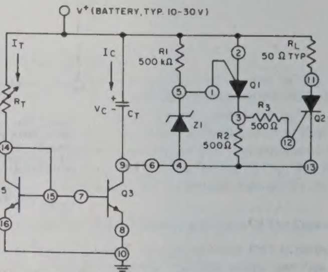


*MONOSTABLE DELAY TIME SET BY ADJUSTMENT OF I_D (VARY R_D) OR BY C_D. I_D MUST BE GREATER THAN I_V OF Q1 (PUT) FOR MONOSTABLE OPERATION.

Q2 (SCR) SWITCHING TIMES:
GATE-CONTROLLED TURN-ON TIME (t_{gt}) = 50 ns (TYP)
CIRCUIT-COMMUTATED TURN-OFF TIME (t_q) = 10 μs (TYP)

92CM-21933

Fig. 33 – Monostable multivibrator with variable delay.



T_{OFF} = TIMING PERIOD (NO LOAD CURRENT)
PUT FIRES WHEN $V_C \approx 8$ V
$V_C = \frac{I_C\ (T_{OFF})}{C_T}$, $I_C \approx I_T$ (Q3, Q5 MATCHED)

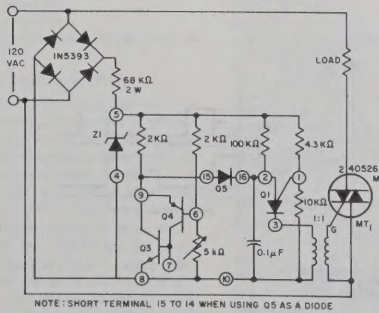
I_T SET BY ADJUSTING R_T. $I_T \approx \frac{V^+ - 0.7}{R_T}$

T_{ON} = CAPACITOR DISCHARGE TIME THROUGH LOAD. LOAD TURNS OFF WHEN SCR ANODE CURRENT FALLS BELOW HOLDING CURRENT (I_{HO}). TYPICAL I_{HO} = 1.2 mA

EXAMPLE: FOR TIMING PERIOD OF 8.3 MIN
C_T = 1000 μF, I_T = 16 μA
$R_T = \frac{V^+ - 0.7}{I_T}$ (FOR V^+ = 16 V, $R_T \approx 1$ MΩ)

92CS-21934

Fig.34 – Low-current-drain battery-operated long interval astable timer.



NOTE: SHORT TERMINAL 15 TO 14 WHEN USING Q5 AS A DIODE

92CS-22178

Fig.35 – Phase control circuit.

Programmable Schmitt Trigger

— With Memory

—Dual-Input Precision Level Detectors

Applications:

- **Control of relays, heaters, LED's lamps, photo-sensitive devices, thyristors, solenoids, etc.**
- **Signal reconditioning**
- **Phase and frequency modulators**
- **On/off motor switching**
- **Schmitt triggers, level detectors**
- **Time delays**
- **Overvoltage, overcurrent, overtemperature protection**
- **Battery-operated equipment**
- **Square and triangular-wave generators**

Features:

- **Programmable operating current**
- **Micropower standby dissipation**
- **Direct control of currents up to 150 mA**
- **Low input on/off current of less than 1 nA for programmable bias current of 1 μA**
- **Built-in hysteresis: 20 mV max.**
- **Programmable hysteresis: 20 mV to V+**
- **Dual reference input**
- **High sensor range: 100 Ω to 100 MΩ**
- **Stable predictable switching levels**
- **Temperature-compensated reference voltage**
- **Power can be strobed off via term. 2**

The RCA-CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with maximum operating voltage of ±8 volts. It can directly control currents up to 150 mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3098 contains the following major circuit-function features (see Fig. 1):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and otuput stages: these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

The CA3098 is supplied in the 8-lead dual-in-line plastic package ("Mini-Dip", E suffix), 8-lead TO-5 style package (T suffix), 8-lead TO-5-style package with formed leads "DIL-CAN" (S suffix), and in chip form (H suffix).

For information on another RCA Dual-Input Precision Level Detector, see the data bulletin for the RCA-CA3099E, File No. 620.

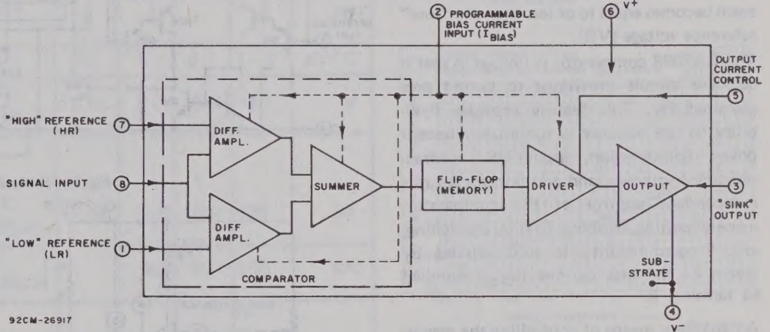


Fig. 1 – Block diagram of CA3098 programmable Schmitt trigger.

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$:*

Supply Voltage Between Terminals 6 and 4,	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 8 and 1, and Terminals 7 and 8	10	V
Operating Voltage Range:		
Term. 8	V^- to V^+	
Term. 7	(V^- plus 2.0 V) to V^+	
Term. 1	(V^-) to (V^+ minus 2.0 V)	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programmable Bias Current (Term. 2)	1	mA
Output Current Control (Term. 5)	15	mA
Power Dissipation:		
Without Heat Sink:		
Up to $T_A = 55°C$		
CA3098S, CA3098T	630	mW
CA3098E	630	mW
Above $T_A = 55°C$ Derate linearly at	6.67	mW/°C
With Heat Sink:		
Up to $T_A = 55°C$		
CA3098S, CA3098T	1.6	W
Above $T_A = 55°C$		
CA3098S, CA3098T Derate linearly at	16.67	mW/°C
Ambient Temperature Range (All Packages):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

CA3098 Types

General Description of Circuit Operation (Refer to Figs. 2, 3, 4)

When the signal-input voltage of the CA3098 is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2.

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 5. Figs. 3 and 4 highlight the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).

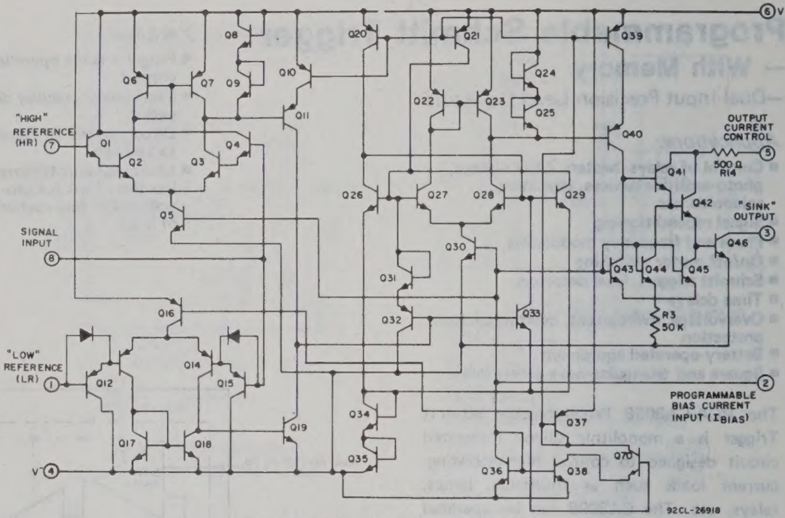

⑥ V+
"HIGH" REFERENCE (HR) ⑦
SIGNAL INPUT ⑧
"LOW" REFERENCE (LR) ①
V- ④
OUTPUT CURRENT CONTROL ⑤
500 Ω R14
"SINK" OUTPUT ③
R3 50 K
PROGRAMMABLE BIAS CURRENT INPUT (I_{BIAS}) ②
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q30 Q31 Q32 Q33 Q34 Q35 Q36 Q37 Q38 Q39 Q40 Q41 Q42 Q43 Q44 Q45 Q46 Q70
92CL-26918

Fig. 2 – Schematic Diagram of CA3098.

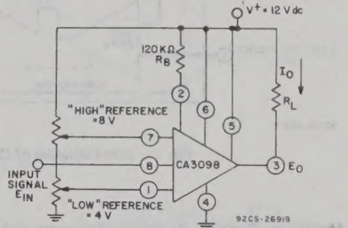


Fig. 3 – Basic hysteresis switch (Schmitt trigger).

Sequence	Input Signal Level	Output Voltage (V) (Term. 3)
1	$4 \geqslant E_{IN} > 0$	0
2	$8 \geqslant E_{IN} > 4$	0
3	$E_{IN} > 8$	12
2	$8 \geqslant E_{IN} > 4$	12
1	$4 \geqslant E_{IN} > 0$	0

Fig. 4 – Resultant output states of the CA3098, shown in Fig. 3 as a function of various input signal levels.

TYPICAL CHARACTERISTIC CURVES

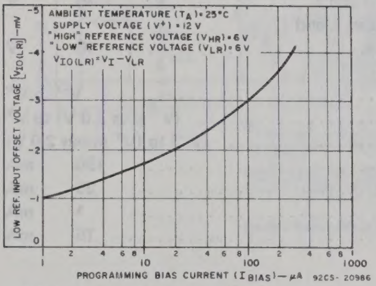


Fig. 5 – Input-offset voltage ("low" reference) vs. programming bias current.

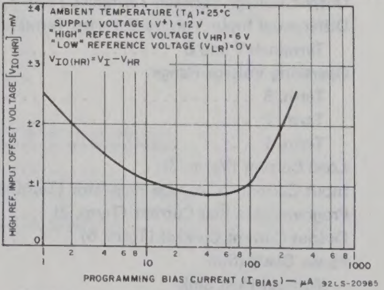


Fig. 6 – Input-offset voltage ("high" reference) vs. programming bias current.

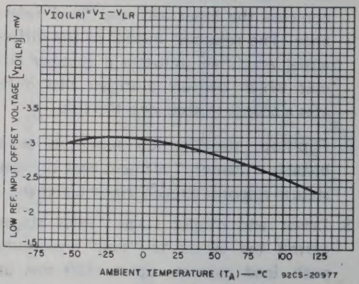


Fig. 7 – Input-offset voltage ("low reference) vs. ambient temperature.

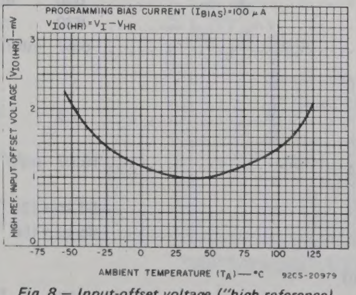


Fig. 8 – Input-offset voltage ("high reference) vs. ambient temperature.

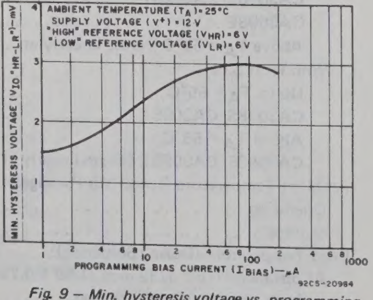


Fig. 9 – Min. hysteresis voltage vs. programming bias current.

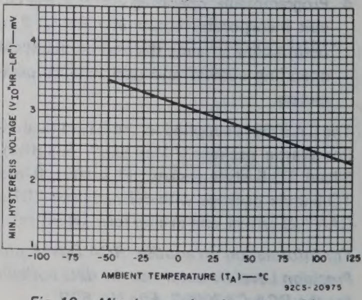


Fig. 10 – Min. hysteresis voltage vs. ambient temperature.

ELECTRICAL CHARACTERISTICS at T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Input Offset Voltage:						
"Low" Ref., $V_{IO(LR)}$	V_{LR} = Gnd, V_{HR} = 3 V I_{BIAS} = 100 μA	5	−15	−3	6	mV
"High" Ref., $V_{IO(HR)}$	V_{HR} = Gnd, V_{LR} = −3 V I_{BIAS} = 100 μA	6	−10	±10	10	
Temp. Coeff:						
"Low" Ref.	−55 °C to + 125 °C	7	–	4.5	–	μV/°C
"High" Ref.	−55 °C to + 125 °C	8	–	±8.2	–	
Min. Hysteresis Voltage $V_{IO(HR-LR)}$:	V_{REG} = 6 V, V^+ = 12 V I_{BIAS} = 100 μA	9	–	3	20	mV
Temp. Coeff.	−55°C to + 125 °C	10	–	6.7	–	μV/°C
Output Saturation Voltage, V_{CE}(SAT)	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	11,12	–	0.72	1.2	V
Total Supply Current, I_{TOTAL}:						
"ON"	V_I = 4 V, V_{REG} = 6 V; V^+ = 12 V, I_{BIAS} = 100 μA	13,14	500	710	800	μA
"OFF"	V_I = 8 V, V_{REG} = 6 V V^+ = 12 V, I_{BIAS} = 100 μA		400	560	750	μA
Input Bias Current, I_{IB}:						
$I_{B(p\text{-}n\text{-}p)}$	V_I = 4 V, V_{REG} = 6 V V^+ = 12 V, I_{BIAS} = 100 μA	15	–	42	100	nA
$I_{B(n\text{-}p\text{-}n)}$	V_I = 8 V, V_{REG} = 6 V V^+ = 12 V, I_{BIAS} = 100 μA		–	28	100	nA
Output Leakage Current, $I_{CE(OFF)}$	Current from Term. 3 when Q46 is "OFF"	–	–	–	10	μA
Switching Times:						
Delay, t_d	I_C = 100 μA	18	–	600	–	ns
Fall, t_f	I_{BIAS} = 100 μA		–	50	–	ns
Rise, t_r	V^+ = 5 V		–	500	–	ns
Storage, t_s	V_{REG} = 2.5 V		–	4.5	–	μs
Output Current, I_O	V^+ = 12 V, I_{BIAS} = 50 μA	–	100	–	–	mA

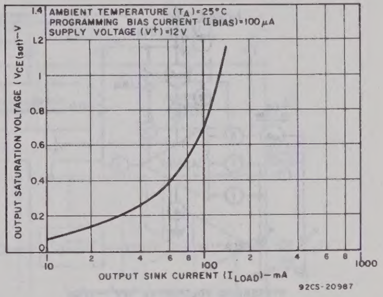


Fig. 11 – Output saturation voltage vs. output sink current.

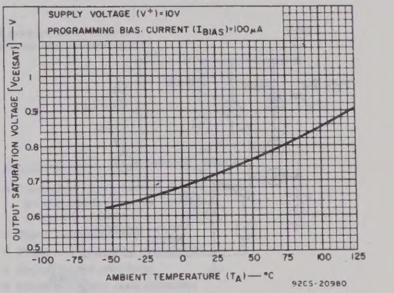


Fig. 12 – Output saturation voltage vs. ambient temperature.

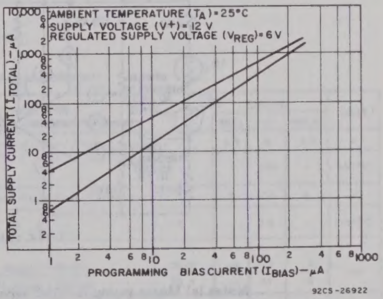


Fig. 13 – Total supply current vs. programming bias current.

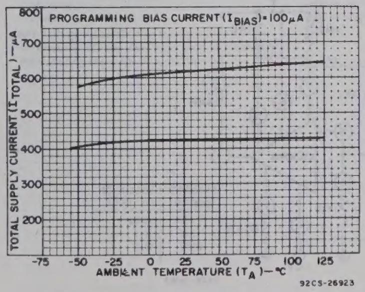


Fig. 14 – Total supply current vs. ambient temperature.

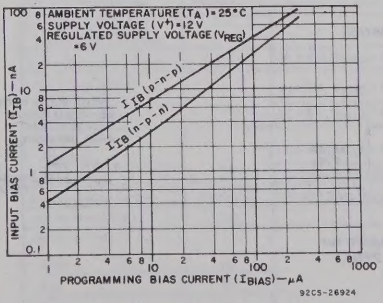


Fig. 15 – Input bias current vs. programming bias current.

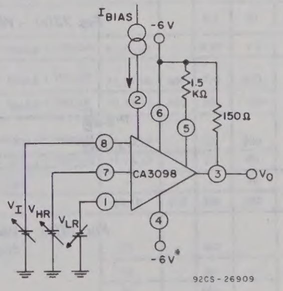


Fig. 16 – Input-offset voltage test circuit.

CA3098 Types

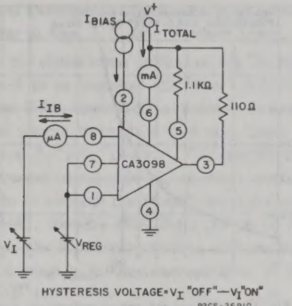


Fig. 17 — Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

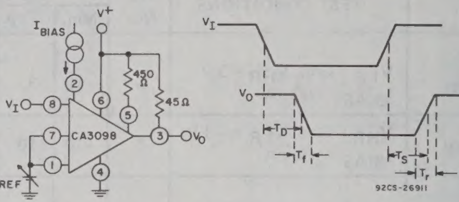


Fig. 18 — Switching time test circuit.

TYPICAL APPLICATIONS

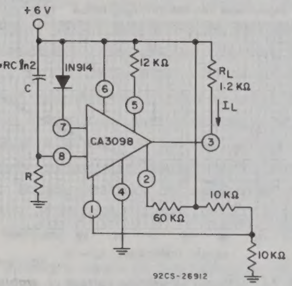


Fig. 19 — Time delay circuit: Terminal 3 "sinks" after τ seconds.

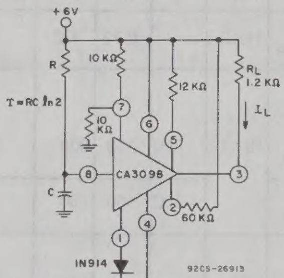


Fig. 20 — Time delay circuit: "sink" current interrupted after T seconds.

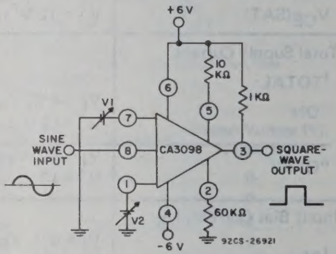
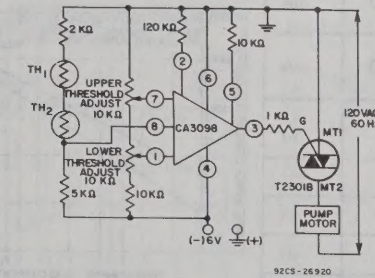


Fig. 21 — Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).



Notes (a) Motor pump is "ON" when water level rises above thermistor TH_2.

(b) Motor pump remains "ON" until water level falls below thermistor TH_1.

(c) Thermistors, operate in self-heating mode.

Fig. 22(a) — Water-level control.

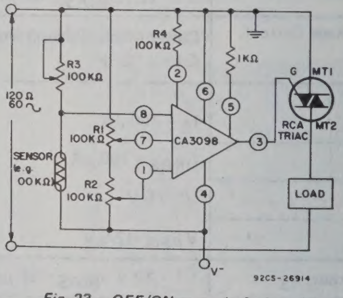


Fig. 23 — OFF/ON control of triac with programmable hysteresis.

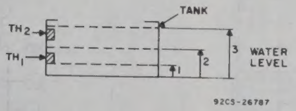


Fig. 22(b) — Water level diagram for circuit of Fig. 22(a).

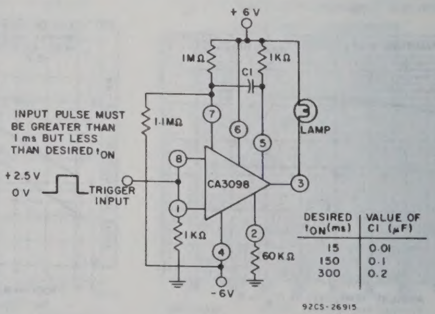


Fig. 24 — One-shot multivibrator.

Programmable Comparator - - With Memory

RCA-CA3099E Programmable Comparator is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3099E can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with a maximum operating voltage of ± 8 volts. It can directly control currents up to 150 mA. It operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3099E contains the following six (6) major circuit-function features (Figure 1):

1. **Differential amplifiers and summer;** the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. **Flip-flop;** the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. **Driver and output stages;** these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. **Programmable operating current;** the circuit incorporates a separate terminal to permit programming the desired quiescent operating current and performance parameters.
5. **Internal sources of reference voltage and programmable bias current;** an integral circuit supplies a temperature-compensated reference voltage ($V_b/2$) which is about 1/2 of the externally applied bias voltage (V_b). Additionally, integral circuitry can optionally be used to supply an uncompensated constant-current source of bias (I_{bias}).
6. **Voltage regulator;** provides optional on-chip voltage regulation when power for the CA3099E is provided by an unregulated supply.

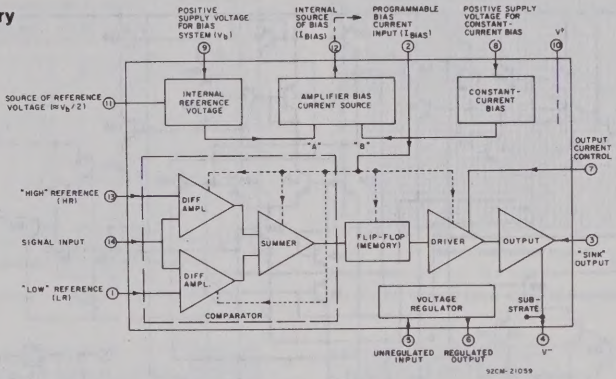


Fig.1—Block diagram of CA3099E programmable comparator. (See page 3 for general description of circuit operation.)

Features:

- Programmable operating current
- Micro-power standby dissipation
- Directly controls current up to 150 mA
- Low input on/off current of less than 1 nA for programmable bias current of 1 μA
- Built-in hysteresis: 10 mV max.
- Programmable hysteresis: 10 mV to V+
- Dual reference input
- High sensor range: 100 Ω to 100 MΩ
- Stable predictable switching levels
- Temperature-compensated reference voltage

Applications:

- Control of relays, heaters, LED's, lamps, photo-sensitive devices, thyristors, solenoids, etc.
- Signal reconditioning
- Phase and frequency modulators
- On/off motor switching
- Schmitt triggers, level detectors
- Time delays
- Overvoltage, overcurrent, overtemperature protection
- Battery-operated equipment
- Square and triangular-wave generators

Maximum Ratings, ***Absolute-Maximum Values at T_A = 25°C:***

Supply Voltage Between Terminals 10 and 4, 9 and 4, 8 and 4	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4.	16	V
Differential Input Voltage Between Terminals 14 and 1, and Terminals 13 and 14	10	V
Operating Voltage Range:		
Term. 14	0 V to V+	
Term. 13	2.0 V to V+	
Term. 1	0 V to V+ minus 2.0 V	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programming Bias Current (Term. 2)	1	mA
Output Current Control (Term. 7)	15	mA
Power Dissipation:		
Up to T_A = 55°C	750	mW
Above T_A = 55°C . . . . Derate Linearly at	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Termperature (During Soldering): At distance not less than 1/32 inch (0.79 mm) from seating plane for 10 s maximum	+265	°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C *(Unless otherwise indicated)*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C Unless Otherwise Indicated	FIG. No.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Reference Voltage	V_{REF}	Term. 9 = 12 V, Term.4 = Grd, Term.11 = Test	–	5.7	6	6.3	V
Reference Voltage Temperature Coefficient			–	–	100	–	μV/°C
Regulated Supply Voltage	V_{REG}	Term.5 1K to 12V, Term.4 = Grd, Term.6 10K to Grd	5	6	7.2	8	V
Regulated Supply Voltage Temperature Coefficient			5	–	2.9	–	mV/°C
Input Offset Voltage: "Low" Reference	V_{IO} (LR)	V_{LR} = Grd, V_{HR} = 3 V, I_{BIAS} = 100 μA	20, 6	−8	−3	2	mV
"High" Reference	V_{IO} (HR)	V_{HR} = Grd, V_{LR} = −3 V, I_{BIAS} = 100 μA	20, 7	−5	±1	5	
"Low" Reference Temp. Coefficient		−55°C to +125°C	20, 8	–	4.5	20	μV/°C
"High" Reference Temp. Coefficient		−55°C to +125°C	20, 9	–	±8.2	±20	
Min. Hysteresis Voltage	$V_{IO(HR-LR)}$	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21, 10	–	3	10	mV
Min. Hysteresis Voltage Temperature Coefficient		−55°C to +125°C	11	–	6.7	20	μV/°C
Output Saturation Voltage	V_{CE}(SAT)	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,12,13	–	0.72	1.2	V
Total Supply Current: I_{TOTAL} "ON"	I_{TOTAL}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	600	710	800	μA
I_{TOTAL} "OFF"		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	420	560	750	
Input Bias Current: $I_{B(p-n-p)}$	I_{IB}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	33	200	nA
$I_{B(n-p-n)}$		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	20	60	
Output Leakage Current	$I_{CE(OFF)}$	Current from Term.3 when Q46 is "OFF"	–	–	–	10	μA
Internal Bias Current	I_{IBC}		18,19	120	200	280	
Switching Times:							
Delay	t_d	I_C = 100 μA I_{BIAS} = 100 μA V^+ = 5 V V_{REG} = 2.5 V	22	–	600	–	ns
Fall	t_f		22	–	50	–	
Rise	t_r		22	–	500	–	
Storage	t_s		22	–	4.5	–	μS

CA3099E

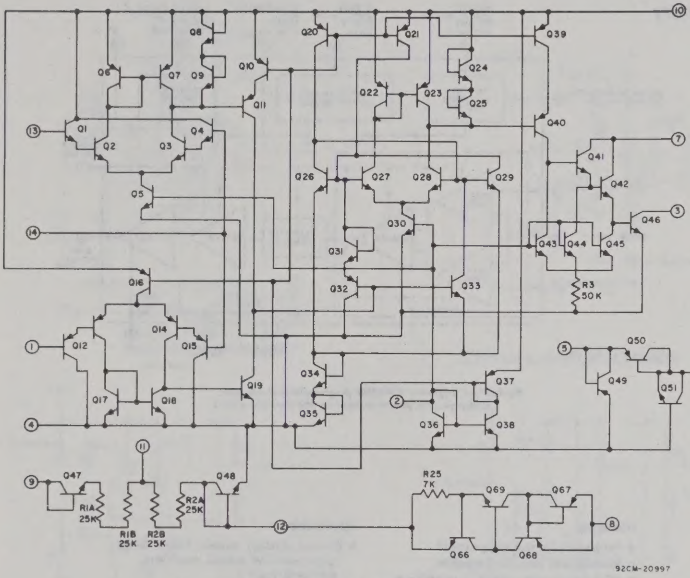


Fig.2—Schematic diagram of CA3099E.

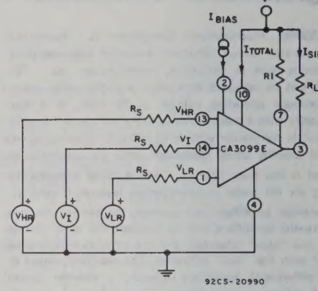


Fig. 3 – Functional diagram.

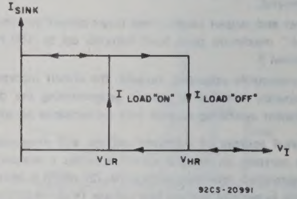


Fig. 4 – Logic diagram.

General Description of Circuit Operation (Refer to Fig.1)

When the signal-input voltage of the CA3099E is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3099E comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2. As an alternative to externally supplied bias current, the CA3099E contains an internal source of regulated bias current accessible at terminal 12. This internal source of bias current is developed by two alternative methods; in the first method, bias voltage (V_b) applied at terminal 9 develops a source of temperature-compensated reference voltage ($\approx V_b/2$) at terminal 11 and additionally supplies a source of bias current at terminal 12 via line "A". Alternately, when a positive supply voltage is applied at terminal 8, a source of constant-current biasing is provided at terminal 12 via line "B".

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 7. The CA3099E contains an on-chip voltage regulator which may optionally be used to regulate the voltages and bias currents (exclusive of the load current at terminal 3) needed for the operation of the IC.

Fig. 2 is the schematic diagram of the CA3099E. Figs. 3 and 4 are, respectively, functional and logic diagrams of CA3099E operation.

TYPICAL CHARACTERISTIC CURVES

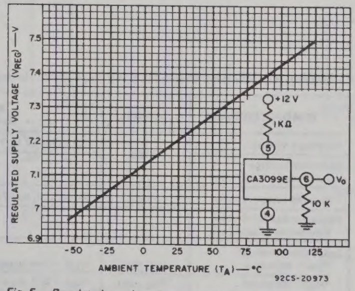


Fig. 5 – Regulated supply voltage vs. ambient temperature.

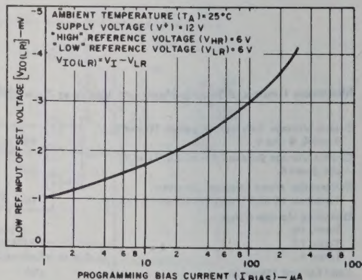


Fig. 6 – Input-offset voltage ("low" reference) vs. programming bias current.

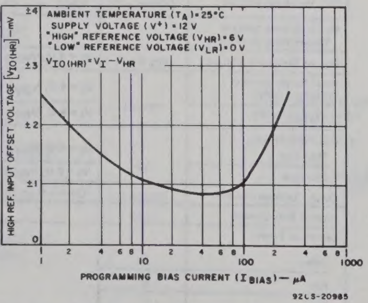


Fig. 7 – Input-offset voltage ("high" reference) vs. programming bias current.

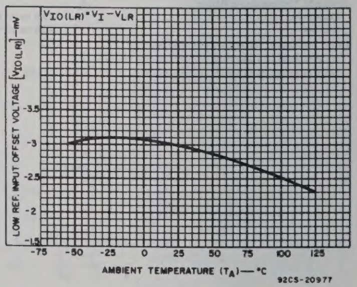


Fig. 8 – Input-offset voltage ("low" reference) vs. ambient temperature.

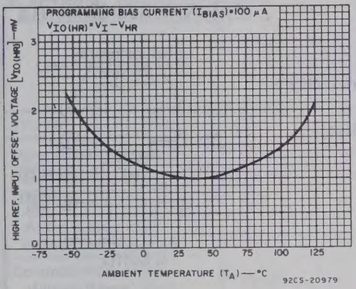


Fig. 9 – Input-offset voltage ("high" reference) vs. ambient temperature.

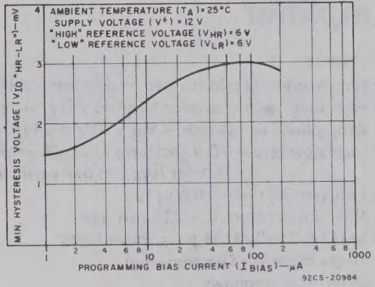


Fig. 10 – Min. hysteresis voltage vs. programming bias current.

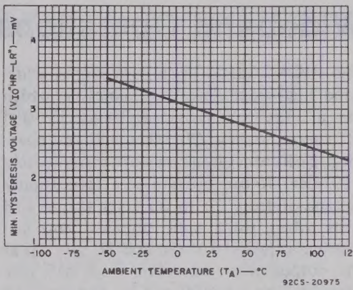


Fig. 11 – Min. hysteresis voltage vs. ambient temperature.

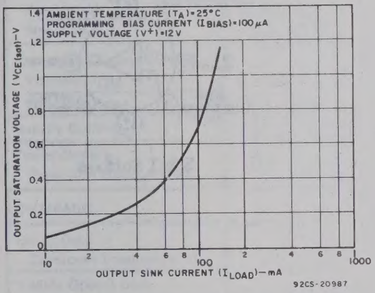


Fig. 12 – Output saturation voltage vs. output sink current.

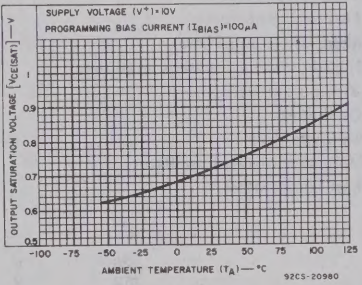


Fig. 13 – Output saturation voltage vs. ambient temperature.

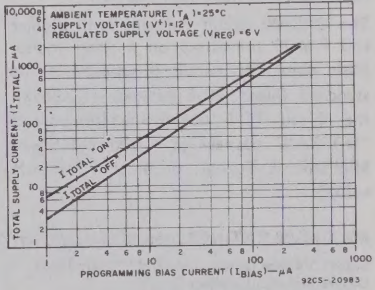


Fig. 14 – Total supply current vs. programming bias current.

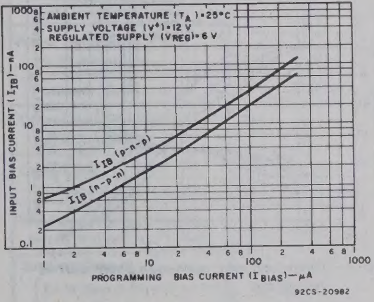


Fig. 15 · Input bias current vs. programming bias current.

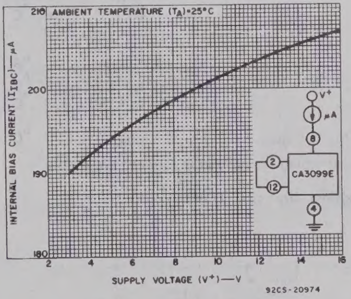


Fig. 16 – Internal bias current vs. supply voltage.

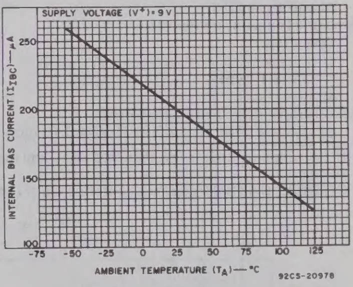


Fig. 17 – Internal bias current vs. ambient temperature.

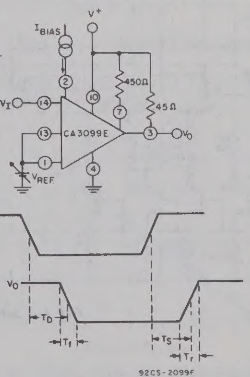


Fig. 20 - Switching time test circuit.

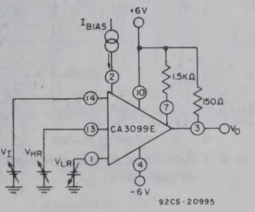
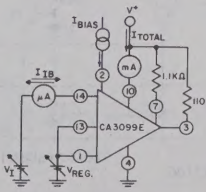


Fig. 18 – Input-offset voltage test circuit.



HYSTERESIS VOLTAGE = V_I "OFF" — V_I "ON"

92CS-20994

Fig. 19 – Min. hysteresis voltage, total supply current, and input bias current test circuit.

For application information, see Data Bulletin File No. 620.

CA3100 Types

Wideband Operational Amplifier

The RCA-CA3100 is a large-signal wideband, high-speed operational amplifier which has a unity gain crossover frequency (f_T) of approximately 38 MHz and an open-loop, 3 dB corner frequency of approximately 110 kHz. It can operate at a total supply voltage of from 14 to 36 volts (±7 to ±18 volts when using split supplies) and can provide at least 18 V p-p and 30 mA p-p at the output when operating from ±15 volt supplies. The CA3100 can be compensated with a single external capacitor and has dc offset adjust terminals for those applications requiring offset null. (See Fig. 15).

The CA3100 circuit contains both bipolar and P-MOS transistors on a single monolithic chip. This circuit is supplied in the standard 8-lead TO-5 package (T suffix), the 8-lead TO-5 dual-in-line formed-lead "DIL-CAN" package (S suffix), the 8-lead Mini-DIP (E Suffix), or in chip form (H suffix).

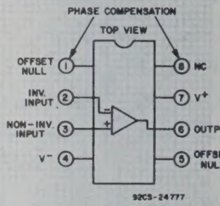
Features:

- **High open-loop gain at video frequencies — 42 dB typ. at 1 MHz**
- **High unity-gain crossover frequency (f_T) — 38 MHz typ.**
- **Wide power bandwidth — V_O = 18 V p-p typ. at 1.2 MHz**
- **High slew rate — 70 V/μs (typ.) in 20 dB amplifier**
  25 V/μs (typ.) in unity-gain amplifier
- **Fast settling time — 0.6 μs typ.**
- **High output current — ±15 mA min.**
- **LM118, 748/LM101 pin compatibility**
- **Single capacitor compensation**
- **Offset null terminals**

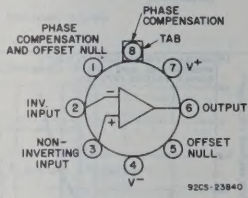
Applications:

- **Video amplifiers**
- **Fast peak detectors**
- **Meter-driver amplifiers**
- **High-frequency feedback amplifiers**
- **Video pre-drivers**
- **Oscillators**
- **Multivibrators**
- **Voltage-controlled oscillator**
- **Fast comparators**

TERMINAL ASSIGNMENTS



E Suffix



S & T Suffixes

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Supply Voltage (between V+ and V⁻ terminals)	36	V
Differential Input Voltage	±12	V
Input Voltage to Ground*	±15	V
Offset Terminal to V⁻ Terminal Voltage	±0.5	V
Output Current	50	mA•
Device Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C	6.67	mW/°C
Ambient Temperature Range:		
Operating:		
E Type	−40 to +85	°C
S and T Types	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

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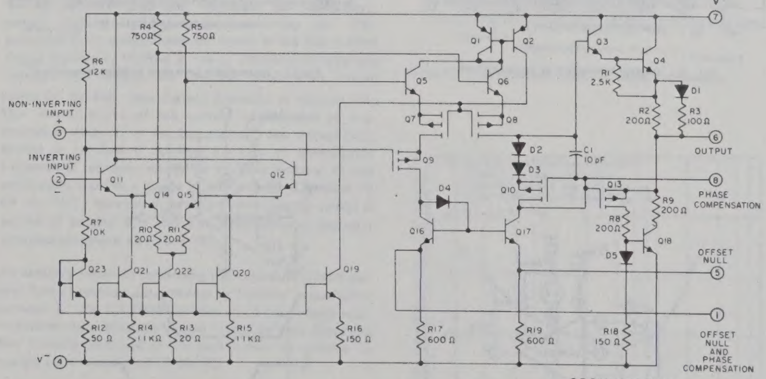
* If the supply voltage is less than ±15 volts, the maximum input voltage to ground is equal to the supply voltage.

• CA3100S, CA3100T does not contain circuitry to protect against short circuits in the output.



92CM-21655R1

Fig. 1 – Schematic diagram for CA3100.

TYPICAL CHARACTERISTIC CURVES

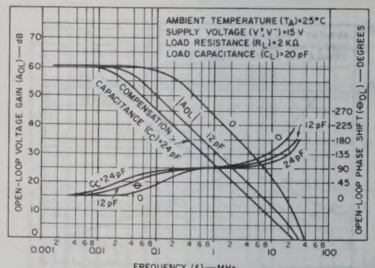


Fig. 2 – Open-loop gain, open-loop phase shift vs. frequency.

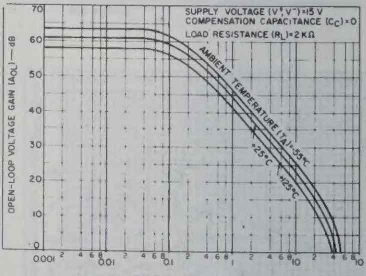


Fig. 3 – Open-loop gain vs. frequency and temperature.

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$:*

CHARACTERISTICS	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15 V UNLESS OTHERWISE SPECIFIED	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC					
Input Offset Voltage, V_{IO}	$V_O = 0 \pm 0.1$ V	–	±1	±5	mV
Input Bias Current, I_{IB}	$V_O = 0 \pm 1$ V	–	0.7	2	μA
Input Offset Current, I_{IO}		–	±0.05	±0.4	μA
Low-Frequency Open-Loop Voltage Gain, A_{OL} •	$V_O = \pm 1$ V Peak, F = 1 kHz	56	61	–	dB
Common-Mode Input Voltage Range, V_{ICR}	CMRR $\geq$ 76 dB	±12	+14 −13	–	V
Common-Mode Rejection Ratio, CMRR	V_I Common Mode = ±12 V	76	90	–	dB
Maximum Output Voltage: Positive, V_{OM}^+	Differential Input Voltage = 0 ± 0.1 V	+9	+11	–	V
Negative, V_{OM}^-	R_L = 2 KΩ	−9	−11	–	
Maximum Output Current: Positive, I_{OM}^+	Differential Input Voltage = 0 ± 0.1 V	+15	+30	–	mA
Negative, I_{OM}^-	R_L = 250 Ω	−15	−30	–	
Supply Current, I^+	$V_O = 0 \pm 0.1$ V, $R_L \geq 10$ KΩ	–	8.5	10.5	mA
Power-Supply Rejection Ratio, PSRR	$\Delta V^+ = \pm 1$ V, $\Delta V^- = \pm 1$ V	60	70	–	dB
DYNAMIC					
Unity-Gain Crossover Frequency, f_T	$C_C = 0$, $V_O = 0.3$ V (P-P)	–	38	–	MHz
1-MHz Open-Loop Voltage Gain, A_{OL}	f = 1 MHz, $C_C = 0$, $V_O = 10$ V (P-P)	36	42	–	dB
Slew Rate, SR: 20-dB Amplifier	$A_V = 10$, $C_C = 0$, $V_I = 1$ V (Pulse)	50	70	–	V/μs
Follower Mode	$A_V = 1$, $C_C = 10$ pF, $V_I = 10$ V (Pulse)	–	25	–	
Power Bandwidth, PBW▲: 20-dB Amplifier	$A_V = 10$, $C_C = 0$, $V_O = 18$ V (P-P)	0.8	1.2	–	MHz
Follower Mode	$A_V = 1$, $C_C = 10$ pF, $V_O = 18$ V (P-P)	–	0.4	–	
Open-Loop Differential Input Impedance, Z_I	F = 1 MHz	–	30	–	KΩ
Open-Loop Output Impedance, Z_O	F = 1 MHz	–	110	–	Ω
Wideband Noise Voltage Referred to Input, e_N(Total)	BW = 1 MHz, R_S = 1 KΩ	–	8	–	μV_{RMS}
Settling Time, t_s [To Within ± 50 mV of 9 V Output Swing]	R_L = 2 KΩ, C_L = 20 pF	–	0.6	–	μs

▲ Power Bandwidth $= \dfrac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$

• Low-frequency dynamic characteristic

TYPICAL CHARACTERISTIC CURVES (Cont'd)

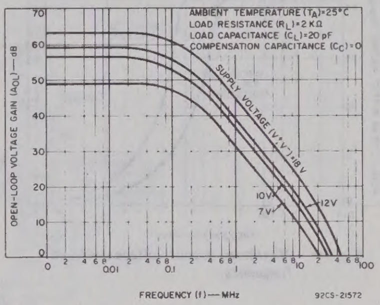


Fig. 4 – Open-loop gain vs. frequency and supply voltage.

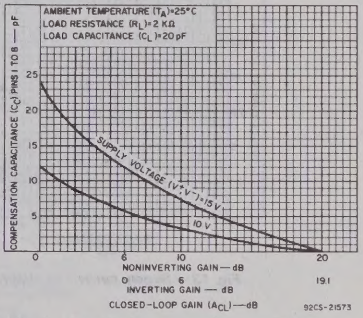


Fig. 5 – Required compensation capacitance vs. closed-loop gain.

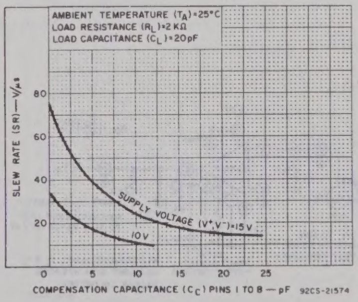


Fig. 6 – Slew rate vs. compensation capacitance.

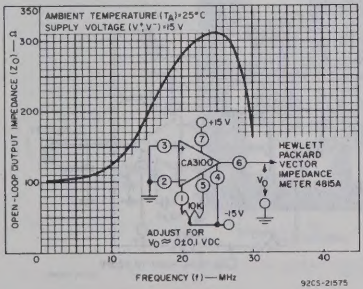


Fig. 7 – Typical open-loop output impedance vs. frequency.

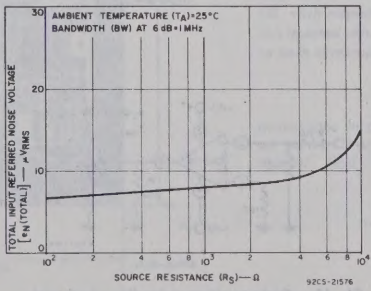


Fig. 8 – Wideband input noise voltage vs. source resistance.

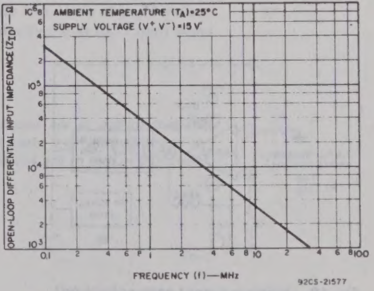


Fig. 9 – Typical open-loop differential input impedance vs. frequency.

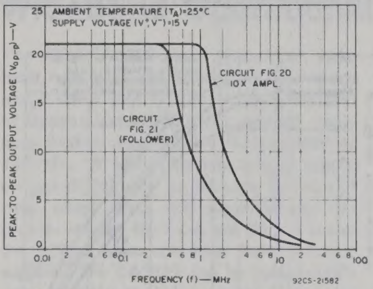


Fig. 10 – Maximum output voltage swing vs. frequency.

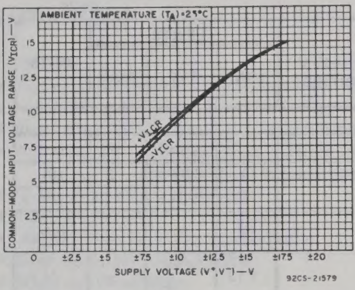


Fig. 11 – Common-mode input voltage range vs. supply voltage.

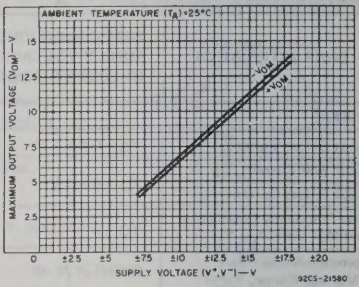


Fig. 12 – Maximum output voltage vs. supply voltage.

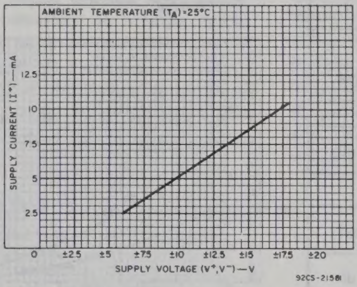


Fig. 13 – Supply current vs. supply voltage.

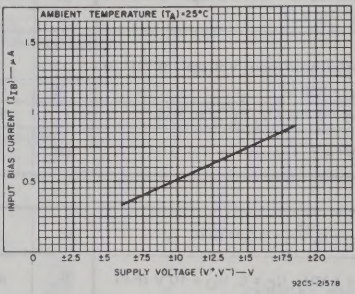


Fig. 14 – Input bias current vs. supply voltage.

TEST CIRCUITS

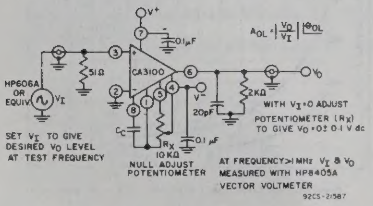

V$^+$
0.1μF
A$_{OL}$ = |V$_O$/V$_I$| |Θ$_{OL}$
HP606A OR EQUIV
V$_I$
51Ω
CA3100
V$_O$
V$^-$
2KΩ
20pF
0.1 μF
C$_C$
R$_X$
10 KΩ NULL ADJUST POTENTIOMETER
WITH V$_I$=0 ADJUST POTENTIOMETER (R$_X$) TO GIVE V$_O$=0±0.1 V dc
SET V$_I$ TO GIVE DESIRED V$_O$ LEVEL AT TEST FREQUENCY
AT FREQUENCY>1 MHz V$_I$ & V$_O$ MEASURED WITH HP8405A VECTOR VOLTMETER
92CS-21587

Fig. 15 – Open-loop voltage gain test circuit.

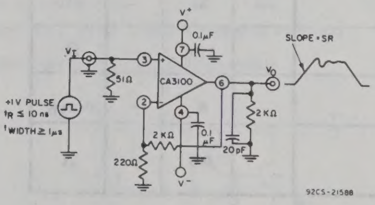


Fig. 16 – Slew rate in 10X amplifier test circuit.

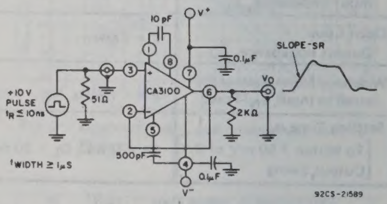


Fig. 17 – Follower slew rate test circuit.

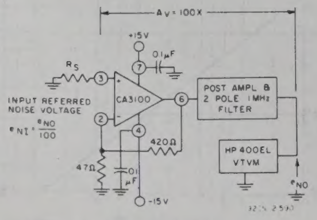


Fig. 18 – Wideband input noise voltage test circuit.

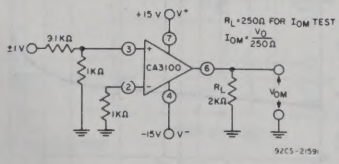


Fig. 19 – Output voltage swing (V_{OM}), output current swing (I_{OM}) test circuit.

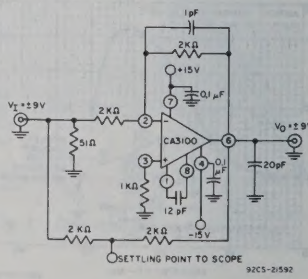


Fig. 20 – Settling time test circuit.

TYPICAL APPLICATIONS

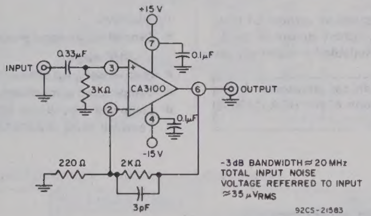


Fig. 21 – 20 dB video amplifier.

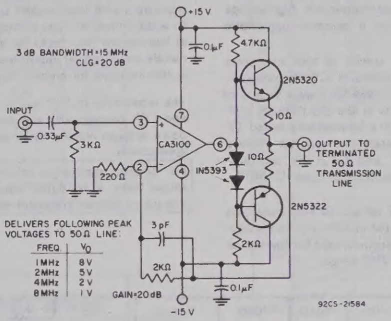


Fig. 22 – 20 dB video line driver.

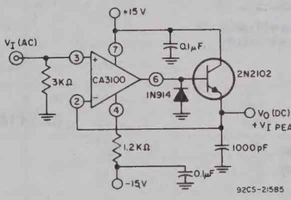


Fig. 23 – Fast positive peak detector.

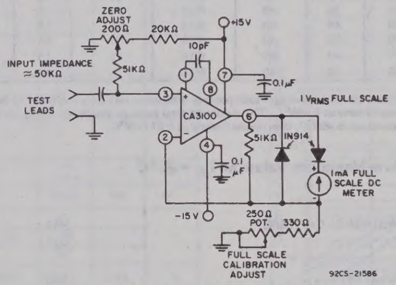
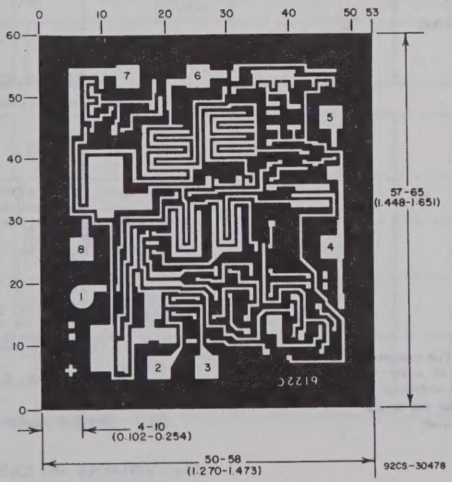


Fig. 24 – 1 MHz meter-driver amplifier.

Chip Dimensions and Pad Layout



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3100H Chip

CA3118, CA3146, CA3183 Types

High-Voltage Transistor Arrays

RCA-CA3118AT, CA3118T, CA3146AE, CA3146E, CA3183AE, and CA3183E are general-purpose high-voltage silicon n-p-n transistor arrays on a common monolithic substrate.

Types CA3118AT and CA3118T consist of four transistors with two of the transistors connected in a Darlington configuration. These types are well suited for a wide variety of applications in low-power systems in the DC through VHF range. Both types are supplied in a hermetically sealed 12-lead TO-5 type package and operate over the full military temperature range. (CA3118AT and CA3118T are high-voltage versions of the popular predecessor type CA3018.

Types CA3146AE and CA3146E consist of five transistors with two of the transistors connected to form a differentially-connected pair. These types are recommended for low-power applications in the DC through VHF range.

Types CA3183AE and CA3183E consist of five high-current transistors with independent connections for each transistor. In addition two of these transistors (Q1 and Q2) are matched at low-current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design.

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated Circuit Transistor Array."

TYPE	P_T● max. mW	I_C max. mA	V_{CEO} max. V	V_{CBO} max. V	V_{CE} sat. at 10 mA typ. V	h_{FE} at 1mA, & V_{CE}=5V typ.	V_{IO} Diff. Pair at 1mA max. mV	I_{IO} Diff. Pair at 1mA max. µA	T_A Range (Operating) °C
VALUES APPLY FOR EACH TRANSISTOR									
CA3118AT	300	50	40	50	0.33	95	±5	2	−55 – +125
CA3118T	300	50	30	40	0.33	95	±5	2	
CA3146AE	300	50	40	50	0.33	95	±5	2	
CA3146E	300	50	30	40	0.33	95	±5	2	
CA3183AE	500	75	40	50	0.16	75	±5	2.5	
CA3183E	500	75	30	40	0.16	75	±5	2.5	

● Caution on Total Package Power Dissipation: The maximum total package dissipation rating for the CA3118 Series circuits is 450 mW at temperatures up to +85°C, then derate linearly at 5 mW°C. The maximum total package dissipation rating for the CA3146 and CA3183 Series circuits is 750 mW at temperatures up to +55°C, then derate linearly at 6.67 mW°C.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor –		
CA3118AT, CA3118T, CA3146AE, CA3146E	300	mW
CA3183AE, CA3183E	500	mW
Total package –		
Up to 85°C (CA3118AT, CA3118T)	450	mW
Up to 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	750	mW
Above 85°C (CA3118AT, CA3118T)	derate linearly 5	mW/°C
Above 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating –	−55 to +125	°C
Storage (all types)	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO}):		
CA3118AT, CA3146AE, CA3183AE	40	V
CA3118T, CA3146E, CA3183E	30	V
Collector-to-Base Voltage (V_{CBO}):		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Collector-to-Substrate Voltage (V_{CIO}): ■		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Emitter-to-Base Voltage (V_{EBO}) all types	5	V
Collector Current –		
CA3118AT, CA3118T, CA3146AE, CA3146E	50	mA
CA3183AE, CA3183E	75	mA
Base Current (I_B) – CA3183AE, CA3183E	20	mA

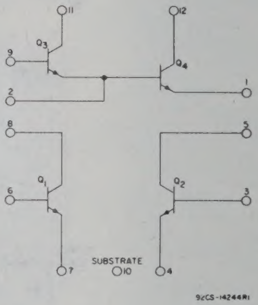
■ The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

Features

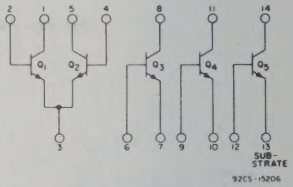
- Matched general-purpose transistors
- V_{BE} matched ±5mV max.
- Operation from DC to 120 MHz (CA3118AT, T; CA3146AE, E)
- Low-noise figure: 3.2dB typ. at 1kHz (CA3118AT, T; CA3146AE, E)
- High I_C: 75mA max. (CA3183AE, E)

Applications

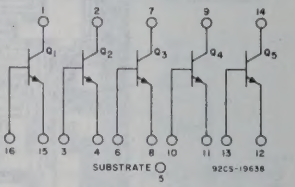
- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- Lamp and relay drivers (CA3183AE, E)
- Thyristor firing (CA3183AE, E)



CA3118AT, CA3118T



CA3146AE, CA3146E



CA3183AE, CA3183E

Fig. 1 – Schematic diagrams of high-voltage arrays.

The CA3146AE and CA3146E are supplied in the 14-lead dual-in-line plastic package; the CA3183AE and CA3183E are supplied in the 16-lead dual-in-line plastic package.

CA3118, CA3146, CA3183 Types

COMPARISON OF RELATED PREDECESSOR TYPE WITH TYPES IN THIS DATA BULLETIN

	DATA FILE NO.	V_{CEO} min.	V_{CBO} min.	$V_{CE\ sat.}$ typ. V	V_{BE} typ. V	I_C max. mA	C_{CB} typ. pF	C_{CI} typ. pF	C_{EB} typ. pF
				I_C=10 mA	I_C=1 mA				
CA3018	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3018A	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3118AT		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3118T		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=10mA	I_C=1 mA				
CA3046	341	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3146AE		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3146E		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=50mA	I_C=10 mA				
CA3083	481	15	20	0.4	0.74	100	–	–	–
CA3183AE		40	50	1.7	0.75	75	–	–	–
CA3183E		30	40	1.7	0.75	75	–	–	–

STATIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	LIMITS CA3118AT, CA3146AE Min.	Typ.	Max.	LIMITS CA3118T, CA3146E Min.	Typ.	Max.	UNITS
For Each Transistor:									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	50	72	–	40	72	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	40	56	–	30	56	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10μA, I_B = 0 I_E = 0	50	72	–	40	72	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0	5	7	–	5	7	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	see curve	5	–	see curve	5	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	0.002	100	–	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=5V, I_C=10 mA	–	85	–	–	85	–	–
		V_{CE}=5V, I_C=1 mA	30	100	–	30	100	–	
		V_{CE}=5V, I_C=10μA	–	90	–	–	90	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 1 mA	0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 10mA, I_B = 1 mA	–	0.33	–	–	0.33	–	V
For transistors Q3 and Q4 (Darlington Configeration):									
Collector-Cutoff Current (CA3118AT and CA3118T only)	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	5	–	–	–	μA
DC Forward-Current Transfer Ratio (CA3118AT and CA3118T only)	h_{FE}	V_{CE} = 5V, I_C = 1 mA	1500	9000	–	1500	9000	–	–
Base-to-Emitter (Q3 to Q4)	V_{BE}	V_{CE}=5V, I_E = 10mA	–	1.46	–	–	1.46	–	V
		V_{CE}=5V, I_E = 1mA	–	1.32	–	–	1.32	–	
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\|\frac{\Delta V_{BE}}{\Delta T}\right\|$	V_{CE} = 5V, I_E = 1 mA	–	4.4	–	–	4.4	–	mV/°C
For transistors Q1 and Q2 (AS a Differential Amplifier):									
Magnitude of Input Offset Voltage $\|V_{BE1} = V_{BE2}\|$	$\|V_{IO}\|$	V_{CE} = 5V, I_E = 1 mA	–	0.48	5	–	0.48	5	mV
Magnitude of h_{FE} Ratio (CA3118AT and CA3118T only)		V_{CE} = 5V, I_{C1} = I_{C2} = 1mA	0.9	1.0	1.1	0.9	1.0	1.1	–
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\|\frac{\Delta V_{BE}}{\Delta T}\right\|$	V_{CE} = 5V, I_E = 1mA	–	1.9	–	–	1.9	–	mV/°C
Magnitude of V_{IO} (V_{BE1} - V_{BE2}) Temperature Coefficient	$\left\|\frac{\Delta V_{IO}}{\Delta T}\right\|$	V_{CE} = 5V, I_{C1} = I_{C2} = 1 mA	–	1.1	–	–	1.1	–	μV/°C
Magnitude of Input Offset Current $\|I_{IO_1} - I_{IO_2}\|$ (CA3146AE and CA3146E only)	I_{IO}	V_{CE} = 5V, I_{C_1} = I_{C_2} = 1 mA	–	0.3	2	–	0.3	2	μA

TYPICAL STATIC CHARACTERISTICS CURVES– CA3118 and CA3146 SERIES (cont'd Fig.2 to 12)

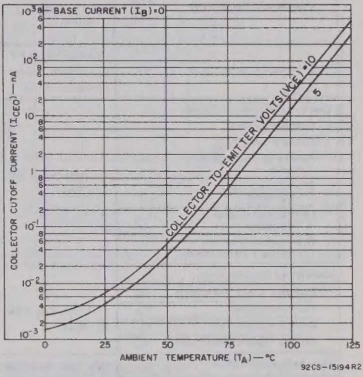


Fig. 2 – I_{CEO} vs. T_A for any transistor.

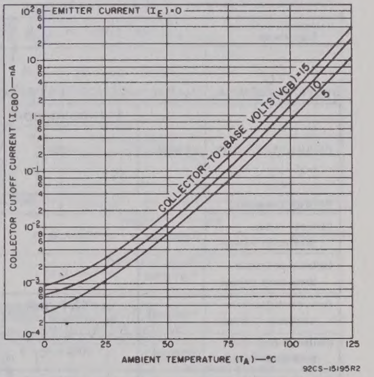


Fig. 3 – I_{CBO} vs. T_A for any transistor.

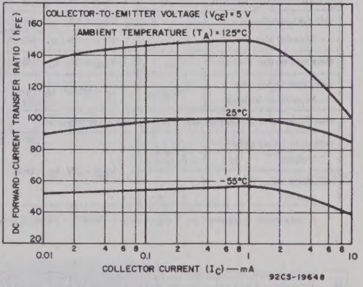


Fig. 4 – h_{FE} vs. I_C for any transistor.

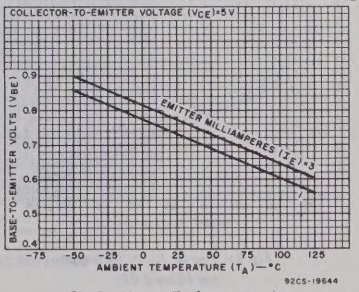


Fig. 5 – V_{BE} vs. T_A for any transistor.

CA3118, CA3146, CA3183 Types

DYNAMIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$	CA3118AT CA3146AE			CA3118T CA3146E			UNITS
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100µA, Source resistance = 1 kΩ	–	3.25	–	–	3.25	–	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:									
Foward-Current Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	–	100	–	–	100	–	–
Short-Circuit Input Impedance	h_{ie}		–	2.7	–	–	3.5	–	kΩ
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	µmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}		–	1.8×10^{-4}	–	–	1.8×10^{-4}	–	–
Admittance Characteristics:									
Foward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	–	31-j1.5	–	–	31-j1.5	–	mmho
Input Admittance	Y_{ie}		–	0.35+j0.04	–	–	0.3+j0.04	–	mmho
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho
Reverse Transfer Admittance	Y_{re}			See curve			See curve		mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	300	500	–	300	500	–	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	–	0.70	–	–	0.70	–	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	–	0.37	–	–	0.37	–	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	–	2.2	–	–	2.2	–	pF

STATIC ELECTRICAL CHARACTERISTICS – CA3183 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$	LIMITS						UNITS
			CA3183AE			CA3183E			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each Transistor:									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100µA, I_E=0	50	–	–	40	–	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	40	–	–	30	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI}=100µA, I_B=0, I_E = 0	50	–	–	40	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500µA, I_C = 0	5	–	–	5	–	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	10	–	–	10	µA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	1	–	–	1	µA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V, I_C = 10mA	40	–	–	40	–	–	–
		V_{CE} = 5V, I_C = 50mA	40	–	–	40	–	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	*V_{CEsat}	I_C = 50mA, I_B = 5mA	–	1.7	3.0	–	1.7	3.0	V
For Transistors Q1 and Q2 (As a Differential Amplifier):									
Absolute Input Offset Voltage	$\lvert V_{IO} \rvert$	V_{CE} = 3V, I_C = 1mA	–	0.47	5	–	0.47	5	mV
Absolute Input Offset Current	$\lvert I_{IO} \rvert$		–	0.78	2.5	–	0.78	2.5	µA

* A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

TYPICAL STATIC CHARACTERISTICS CURVES– CA3118 and CA3146 SERIES (cont'd Fig.2 to 12)

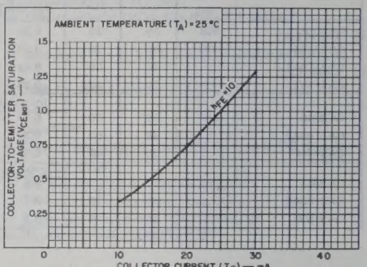


Fig. 6 – V_{CE} sat vs. I_C for any transistor.

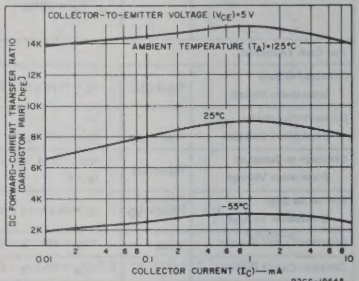


Fig. 7 – h_{FE} vs. I_C for Darlington pair (Q3 and Q4) for types CA3118AT and CA3118T.

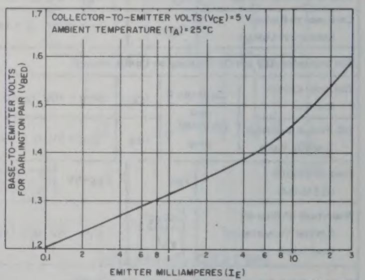


Fig. 8 – V_{BE} vs. I_E for Darlington pair (Q3 and Q4).

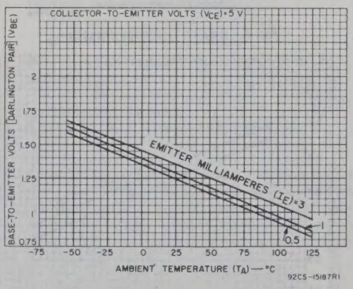


Fig. 9 – V_{BE} vs. T_A for Darlington pair (Q3 and Q4).

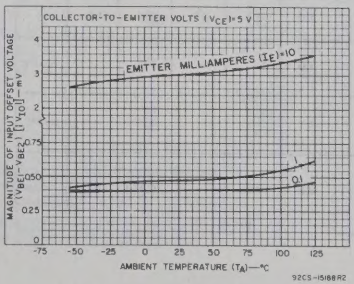


Fig. 10 – V_{IO} vs. T_A for Q1 and Q2.

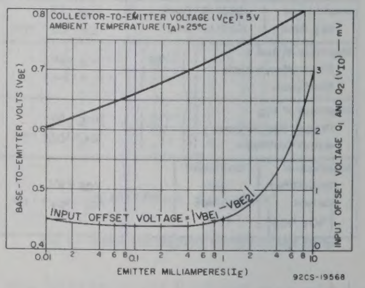


Fig. 11 – V_{BE} and V_{IO} vs. I_E for Q1 and Q2.

TYPICAL STATIC CHARACTERISTICS CURVES— CA3118 and CA3146 SERIES (Fig.2 to 12)

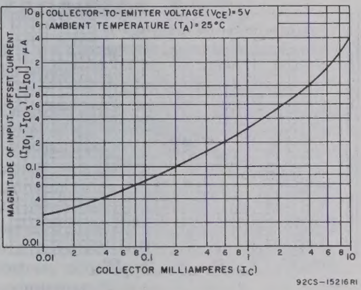


Fig. 12 – I_{IO} vs. I_C (Q1 and Q2) for types CA3146AE and CA3146E.

TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR)—CA3118,CA3146 SERIES (Fig. 13 to 22)

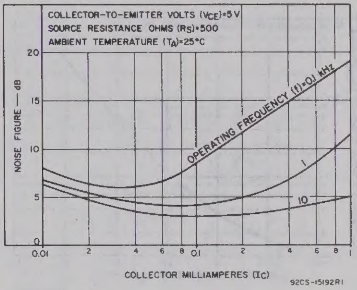


Fig. 13 – NF vs. I_C @ R_S = 500Ω.

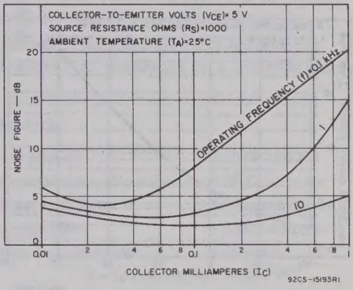


Fig. 14 – NF vs. I_C @ R_S = 1kΩ.

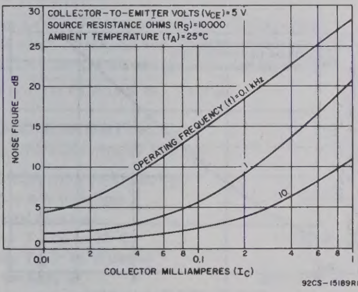


Fig. 15 – NF vs. I_C @ R_S = 10kΩ.

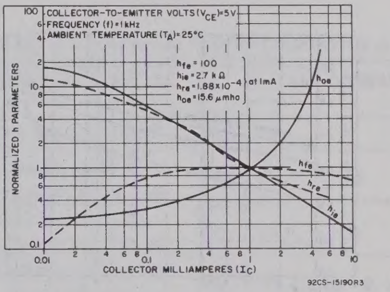


Fig. 16 – h_{fe}, h_{ie}, h_{oe}, h_{re} vs. I_C.

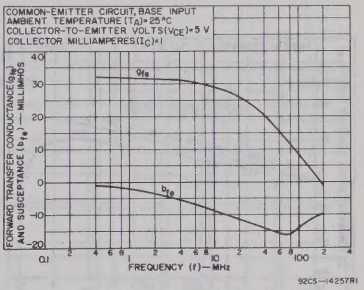


Fig. 17 – y_{fe} vs. f.

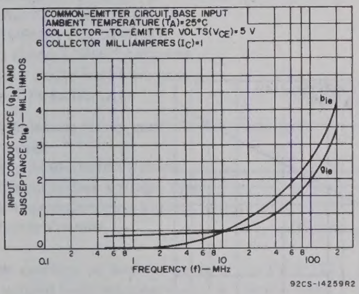


Fig. 18 – y_{ie} vs. f.

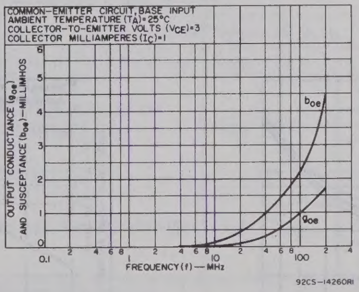


Fig. 19 – y_{oe} vs. f.

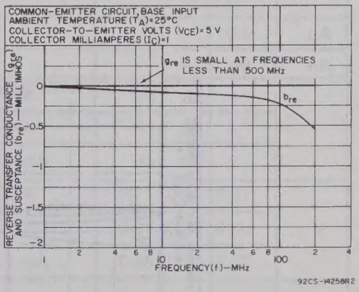


Fig. 20 – y_{re} vs. f.

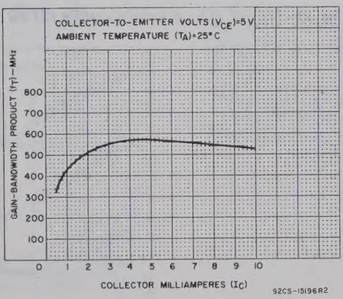


Fig. 21 – f_T vs. I_C.

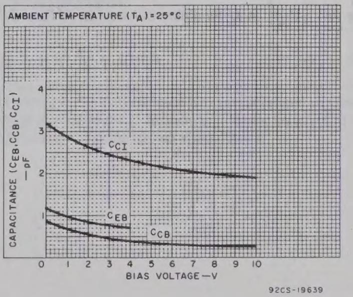


Fig. 22 – C_{EB}, C_{CB}, C_{CI} vs. bias voltage

TYPICAL STATIC CHARACTERISTICS CURVES—CA3183 SERIES
(Fig. 23 to 30)

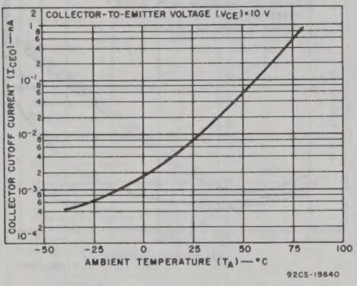


Fig. 23 – I_{CEO} vs. T_A for any transistor.

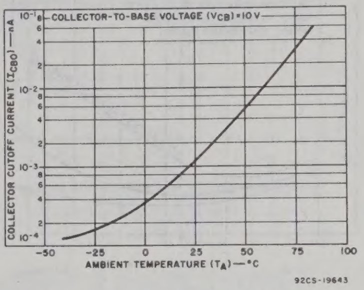


Fig. 24 – I_{CBO} vs. T_A for any transistor.

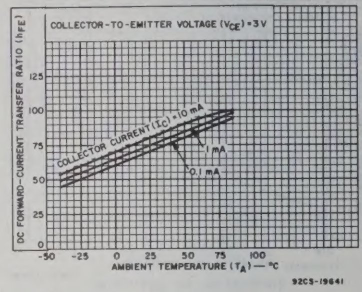


Fig. 25 – h_{FE} vs. T_A for any transistor.

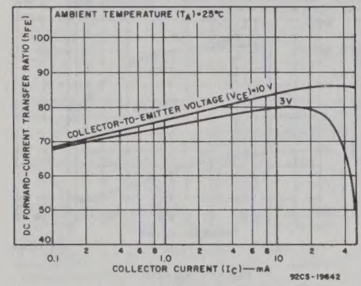


Fig. 26 – h_{FE} vs. I_C for any transistor.

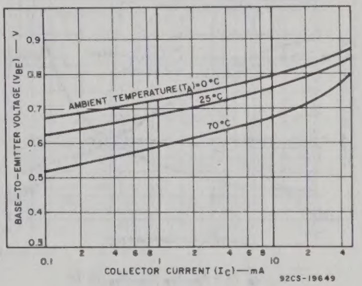


Fig. 27 – V_{BE} vs. I_C for any transistor.

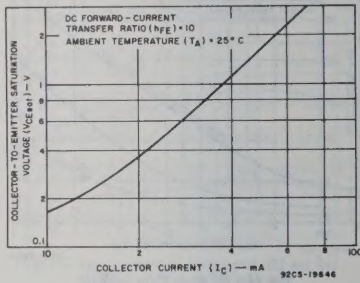


Fig. 28 – $V_{CE\ sat}$ vs. I_C for any transistor.

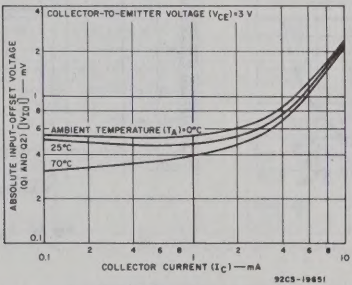


Fig. 29 – $|V_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2!.

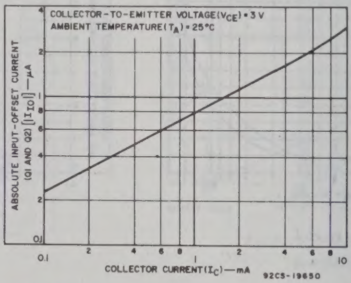


Fig. 30 – $|I_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

RCA-CA3127E* consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127E useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127E provides close electrical and thermal matching of the five transistors.

The CA3127E is supplied in a 16-lead dual-in-line plastic package and operates over the full military temperature range of −55 to +125°C.

* Formerly RCA Dev. No. TA6206.

MAXIMUM RATINGS,

Absolute-Maximum Values:

POWER DISSIPATION, P_D:
Any one transistor . . . . 85 mW
Total Package:
For T_A up to 75°C . . . . 425 mW
For $T_A > 75$°C Derate
Linearly at . . . . 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating . . . . −55 to +125°C
Storage . . . . −65 to +125°C
LEAD TEMPERATURE
(DURING SOLDERING):
At distance 1/16 ± 1/32 inch
(1.59 ± 0.79 mm) from case
for 10 seconds max. . . . . . . +265°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO} . . . 15 V
Collector-to-Base Voltage, V_{CBO} . . . 20 V
Collector-to-Substrate Voltage, V_{CIO}* . . 20 V
Collector Current, I_C . . . . . . 20 mA

*The collector of each transistor of the CA3127E is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

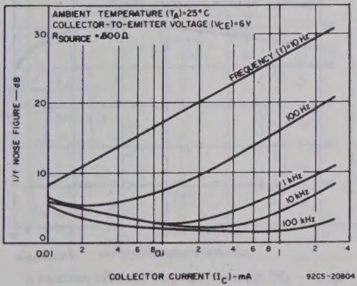


Fig. 2 — 1/f noise figure as a function of collector current at R_{SOURCE} = 500 Ω.

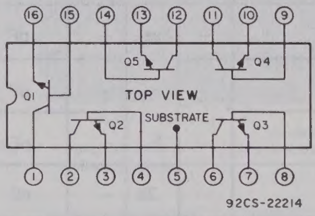


Fig. 1 — Schematic diagram of CA3127E.

Features:

- Gain-Bandwidth Product (f_T) > 1 GHz
- Power Gain = 30 dB (typ.) at 100 MHz
- Noise Figure = 3.5 dB (typ.) at 100 MHz
- Five independent transistors on a common substrate

Applications:

- VHF amplifiers
- Multifunction combinations—RF/mixer/oscillator
- Sense amplifiers
- Synchronous detectors
- VHF mixers
- IF Converter
- IF amplifiers
- Synthesizers
- Cascade amplifiers

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	TEST CONDITIONS		LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$		20	32	–	V
Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$		15	24	–	V
Collector-to-Substrate Breakdown Voltage	$I_{C1} = 10\ \mu A$, $I_B = 0$, $I_E = 0$		20	60	–	V
Emitter-to-Base Breakdown Voltage*	$I_E = 10\ \mu A$, $I_C = 0$		4	5.7	–	V
Collector-Cutoff-Current	$V_{CE} = 10$ V, $I_B = 0$		–	–	0.5	μA
Collector-Cutoff-Current	$V_{CB} = 10$ V, $I_E = 0$		–	–	40	nA
DC Forward-Current Transfer Ratio	$V_{CE} = 6$ V	$I_C = 5$ mA	35	88	–	
		$I_C = 1$ mA	40	90	–	
		$I_C = 0.1$ mA	35	85	–	
Base-to-Emitter Voltage	$V_{CE} = 6$ V	$I_C = 5$ mA	0.71	0.81	0.91	V
		$I_C = 1$ mA	0.66	0.76	0.86	
		$I_C = 0.1$ mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	$V_{CE} = 6$ V, $I_C = 1$ mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

CA3127E

DYNAMIC CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTICS	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
I/F Noise Figure	f = 100 kHz, $R_S = 500\ \Omega$, $I_C = 1$ mA	–	1.8	–	dB
Gain-Bandwidth Product	$V_{CE} = 6$ V, $I_C = 5$ mA	–	1.15	–	GHz
Collector-to-Base Capacitance	$V_{CB} = 6$ V, f = 1 MHz	–	See	–	pF
Collector-to-Substrate Capacitance	$V_{CI} = 6$ V, f = 1 MHz	–	Fig.	–	pF
Emitter-to-Base Capacitance	$V_{BE} = 4$ V, f = 1 MHz	–	5	–	pF
Voltage Gain	$V_{CE} = 6$ V, f = 10 MHz $R_L = 1\ k\Omega$, $I_C = 1$ mA	–	28	–	dB
Power Gain	Cascode Configuration f = 100 MHz, $V^+ = 12$ V	27	30	–	dB
Noise Figure	$I_C = 1$ mA	–	3.5	–	dB
Input Resistance	Common-Emitter Configuration $V_{CE} = 6$ V $I_C = 1$ mA	–	400	–	Ω
Output Resistance		–	4.6	–	kΩ
Input Capacitance		–	3.7	–	pF
Output Capacitance		–	2	–	pF
Magnitude of Forward Transadmittance	f = 200 MHz	–	24	–	mmho

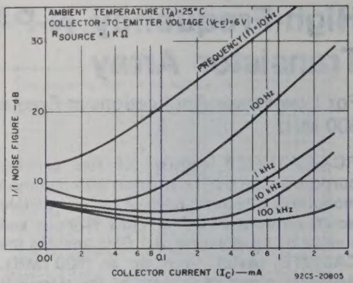


Fig. 3 – 1/f noise figure as a function of collector current at $R_{SOURCE} = 1\ k\Omega$.

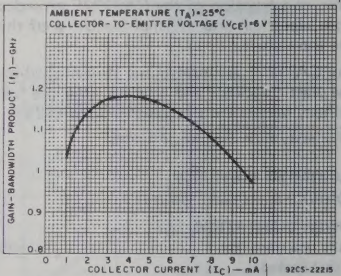


Fig. 4 – Gain-bandwidth product as a function of collector current.

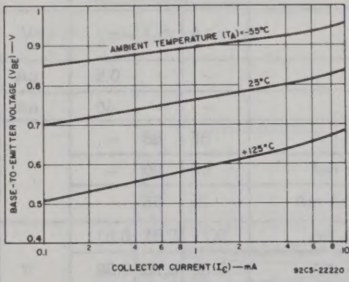


Fig. 5 – Base-to-emitter voltage as a function of collector current.

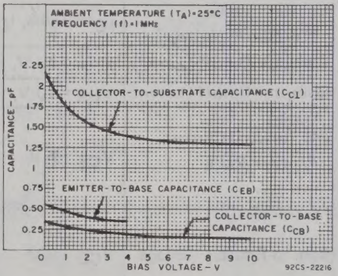


Fig. 6(a) – Capacitance as a function of bias voltage for Q_2.

Transistor	Capacitance (pF) C_{CB} Pkg.	C_{CB} Total	C_{CE} Pkg.	C_{CE} Total	C_{EB} Pkg.	C_{EB} Total	C_{CI} Pkg.	C_{CI} Total
Bias Voltage	–	6 V	–	6 V	–	4 V	–	6 V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

Fig. 6(b) – Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

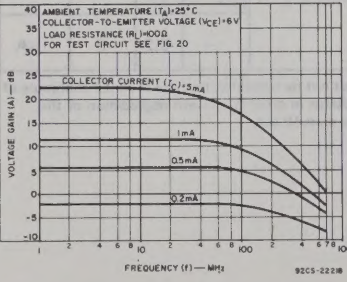


Fig. 7 – Voltage gain as a function of frequency at $R_L = 100\ \Omega$.

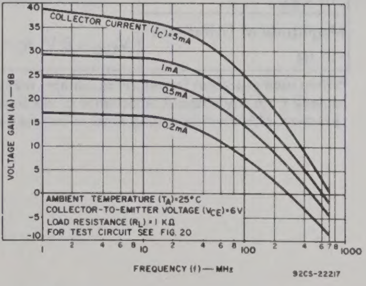


Fig. 8 – Voltage gain as a function of frequency at $R_L = 1\ k\Omega$.

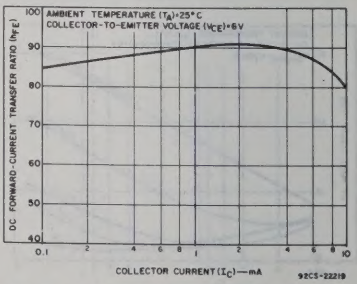


Fig. 9 – DC forward-current transfer ratio as a function of collector current.

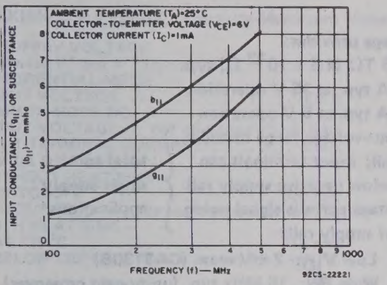


Fig. 10 — Input admittance (Y_{11}) as a function of frequency.

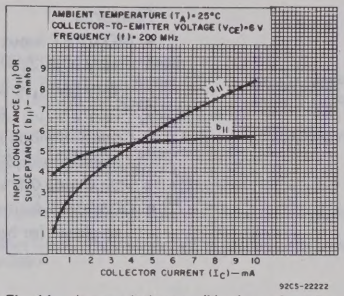


Fig. 11 — Input admittance (Y_{11}) as a function of collector current.

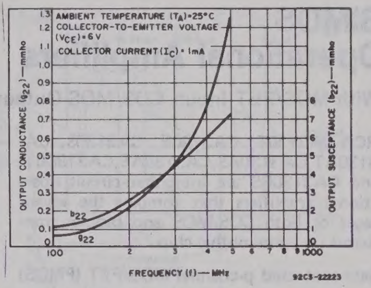


Fig. 12 — Output admittance (Y_{22}) as a function of frequency.

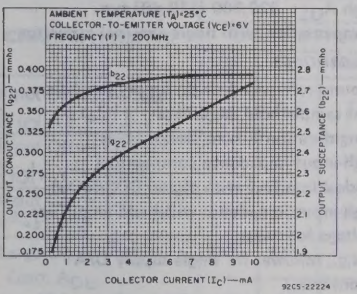


Fig. 13 — Output admittance (Y_{22}) as a function of collector current.

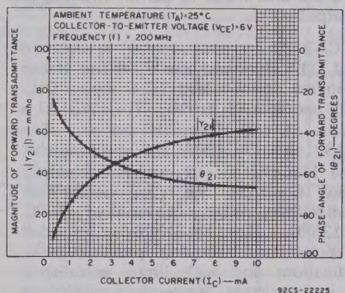


Fig. 14 — Forward transadmittance (Y_{21}) as a function of collector current.

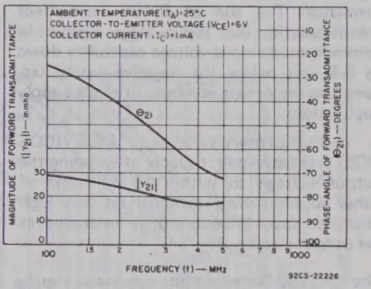


Fig. 15 — Forward transadmittance (Y_{21}) as a function of frequency.

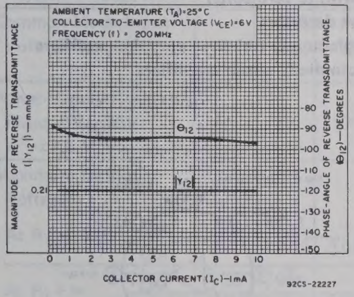


Fig. 16 — Reverse transadmittance (Y_{12}) as a function of collector current.

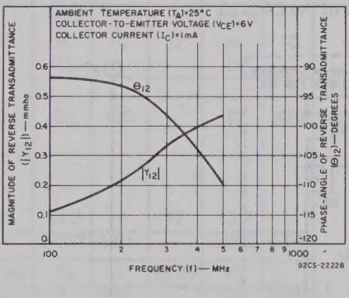


Fig. 17 — Reverse transadmittance (Y_{12}) as a function of frequency.

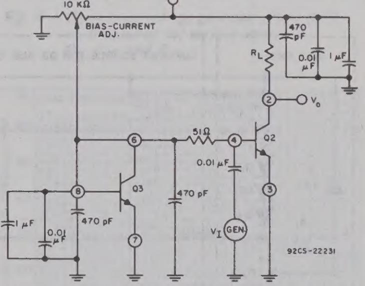


Fig. 18 — Voltage-gain test circuit using current-mirror biasing for Q_2.

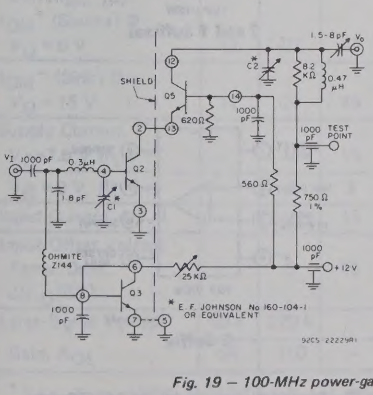


Fig. 19 — 100-MHz power-gain and noise-figure test circuit.

This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

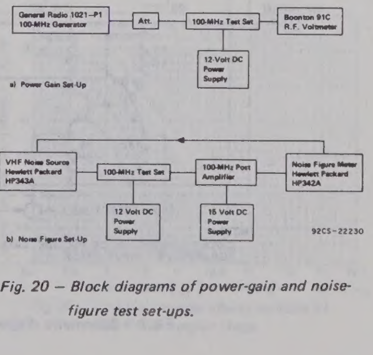


Fig. 20 — Block diagrams of power-gain and noise-figure test set-ups.

CA3130, CA3130A, CA3130B Types

BiMOS Operational Amplifiers

With MOS/FET Input, COS/MOS Output

RCA-CA3130T, CA3130E, CA3130S, CA3130AT, CA3130AS, CA3130AE, CA3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3130 is available in chip form (H suffix). The CA3130 and CA3130A are also available in the Mini-DIP 8-lead dual-in-line plastic package (E suffix). All types operate over the full military-temperature range of −55°C to +125°C. The CA3130B is intended for applications requiring premium-grade specifications and with limits established for: input current, temperature coefficient of input-offset voltage, and gain over the range of −55°C to +125°C. The CA3130A offers superior input characteristics over those of the CA3130.

Features:

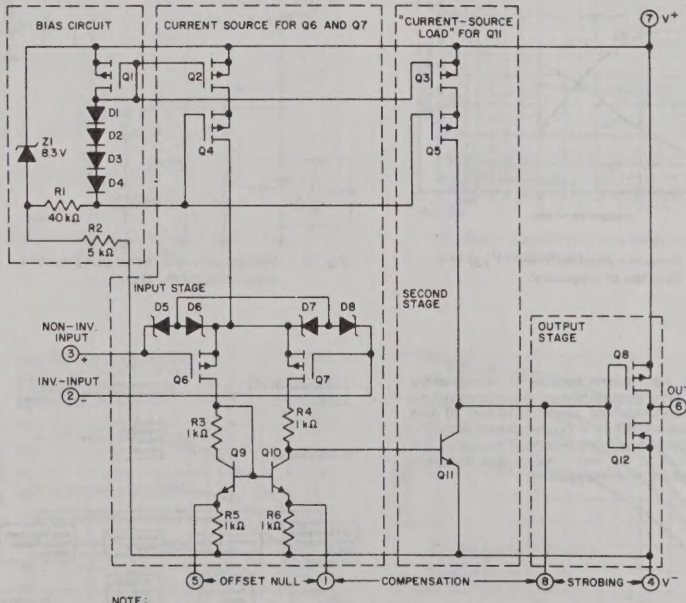
- **MOS/FET input stage provides:**
  - **very high Z_I = 1.5 TΩ (1.5×10^{12} Ω) typ.**
  - **very low I_I = 5 pA typ. at 15-V operation**
  - **2 pA typ. at 5-V operation**
- **Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail**
- **COS/MOS output stage permits signal swing to either (or both) supply rails**

Ideal for single-supply applications

- **Low V_{IO}: 2 mV max. (CA3130B)**
- **Wide BW: 15 MHz typ. (unity-gain crossover)**
- **High SR: 10 V/μs typ. (unity-gain follower)**
- **High output current (I_O): 20 mA typ.**
- **High A_{OL}: 320,000 (110 dB) typ.**
- **Compensation with single external capacitor**

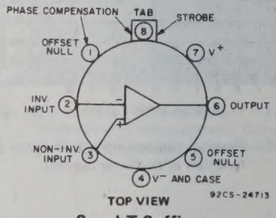
Applications:

- **Ground-referenced single-supply amplifiers**
- **Fast sample-hold amplifiers**
- **Long-duration timers/monostables**
- **High-input-impedance comparators (ideal interface with digital COS/MOS)**
- **High-input-impedance wideband amplifiers**
- **Voltage followers (e.g., follower for single-supply D/A converter)**
- **Voltage regulators (permits control of output voltage down to zero volts)**
- **Peak detectors**
- **Single-supply full-wave precision rectifiers**
- **Photo-diode sensor amplifiers**

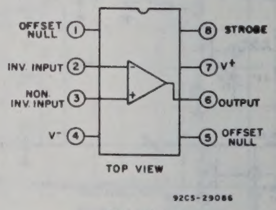


NOTE: DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

Fig. 1 – Schematic diagram of the CA3130 Series.



S and T Suffixes



E Suffix

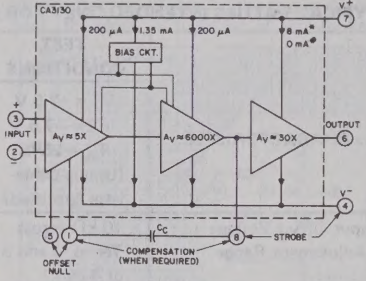
Fig. 2 – Functional diagrams for the CA3130 series.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V$^+$ and V$^-$ Terminals) . . . . 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE . . . . ±8 V
COMMON-MODE DC
INPUT VOLTAGE . . . (V$^+$ +8 V) to (V$^-$ −0.5 V)
INPUT-TERMINAL CURRENT . . . . 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK –
UP TO 55°C . . . . 630 mW
ABOVE 55°C . . . . Derate linearly 6.67 mW/°C
WITH HEAT SINK –
AT 125°C . . . . 418 mW
BELOW 125°C . . . Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (all types) . . . . . −55 to + 125°C
STORAGE (all types) . . . . −65 to + 150°C
OUTPUT SHORT-CIRCUIT
DURATION* . . . . INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 mm) FROM CASE
FOR 10 SECONDS MAX. . . . . . +265°C

*Short circuit may be applied to ground or to either supply.



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
* WITH INPUT TERMINALS BIASED SO THAT TERM 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
• WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

92CS-24715

Fig. 3 – Block diagram of the CA3130 Series.

ELECTRICAL CHARACTERISTICS at T_A=25°C, V$^+$=15 V, V$^-$ = 0 V (Unless otherwise specified)

CHARACTERISTIC		LIMITS									Units
		CA3130B (T,S)			CA3130A (T,S,E)			CA3130 (T,S,E)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, V$^\pm$=±7.5 V		–	0.8	2	–	2	5	–	8	15	mV
Input Offset Current, $\|I_{IO}\|$, V$^\pm$=±7.5 V		–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I V$^\pm$=±7.5 V		–	5	20	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL} V_O=10 V_{p-p}, R_L=2 kΩ		100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V
		100	110	–	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR		86	100	–	80	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}		0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^\pm$ V$^\pm$=±7.5 V		–	32	100	–	32	150	–	32	320	μV/V
Maximum Output Voltage: At R_L=2 kΩ	V_{OM}^+	12	13.3	–	12	13.3	–	12	13.3	–	V
	V_{OM}^-	–	0.002	0.01	–	0.002	0.01	–	0.002	0.01	
At R_L = ∞	V_{OM}^+	14.99	15	–	14.99	15	–	14.99	15	–	
	V_{OM}^-	–	0	0.01	–	0	0.01	–	0	0.01	
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V		12	22	45	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V		12	20	45	12	20	45	12	20	45	
Supply Current, I^+: V_O=7.5 V, R_L = ∞		–	10	15	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞		–	2	3	–	2	3	–	2	3	
Input Current, I_I*		–	Fig.12	15	–	Fig.12	–	–	Fig.12	–	nA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*		–	5	15	–	10	–	–	10	–	μV/°C
Large-Signal Voltage Gain, A_{OL}*		50 k	320 k	–	–	320 k	–	–	320 k	–	V/V
		94	110	–	–	110	–	–	110	–	dB

* T_A = −55 to +125°C, V$^\pm$ = ± 7.5 V (I_I and $\Delta V_{IO}/\Delta T$), V_O = 10 V_{p-p} and R_L = 2 kΩ (A_{OL}).

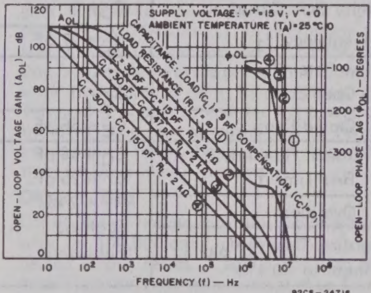


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Fig. 4 – Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

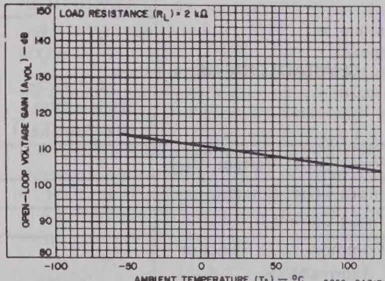

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Fig. 5 – Open-loop gain vs. temperature.

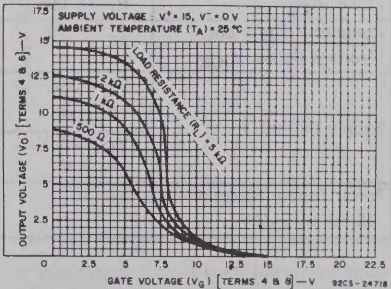

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Fig. 6 – Voltage transfer characteristics of COS/MOS output stage.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS $V^+ = +7.5$ V $V^- = -7.5$ V $T_A = 25^{\circ}C$ (Unless Otherwise Specified)	CA3130B (T,S)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	±22	mV
Input Resistance, R_I		1.5	1.5	1.5	TΩ
Input Capacitance, C_I	f = 1 MHz	4.3	4.3	4.3	pF
Equivalent Input Noise Voltage, e_n	BW = 0.2 MHz R_S = 1 MΩ*	23	23	23	μV
Unity Gain Crossover	$C_C = 0$	15	15	15	MHz
Frequency, f_T	C_C = 47 pF	4	4	4	
Slew Rate, SR:					
Open Loop	$C_C = 0$	30	30	30	V/μs
Closed Loop	C_C = 56 pF	10	10	10	
Transient Response: Rise Time, t_r	C_C = 56 pF C_L = 25 pF R_L = 2 kΩ (Voltage Follower)	0.09	0.09	0.09	μs
Overshoot		10	10	10	%
Settling Time (4 V_{p-p} Input to <0.1%)		1.2	1.2	1.2	μs

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10 MΩ.

CHARACTERISTIC	TEST CONDITIONS $V^+ = 5$ V $V^- = 0$ V $T_A = 25^{\circ}C$ (Unless Otherwise Specified)	CA3130B (T,S)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
Input Offset Voltage, V_{IO}		1	2	8	mV
Input Offset Current, I_{IO}		0.1	0.1	0.1	pA
Input Current, I_I		2	2	2	pA
Common-Mode Rejection Ratio, CMRR		100	90	80	dB
Large-Signal Voltage	V_O = 4 V_{p-p}	100 k	100 k	100 k	V/V
Gain, A_{OL}	R_L = 5 kΩ	100	100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, $R_L = \infty$	300	300	300	μA
	V_O = 2.5 V, $R_L = \infty$	500	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V

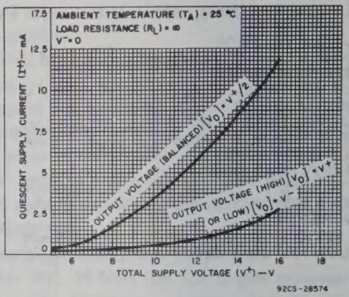

Fig. 7 – Quiescent supply current vs. supply voltage.

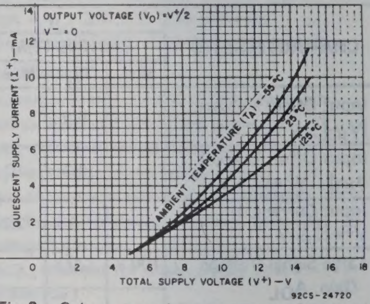

Fig. 8 – Quiescent supply current vs. supply voltage at several temperatures.

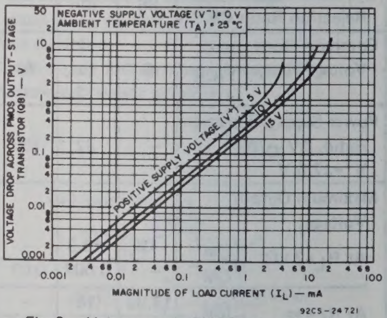

Fig. 9 – Voltage across PMOS output transistor (Q8) vs. load current.

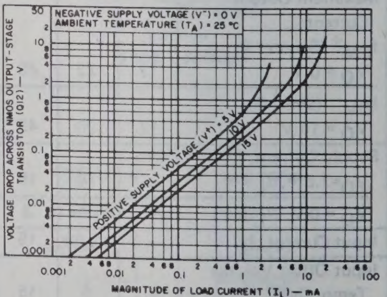

Fig. 10 – Voltage across NMOS output transistor (Q12) vs. load current.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages—The circuit of the CA3130 is shown in Fig. 1. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes nonconductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage, Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are nonlinear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5 pA at T_A=25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig.11 contains data showing the variation of input current as a function of common-mode input voltage at T_A = 25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

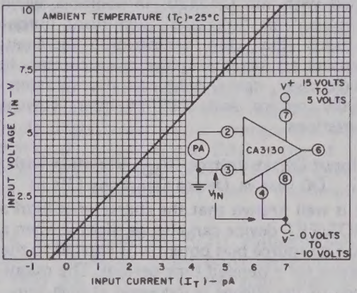

Fig.11 — Input current vs. common-mode voltage.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig.12 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

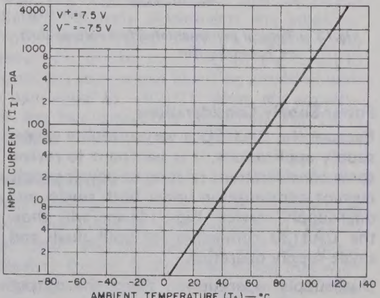

Fig.12 — Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

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†For general information on the characteristics of COS/MOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array".

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig.13 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

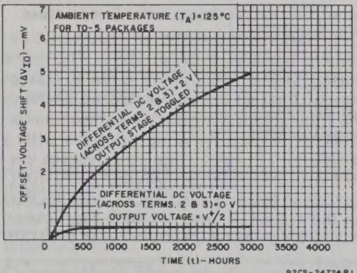

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Fig.13 – Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 14a and 14b show the CA3130 connected for both dual- and single-supply operation.

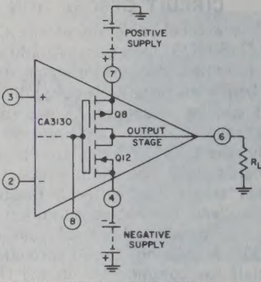
Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Term. 8 down to that of Term. 4.

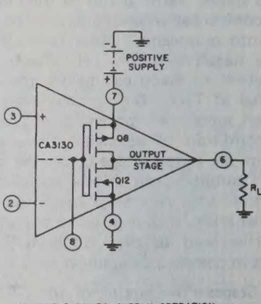
Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig.14b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 µV when the test-circuit amplifier of Fig. 15 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.



(a) DUAL POWER-SUPPLY OPERATION



(b) SINGLE POWER-SUPPLY OPERATION

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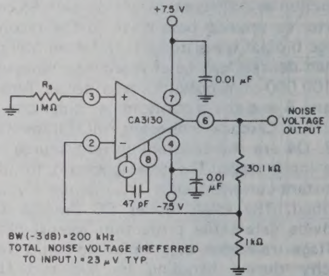
Fig.14 – CA3130 output stage in dual and single power-supply operation.



BW (-3 dB) = 200 kHz
TOTAL NOISE VOLTAGE (REFERRED TO INPUT) = 23 µV TYP

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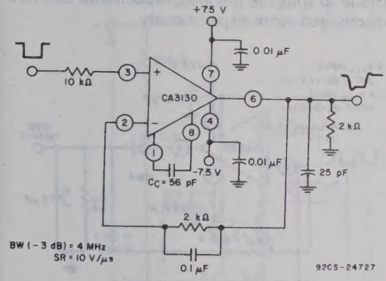
Fig.15 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

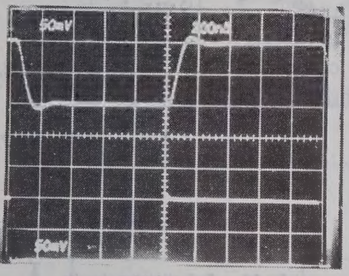
TYPICAL APPLICATIONS

Voltage Followers

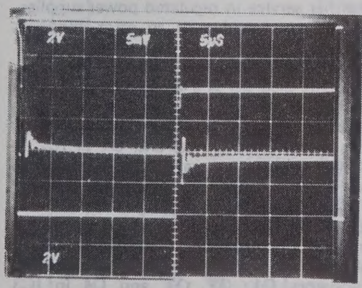
Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 16 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 17, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 17a with input-signal ramping. The waveforms in Fig. 17b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 17b also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.





Top Trace: Output
Bottom Trace: Input
(a) Small-signal response (50 mV/div. and 200 ns/div.)



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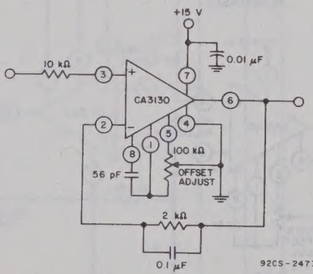
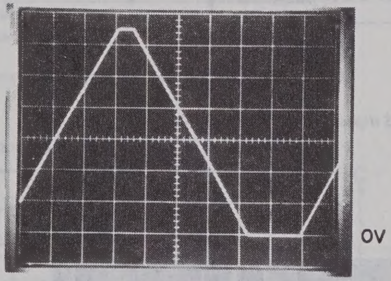
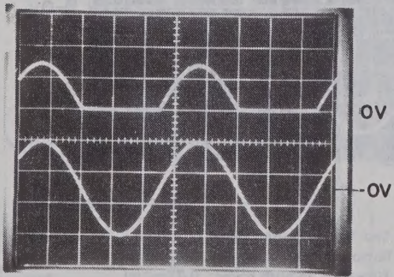
Top Trace: Output signal (2 V/div. and 5 µs/div.)
Center Trace: Difference signal (5 mV/div. and 5 µs/div.)
Bottom Trace: Input signal (2 V/div. and 5 µs/div.)
(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

Fig. 16 – Split-supply voltage follower with associated waveforms.





(a) Output-waveform with input-signal ramping (2 V/div. and 500 µs/div.)



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Top Trace: Output (5 V/div. and 200 µs/div.)
Bottom Trace: Input (5 V/div. and 200 µs/div.)
(b) Output-waveform with ground-reference sine-wave input

Fig.17 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig.9 in ICAN-6080).

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.18 This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig.18.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Fig. 19. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to $-R2/R1$. When the equality of the two equations shown in Fig. 19 is satisfied, the full-wave output is symmetrical.

Peak Detectors

Peak-detector circuits are easily implemented with the CA3130, as illustrated in Fig. 20 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the

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*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.

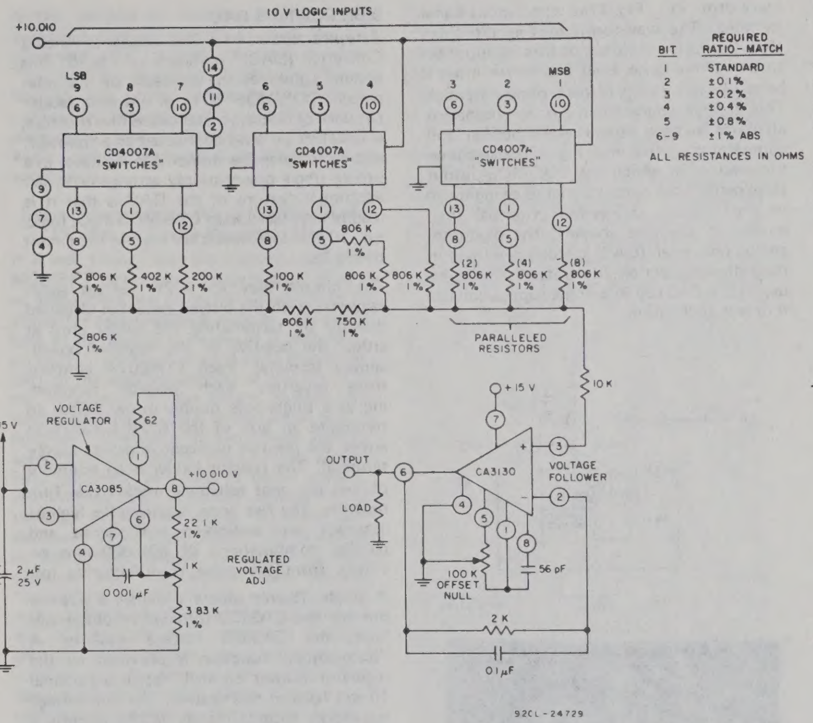
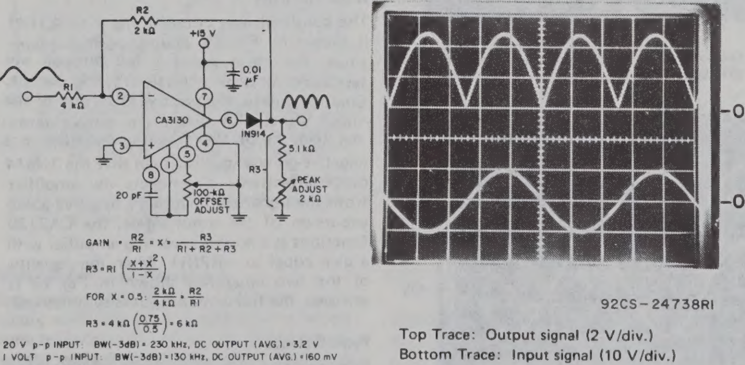


Fig.18 – 9-bit DAC using COS/MOS digital switches and CA3130.


R2 2 kΩ
+15 V
0.01 µF
R1 4 kΩ
CA3130
IN914
5.1 kΩ
R3
PEAK ADJUST 2 kΩ
20 pF
100-kΩ OFFSET ADJUST
GAIN = R2/R1 = X = R3/(R1+R2+R3)
R3 = R1 ((X+X²)/(1-X))
FOR X = 0.5: 2 kΩ/4 kΩ = R2/R1
R3 = 4 kΩ (0.75/0.5) = 6 kΩ
20 V p-p INPUT: BW(-3dB) = 230 kHz, DC OUTPUT (AVG.) = 3.2 V
1 VOLT p-p INPUT: BW(-3dB) = 130 kHz, DC OUTPUT (AVG.) = 160 mV
92CS-24730
-0V
-0V
92CS-24738RI

Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

Fig.19 – Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.

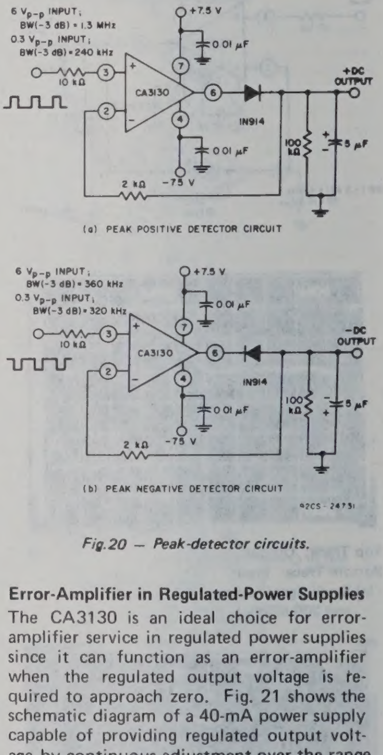

6 Vp-p INPUT; BW(-3 dB) = 1.3 MHz
0.3 Vp-p INPUT; BW(-3 dB) = 240 kHz
+7.5 V
0.01 µF
10 kΩ
CA3130
+DC OUTPUT
IN914
100 kΩ
5 µF
2 kΩ
-7.5 V
(a) PEAK POSITIVE DETECTOR CIRCUIT
6 Vp-p INPUT; BW(-3 dB) = 360 kHz
0.3 Vp-p INPUT; BW(-3 dB) = 320 kHz
-DC OUTPUT
(b) PEAK NEGATIVE DETECTOR CIRCUIT
92CS-24731

Fig.20 – Peak-detector circuits.

Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 21 shows the schematic diagram of a 40-mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Fig. 22 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 23. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

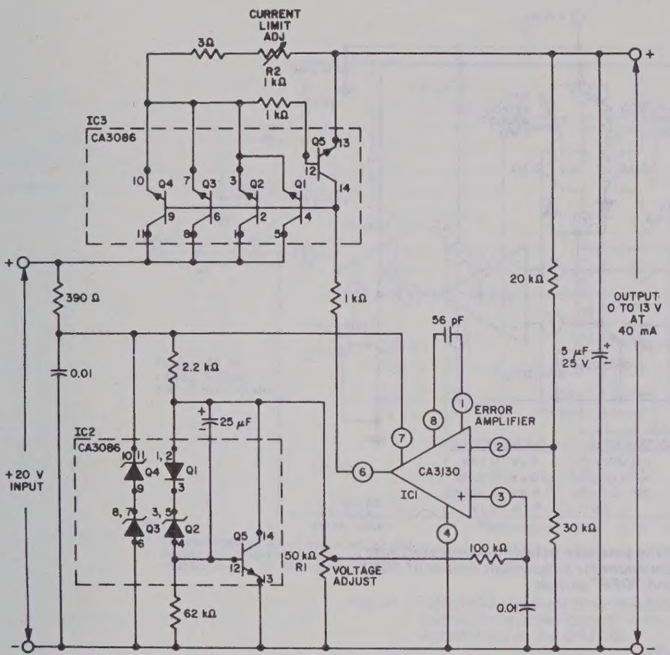
Function Generator

Fig. 24 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

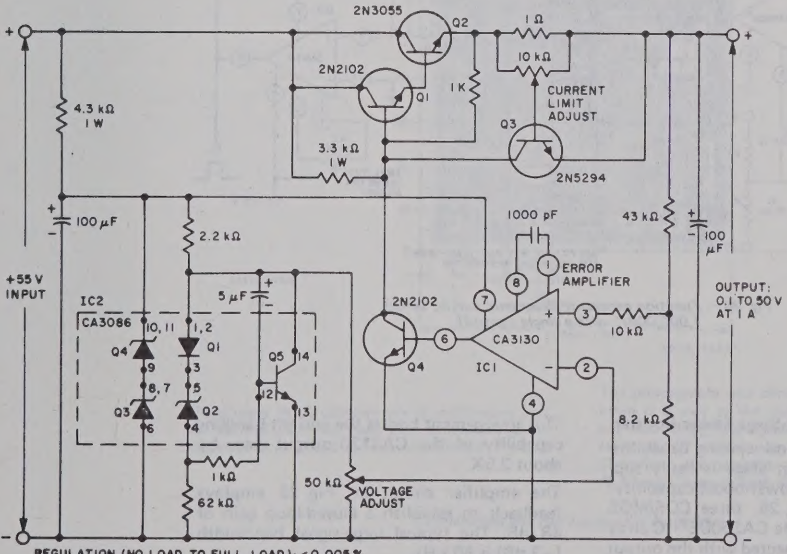
Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.



REGULATION (NO LOAD TO FULL LOAD): < 0.01%
INPUT REGULATION: 0.02%/V
HUM AND NOISE OUTPUT: < 25 µV UP TO 100 kHz

92CM-24732

Fig.21 — Voltage regulator circuit (0 to 13 V at 40 ma).



REGULATION (NO LOAD TO FULL LOAD): < 0.005%
INPUT REGULATION: < 0.01%/V
HUM AND NOISE OUTPUT: < 250 µV RMS UP TO 100 kHz

92CM-24734

Fig.22 — Voltage regulator circuit (0.1 to 50 V at 1 A).

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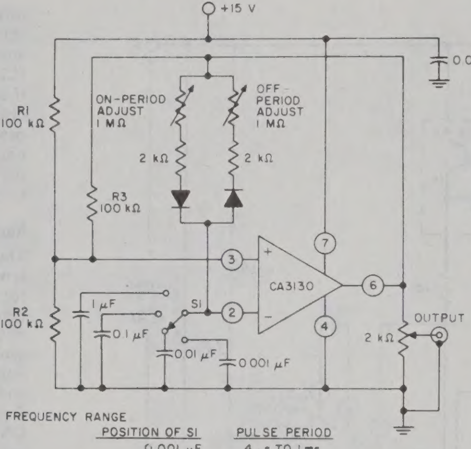
*See File No. 475 and ICAN-6668.

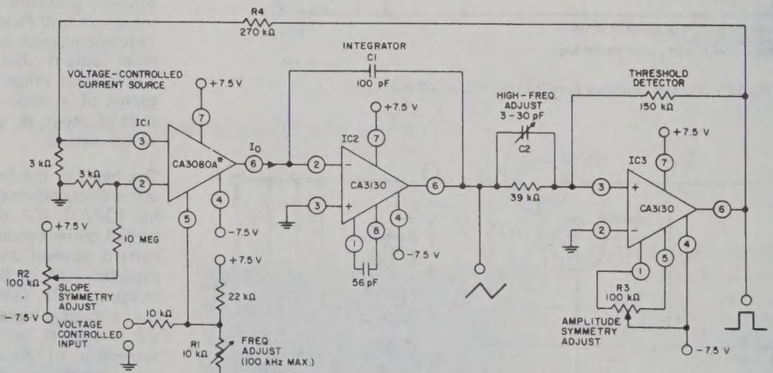
CA3130, CA3130A, CA3130B Types



FREQUENCY RANGE

POSITION OF S1	PULSE PERIOD
0.001 μF	4 μs TO 1 ms
0.01 μF	40 μs TO 10 ms
0.1 μF	0.4 ms TO 100 ms
1 μF	4 ms TO 1 s

Fig.23 – Pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.



*SEE FILE NO. 475 AND ICAN-6668 FOR TECHNICAL INFORMATION

Fig. 24 – Function generator (frequency can be varied 1,000,000/1 with a single control).

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 25, three COS/MOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Fig. 25 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (−3 dB) is 50 kHz.

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*See File No. 619 for technical information.

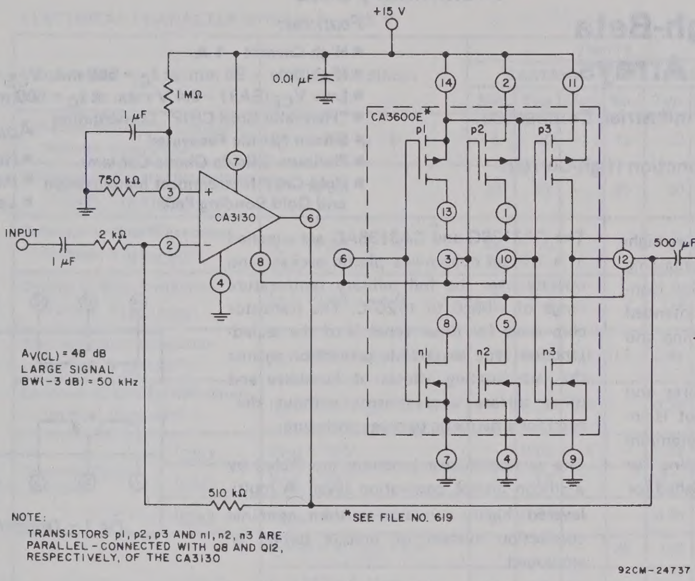
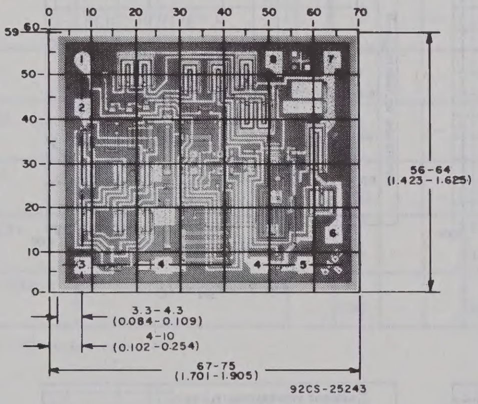


Fig. 25 — COS/MOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CA3130H.

CA3138G, CA3138AG Types

Preliminary Data

High-Current, High-Beta N-P-N Transistor Arrays

Hermetic Gold-CHIP Type For Industrial, Commercial, and Military Applications

Four Isolated Discrete Sealed-Junction High-Current N-P-N Transistors

Features:

- **High Current –1 A**
- **High Beta – 95 min. at I_C = 500 mA, V_{CE} = 5 V**
- **Low V_{CE}(SAT) –0.4 V max. at I_C = 500 mA, I_B = 12.5 mA**
- **"Hermetic Gold-CHIP" Construction**
- **Silicon Nitride Passivated**
- **Platinum Silicide Ohmic Contacts**
- **Gold-CHIP Interconnect Metallization and Gold Bonding Pads**

Applications:

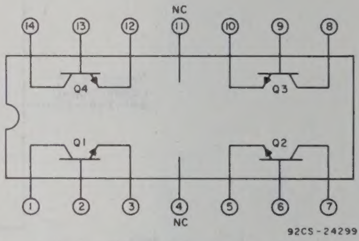
- **High-Current LED Driver**
- **Relay and Solenoid Driver**
- **Lamp Driver**

The RCA-CA3138G and CA3138AG are high-current n-p-n transistor arrays containing four isolated (discrete) sealed-junction high-current n-p-n transistors. They are intended for high-current, high-speed switching and driver applications.

The CA3138AG has all the features and characteristics of the CA3138G but is intended for applications requiring premium grade specifications –– higher rating for V_{CBO} of 25 volts and limits established for I_{CEO}, I_{EBO}, and h_{FE} at 10 mA.

The CA3138G and CA3138AG are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of –55°C to +125°C. The transistor chip used for these types is of the sealed-junction type to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure.

The semiconductor junctions are sealed by a silicon nitride passivation layer. A multilayered, highly corrosion-resistant, terminal connection system of unique design is employed.

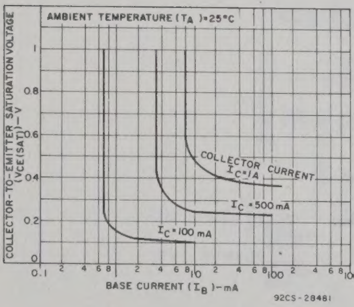


92CS-24299

Fig. 1 – Terminal diagram (top view).

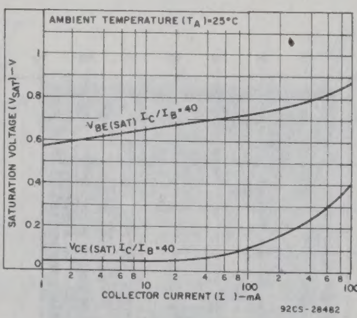
MAXIMUM RATINGS, *Absolute-Maximum Values*

COLLECTOR-TO-EMITTER VOLTAGE .... With Base Open (V_{CEO})	15	V
COLLECTOR-TO-BASE VOLTAGE With Emitter Open (V_{CBO})		
CA3138G	20	V
CA3138AG	25	V
EMITTER-TO-BASE VOLTAGE .... With Collector Open (V_{EBO})	5	V
COLLECTOR CURRENT (I_C)	1	A
POWER DISSIPATION (P_D):		
At T_A up to 25°C:		
For Each Transistor	1	W
Total Package	2	W
At T_A above 25°C derate linearly	20	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C



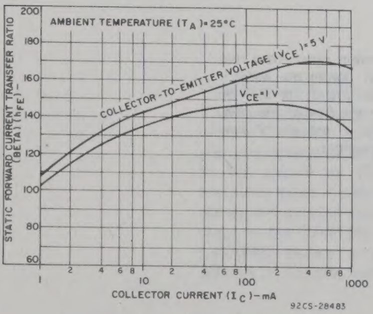
92CS-28481

Fig. 2 – V_{CE}(sat) vs I_B



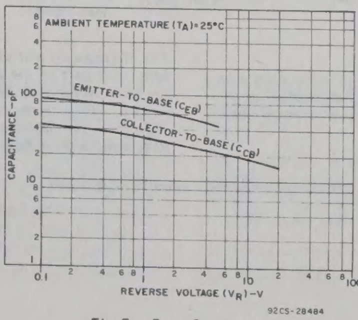
92CS-28482

Fig. 3 – V_{sat} vs I_C



92CS-28483

Fig. 4 – h_{FE} vs I_C



92CS-28484

Fig. 5 – C_{CB}, C_{CE} vs V_R

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Characteristic	Test Conditions	LIMITS						Units
		CA3138G			CA3138AG			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO}(sus)$*	$I_C = 1$ mA, $I_B = 0$	15	20	–	15	20	–	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	$I_C = 10\ \mu A$	20	55	–	25	60	–	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$	20	55	–	25	60	–	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$	5	7.2	–	5	7.2	–	V
Base-to-Emitter Saturation Voltage, $V_{BE}(sat)$*	$I_C = 500$ mA, $I_B = 12.5$ mA	0.7	0.81	1.1	0.7	0.81	1.1	V
Collector-to-Emitter Saturation Voltage, $V_{CE}(sat)$*	$I_C = 500$ mA, $I_B = 12.5$ mA	–	0.26	0.4	–	0.26	0.4	V
Collector-Cutoff Current I_{CBO}	$V_{CB} = 15$ V	–	0.03	1	–	0.02	0.1	μA
I_{CEO}	$V_{CE} = 10$ V	–	0.5	–	–	0.3	1.0	
I_{EBO}	$V_{EB} = 4$ V	–	0.01	–	–	0.01	0.1	
Static Forward-Current Transfer Ratio (Beta), h_{FE}*	$I_C = 10$ mA, $V_{CE} = 5$ V	–	–	–	35	140	–	
	$I_C = 100$ mA, $V_{CE} = 5$ V	80	160	450	80	160	450	
	$I_C = 500$ mA, $V_{CE} = 5$ V	95	170	500	95	170	500	
	$I_C = 1$ A, $V_{CE} = 5$ V	40	170	–	40	170	–	
Small-Signal Forward Current Transfer Ratio, h_{fe}	$I_C = 50$ mA, $V_{CE} = 10$ V, f = 100 MHz	2	–	–	2	–	–	
Collector-to-Base Capacitance, C_{CB}	$V_{CB} = 10$ V, $I_E = 0$	–	18	–	–	18	–	pF
Emitter-to-Base Capacitance, C_{EB}	$V_{EB} = 0.5$ V, $I_C = 0$	–	77	–	–	77	–	pF
Rise Time (See Test Ckt. Fig. 6), t_r	$I_C = 570$ mA	–	6	–	–	6	–	ns
Fall Time (See Test Ckt. Fig. 6), t_f	$I_{B1} = 30$ mA	–	100	–	–	100	–	ns
Delay Time (See Test Ckt. Fig. 6), t_d	$I_{B2} = 0$	–	7.5	–	–	7.5	–	ns
Storage Time (See Test Ckt. Fig. 6), t_s		–	850	–	–	850	–	ns

*Pulse Conditions: width = 300 μs; duty cycle = 1%.

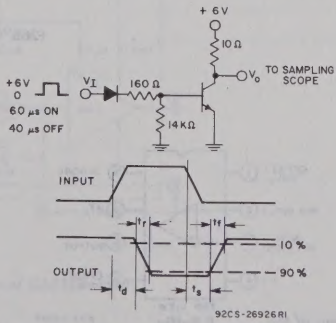


Fig. 6 – Switching time test circuit and waveforms.

CA3140, CA3140A, CA3140B Types

BiMOS Operational Amplifiers

With MOS/FET Input, Bipolar Output

The CA3140B, CA3140A, and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 COS/MOS operational amplifiers and the versatility of the 741 series of industry-standard operational amplifiers.

The CA3140, CA3140A, and CA3140 BiMOS operational amplifiers feature gate-protected MOS/FET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA3140B operates at supply voltages from 4 to 44 volts; the CA3140A and CA3140 from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling.

The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail or to ground.

The CA3140 Series has the same 8-lead terminal pin-out used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140 is available in chip form (H suffix). The CA3140A and CA3140 are also available in an 8-lead dual-in-line plastic package (Mini-DIP-E suffix). The CA3140B is intended for operation at supply voltages ranging from 4 to 44 volts, for applications requiring premium-grade specifications and with electrical limits established for operations over the range from −55°C to +125°C. The CA3140A and CA3140 are for operation at supply voltages up to 36 volts (±18 volts). The CA3140 ages up to 36 volts (±18 volts). All types can be operated safely over the temperature range from −55°C to +125°C.

Features:

- **MOS/FET Input Stage**
  - **(a) Very high input impedance (Z_{IN}) – 1.5 TΩ typ.**
  - **(b) Very low input current (I_I) – 10 pA typ. at ± 15**
  - **(c) Low input-offset voltage (V_{IO}) – to 2 mV max.**
  - **(d) Wide common-mode input-voltage range (V_{ICR}) – can be swung 0.5 volt below negative supply-voltage rail**
  - **(e) Output swing complements input common-mode range**
  - **(f) Rugged input stage – bipolar diode protected**
- **Directly replaces industry type 741 in most applications**
- **Includes numerous industry operational amplifier categories such as general-purpose, FET input, wideband (high slew rate)**
- **Operation from 4-to-44 volts Single or Dual supplies**
- **Internally compensated**
- **Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts**
- **Wide bandwidth – 4.5 MHz unity gain at ± 15 V or 30 V; 3.7 MHz at 5 V**
- **High voltage-follower slew rate – 9 V/µs**
- **Fast settling time – 1.4 µs typ. to 10 mV with a 10-V_{p-p} signal**
- **Output swings to within 0.2 volt of negative supply**
- **Strobable output stage**

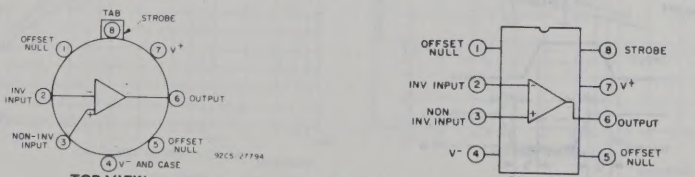
MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3140, CA3140A	CA3140B
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V	44 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V	±8 V
COMMON-MODE DC INPUT VOLTAGE		(V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT		1 mA
DEVICE DISSIPATION:		
WITHOUT HEAT SINK –		
UP TO 55°C		630 mW
ABOVE 55°C		Derate linearly 6.67 mW/°C
WITH HEAT SINK –		
Up to 55°C		1 W
Above 55°C		Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:		
OPERATING (ALL TYPES)		−55 to + 125°C
STORAGE (ALL TYPES)		−65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION*		INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING): AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.		+265°C

* Short circuit may be applied to ground or to either supply.

Applications:

- **Ground-referenced single-supply amplifiers in automobile and portable instrumentation**
- **Sample and hold amplifiers**
- **Long-duration timers/multivibrators (microseconds–minutes–hours)**
- **Photocurrent instrumentation**
- **Peak detectors**
- **Active filters**
- **Comparators**
- **Interface in 5 V TTL systems & other low-supply voltage systems**
- **All standard operational amplifier applications**
- **Function generators**
- **Tone controls**
- **Power supplies**
- **Portable instruments**
- **Intrusion alarm systems**



TOP VIEW
S and T Suffixes

TOP VIEW
E Suffix

Fig. 1 – Functional diagrams of the CA3140 series.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS $V^+ = +15$ V $V^- = -15$ V $T_A = 25^oC$	CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage Adjustment Resistor	Typ. Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}	43	18	4.7	kΩ
Input Resistance R_I		1.5	1.5	1.5	TΩ
Input Capacitance C_I		4	4	4	pF
Output Resistance R_O		60	60	60	Ω
Equivalent Wideband Input Noise Voltage e_n (See Fig. 39)	BW = 140 kHz R_S = 1 MΩ	48	48	48	µV
Equivalent Input Noise Voltage e_n (See Fig.10)	f = 1 kHz, R_S = 100 Ω	40	40	40	nV/$\sqrt{Hz}$
	f = 10 kHz, R_S = 100 Ω	12	12	12	
Short-Circuit Current to Opposite Supply Source I_{OM}^+		40	40	40	mA
Sink I_{OM}^-		18	18	18	mA
Gain-Bandwidth Product, (See Figs. 5 &18) f_T		4.5	4.5	4.5	MHz
Slew Rate, (See Fig.6) SR		9	9	9	V/µs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low		220	220	220	µA
Transient Response: Rise Time t_r	R_L = 2 kΩ C_L = 100 pF	0.08	0.08	0.08	µs
Overshoot (See Fig. 37)		10	10	10	%
Settling Time at 10 V_{p-p}, (See Fig.17) t_s 1 mV	R_L = 2 kΩ C_L = 100 pF Voltage Follower	4.5	4.5	4.5	µs
10 mV		1.4	1.4	1.4	

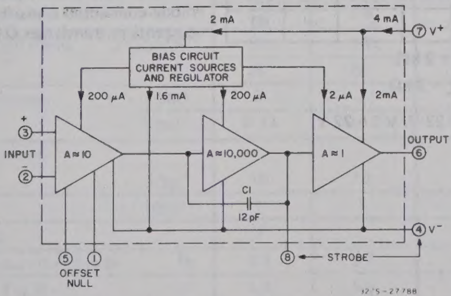


Fig.2 – Block diagram of CA3140 series.

CIRCUIT DESCRIPTION

Fig.2 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensating capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The schematic circuit diagram of the CA3140 is shown in Fig.3. It consists of a differential-input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second Stage – Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage – The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

CA3140, CA3140A, CA3140B Types

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At $V^+ = 15$ V, $V^- = 15$ V, $T_A = 25^oC$ Unless Otherwise Specified

CHARACTERISTIC		LIMITS								UNITS
	CA3140B			CA3140A			CA3140			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $|V_{IO}|$	–	0.8	2	–	2	5	–	5	15	mV
Input Offset Current, $|I_{IO}|$	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	30	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}● (See Figs. 4,18)	50 k	100 k	–	20 k	100 k	–	20 k	100 k	–	V/V
	94	100	–	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR (See Fig.9)	–	20	50	–	32	320	–	32	320	µV/V
	86	94	–	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig.20)	–15	–15.5 to +12.5	12	–15	–15.5 to +12.5	12	–15	–15.5 to +12.5	11	V
Power-Supply Rejection Ratio, PSRR $\Delta V_{IO}/\Delta V$ (See Fig.11)	–	32	100	–	100	150	–	100	150	µV/V
	80	90	–	76	80	–	76	80	–	dB
Max. Output Voltage■ (See Figs.13,20) V_{OM}^+	+12	13	–	+12	13	–	+12	13	–	V
V_{OM}^-	–14	–14.4	–	–14	–14.4	–	–14	–14.4	–	
Supply Current, I^+ (See Fig.7)	–	4	6	–	4	6	–	4	6	mA
Device Dissipation, P_D	–	120	180	–	120	180	–	120	180	mW
Input Current, I_I▲ (See Fig.19)	–	10	30	–	10	–	–	10	–	nA
Input Offset Voltage $|V_{IO}|$▲	–	1.3	3	–	3	–	–	10	–	mV
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$	–	5	–	–	6	–	–	8	–	µV/°C
Large-Signal Voltage Gain, A_{OL}▲ (See Figs.4,18)	20 k	100 k	–	–	100 k	–	–	100 k	–	V/V
	86	100	–	–	100	–	–	100	–	dB
Max. Output Voltage,★ V_{OM}^+	+19	+19.5	–	–	–	–	–	–	–	V
V_{OM}^-	–21	–21.4	–	–	–	–	–	–	–	
Large-Signal Voltage Gain, A_{OL}♠★	20 k	50 k	–	–	–	–	–	–	–	V/V
	86	94	–	–	–	–	–	–	–	dB

● At $V_O = 26V_{p-p}$, +12V, –14V and $R_L = 2$ kΩ.

■ At $R_L = 2$ kΩ.

▲ At $T_A = -55^oC$ to $+125^oC$, $V^+ = 15$ V, $V^- = 15$ V, $V_O = 26V_{p-p}$, $R_L = 2$ kΩ.

♠ At $V_O = +19$ V, –21 V, and $R_L = 2$ kΩ.

★ At $V^+ = 22$ V, $V^- = 22$ V.

When the CA3140 is operating such that output terminal 6 is sinking current to the V– bus, transistor Q16 is the current-sinking element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V– supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V– bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

Bias Circuit – Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

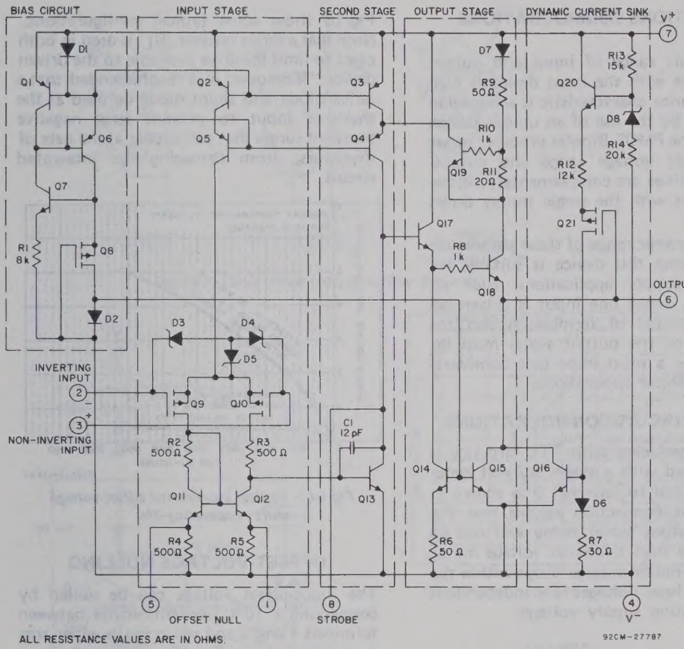


Fig.3 – Schematic diagram of CA3140 series.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE

At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$

CHARACTERISTIC		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage	$\|V_{IO}\|$	0.8	2	5	mV
Input Offset Current	$\|I_{IO}\|$	0.1	0.1	0.1	pA
Input Current	I_I	2	2	2	pA
Input Resistance		1	1	1	TΩ
Large-Signal Voltage Gain	A_{OL}	100 k	100 k	100 k	V/V
(See Figs.4,18)		100	100	100	dB
Common-Mode Rejection Ratio,	CMRR	20	32	32	µV/V
		94	90	90	dB
Common-Mode Input-Voltage Range	V_{ICR}	−0.5	−0.5	−0.5	V
(See Fig.20)		2.6	2.6	2.6	
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	32	100	100	µV/V
		90	80	80	dB
Maximum Output Voltage	V_{OM}^+	3	3	3	V
(See Figs.13,20)	V_{OM}^-	0.13	0.13	0.13	
Maximum Output Current:					
Source	I_{OM}^+	10	10	10	mA
Sink	I_{OM}^-	1	1	1	
Slew Rate (See Fig.6)		7	7	7	V/µs
Gain-Bandwidth Product (See Fig.5)	f_T	3.7	3.7	3.7	MHz
Supply Current (See Fig.7)	I^+	1.6	1.6	1.6	mA
Device Dissipation	P_D	8	8	8	mW
Sink Current from Term. 8 to Term. 4 to Swing Output Low		200	200	200	µA

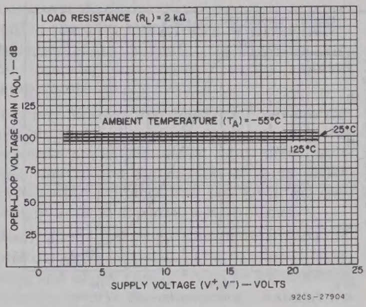


Fig.4 – Open-loop voltage gain vs supply voltage and temperature.

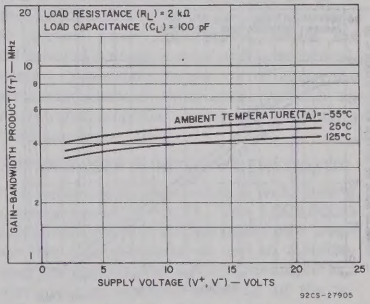


Fig.5 – Gain-bandwidth product vs supply voltage and temperature.

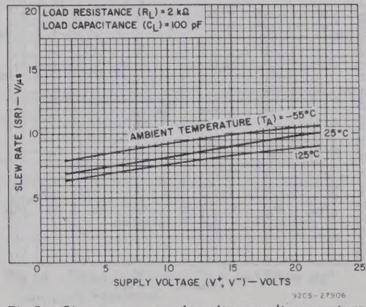


Fig.6 – Slew rate vs supply voltage andtemperature.

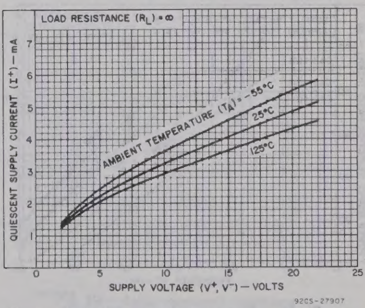


Fig.7 – Quiescent supply current vs supply voltage and temperature.

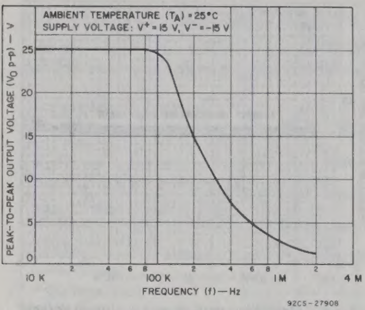


Fig.8 – Maximum output voltage swing vs frequency.

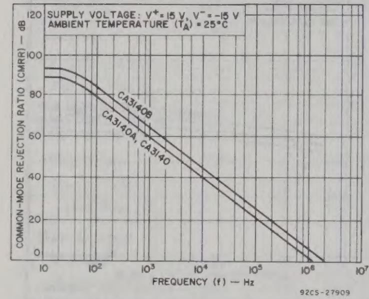


Fig.9 – Common-mode rejection ratio vs frequency.

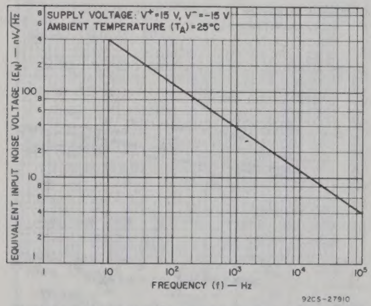


Fig.10 – Equivalent input noise voltage vs frequency.

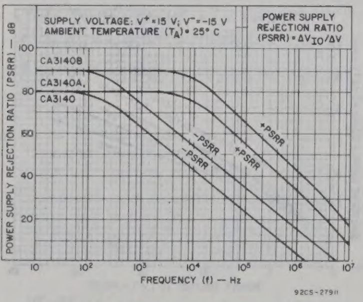


Fig.11 – Power supply rejection ratio vs frequency.

APPLICATIONS CONSIDERATIONS

Wide dynamic range of input and output characteristics with the most desirable high input-impedance characteristic is achieved in the CA3140 by the use of an unique design based upon the PMOS-Bipolar process. Input-common-mode voltage range and output-swing capabilities are complementary, allowing operation with the single supply down to four volts.

The wide dynamic range of these parameters also means that this device is suitable for many single-supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained – a most important consideration in comparator applications.

OUTPUT CIRCUIT CONSIDERATIONS

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2-volt zener diode connected to terminal 8 as shown in Fig.12. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

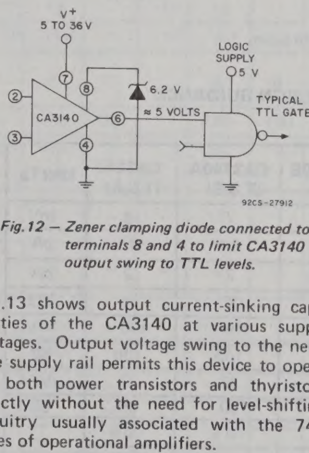


Fig.12 – Zener clamping diode connected to terminals 8 and 4 to limit CA3140 output swing to TTL levels.

Fig.13 shows output current-sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

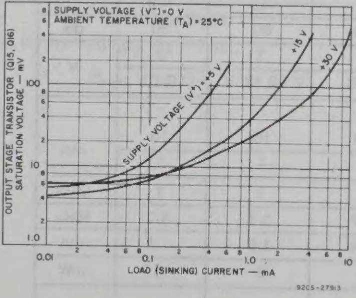


Fig.13 – Voltage across output transistors Q15 and Q16 vs load current.

Fig.16 show some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

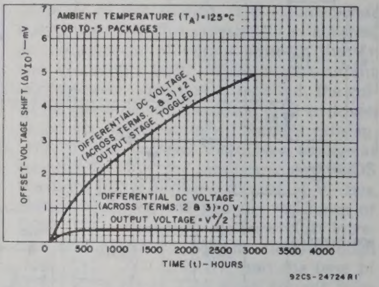


Fig.14 – Typical incremental offset-voltage shift vs operating life.

OFFSET-VOLTAGE NULLING

The input-offset voltage can be nulled by connecting a 10-kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Fig.15a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig.15b, to optimize its utilization range are given in the table "Typical Electrical Characteristics" shown in this bulletin.

An alternate system is shown in Fig.15c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

LOW-VOLTAGE OPERATION

Operation at total supply voltages as low as 4 volts is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low-voltage limitation occurs when the upper extreme of the input common-mode voltage range extends down to the voltage at terminal 4. This limit is reached at a total supply voltage just below 4 volts. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Fig.20 shows these characteristics and shows that with 2-volt dual supplies, the lower extreme of the input common-mode voltage range is below ground potential.

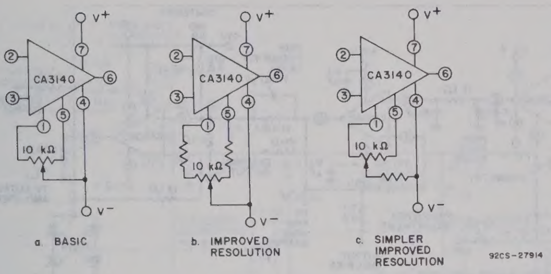


Fig.15 — Three offset-voltage nulling methods.

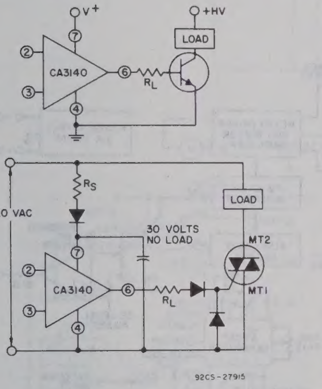


Fig.16 — Methods of utilizing the $V_{CE}(sat)$ sinking-current capability of the CA3140 series.

BANDWIDTH AND SLEW RATE

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open-loop −3 dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Fig.17 shows the typical settling time required to reach 1 mV or 10 mV of the final value for various levels of large signal inputs for the voltage-follower and inverting unity-gain amplifiers. The exceptionally fast settling time characteristics shown in Fig.18 are largely due to the high combination of high gain and wide bandwidth of the CA3140.

INPUT CIRCUIT CONSIDERATIONS

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

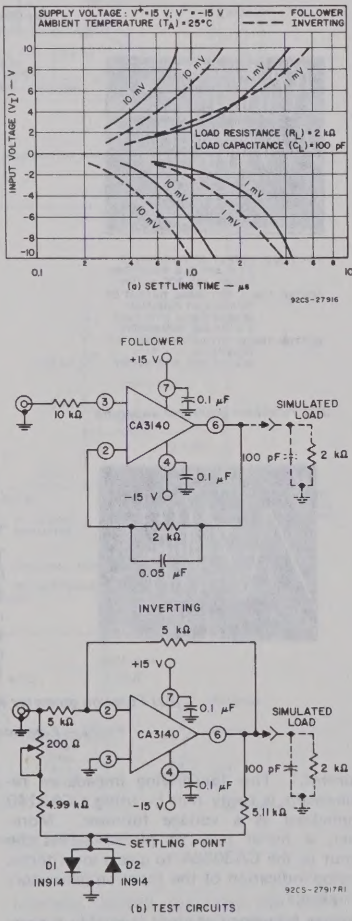
The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig.19 shows typical input-terminal current versus ambient temperature for the CA3140.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Fig.14 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetircal, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar a transistor input stage.

SUPER SWEEP FUNCTION GENERATOR

A function generator having a wide tuning range is shown in Fig.21. The 1,000,000/1 adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting read-out amplifier of the tri-



(b) TEST CIRCUITS

Fig.17 — Input voltage vs settling time.

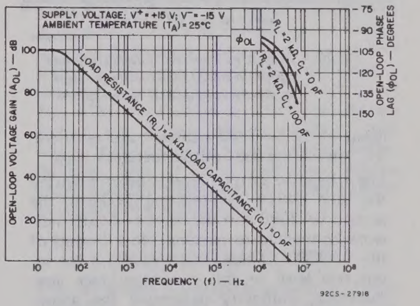


Fig.18 — Open-loop voltage gain and phase lag vs frequency.

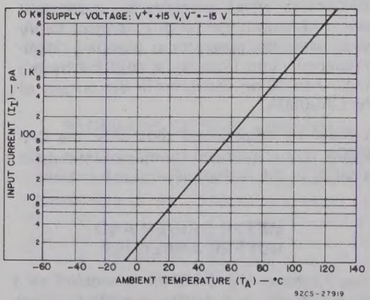


Fig.19 — Input current vs ambient temperature.

angular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

Buffered triangular output signals are then applied to a second CA3080 functioning as a high-speed hysteresis switch. Output from the switch is returned directly back to the input of the CA3080A current source, thereby, completing the positive feedback loop.

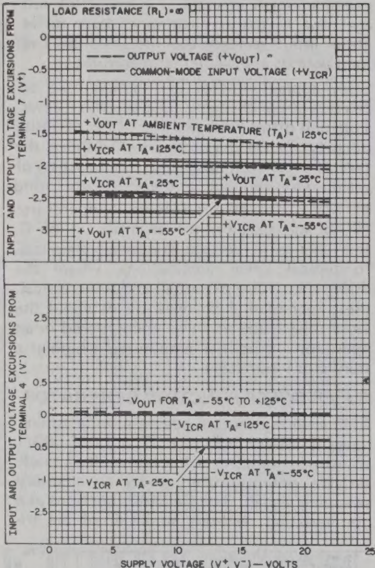


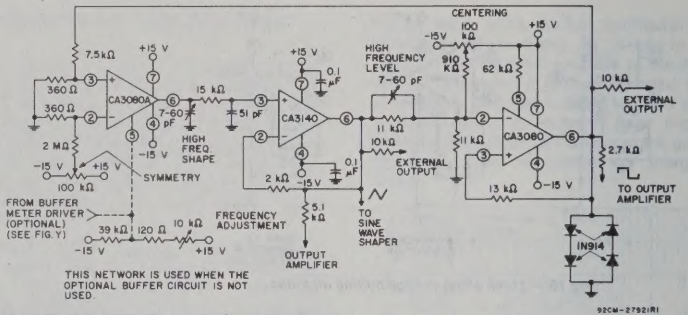
Fig.20 — Output-voltage-swing capability and common-mode input-voltage range vs supply voltage and temperature.

The triangular output level is determined by the four 1N914 level-limiting diodes of the second CA3080 and the resistor-divider network connected to terminal No.2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

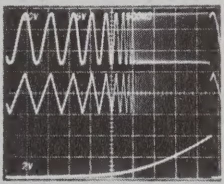
Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High-frequency ramp linearity is adjusted by the single 7-to-60 pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA-3080A is characterized for maximum output linearity in the current-generator function.

METER DRIVER AND BUFFER AMPLIFIER



(a) Circuit

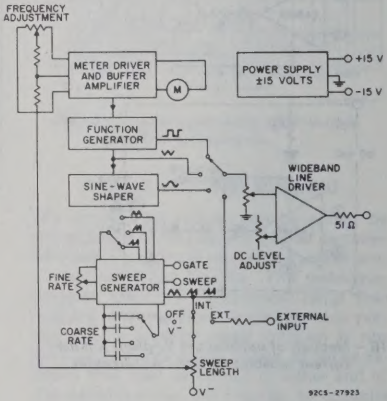


TOP TRACE: OUTPUT AT JUNCTION OF 2.7 Ω AND 51 Ω RESISTORS 5 V/DIV AND 500 ms/DIV

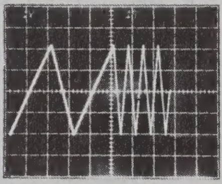
CENTER TRACE: EXTERNAL OUTPUT OF TRIANGULAR FUNCTION GENERATOR 2 V/DIV AND 500 ms/DIV

BOTTOM TRACE: OUTPUT OF "LOG" GENERATOR 10 V/DIV AND 500 ms/DIV

(b1) Function generator sweeping



(c) Interconnections



1V/DIV and 1 sec/DIV

Three tone test signals, highest frequency ≥ 0.5 MHz. Note the slight assymmetry at the three-second/cycle signal. This assymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100-pA level.

(b2) Function generator with fixed frequencies

Fig.21 — Function generator.

Fig. 22 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA-3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60-mV change in the applied voltage, V_{ABC} (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360-mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To

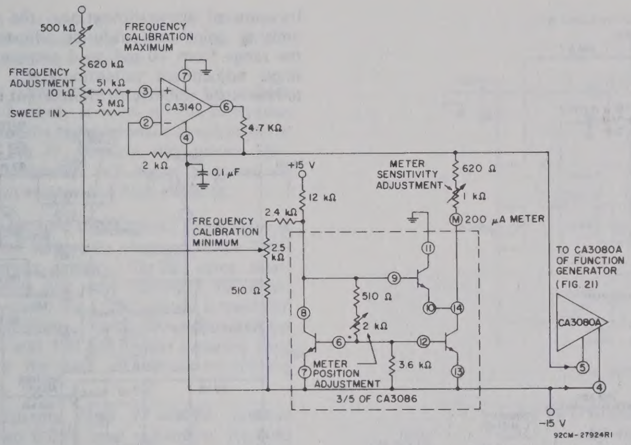

500 kΩ
FREQUENCY CALIBRATION MAXIMUM
620 kΩ
FREQUENCY ADJUSTMENT 10 kΩ
51 kΩ
3 MΩ
SWEEP IN
CA3140
4.7 KΩ
2 kΩ
0.1 μF
+15 V
12 kΩ
2.4 kΩ
FREQUENCY CALIBRATION MINIMUM
2.5 kΩ
510 Ω
METER SENSITIVITY ADJUSTMENT
620 Ω
1 kΩ
200 μA METER
510 Ω
2 kΩ
3.6 kΩ
METER POSITION ADJUSTMENT
3/5 OF CA3086
TO CA3080A OF FUNCTION GENERATOR (FIG. 21)
CA3080A
-15 V
92CM-27924R1

Fig. 22 – Meter driver and buffer amplifier.

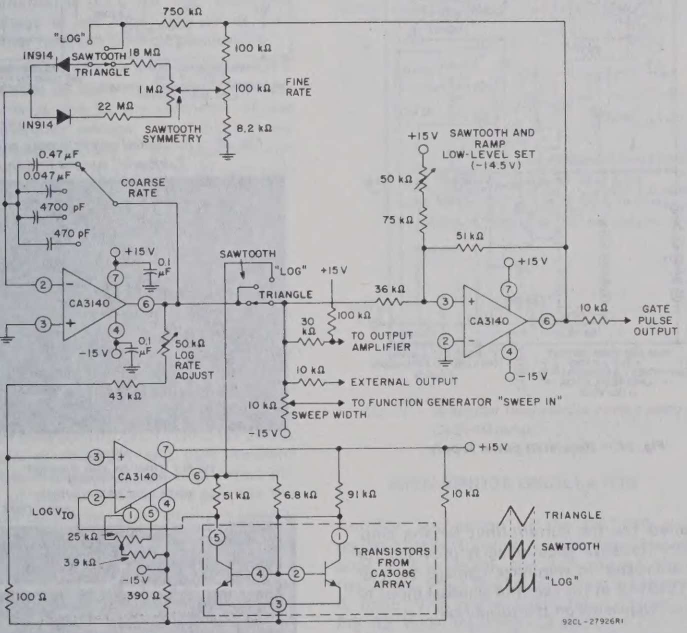


Fig. 24 – Sweeping generator.

establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necesary.

Two adjustments are used for the meter. The meter sensitivity control sets the meter-scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects 1/6 of full scale for each decade change in frequency.

SINE-WAVE SHAPER

The circuit shown in Fig. 23 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero-crossing slope is established by the 10-kΩ potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1-kΩ resistor and 10-kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage-follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

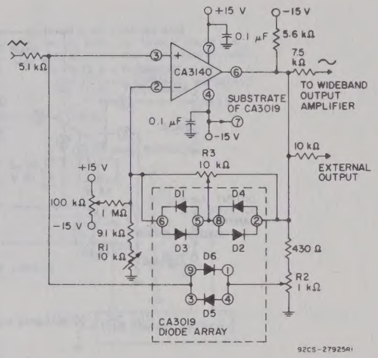


Fig. 23 – Sine-wave shaper.

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine-wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary

SWEEPING GENERATOR

Fig. 24 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

WIDEBAND OUTPUT AMPLIFIER

Fig. 25 shows a high-slew-rate, wideband amplifier suitable for use as a 50-ohm transmission-line driver. This circuit, when used in conjunction with the function generator and sine-wave shaper circuits shown in Figs. 21 and 23 provides 18 volts peak-to-peak output open-circuited, or 9 volts peak-to-peak output when terminated in 50 ohms. The slew rate required of this amplifier is 28 volts/μs (18 volts peak-to-peak × π × 0.5 MHz).

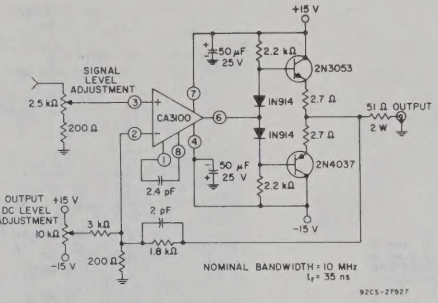


Fig. 25 – Wideband output amplifier.

POWER SUPPLIES

High input-impedance, common-mode capability down to the negative supply and high output-drive current capability are key factors in the design of wide-range output-voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0 to 24 volts. Unlike many regulator systems using comparators having a bipolar transistor-input stage, a high-impedance reference-voltage divider from a single supply can be used in connection with the CA3140 (see Fig. 26).

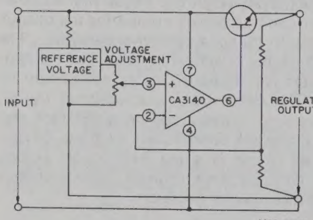


Fig. 26 – Basic single-supply voltage regulator showing voltage-follower configuration.

Essentially, the regulators, shown in Figs. 27 and 28, are connected as non-inverting power operational amplifiers with a gain of 3.2. An 8-volt reference input yields a maximum output voltage slightly greater than 25 volts. As a voltage follower, when the reference input goes to 0 volts the output will be 0 volts. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CE}sat) across the output of the CA3140 (see Fig.13). This saturation voltage level may indeed set the lowest voltage obtainable.

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply-rail.

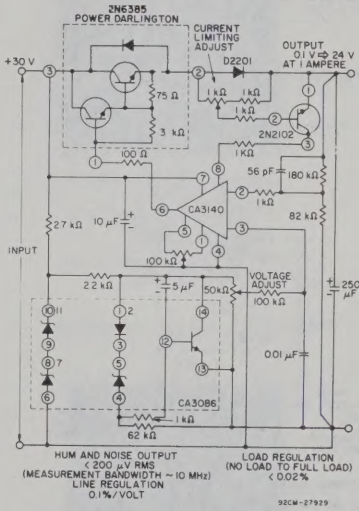


Fig. 27 – Regulated power supply.

Figs. 27 and 28, show circuits in which a D2201 high-speed diode is used for the current sensor. This diode was chosen for its slightly higher forward-voltage drop characteristic thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1 ampere at 1 volt forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small-signal reference amplifier in the proximity of the current-sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode.

In spite of those limitations, the current limiting point can easily be adjusted over the range from 10 mA to 1 ampere with a single adjustment potentiometer. If the temperature stability of the current-limiting

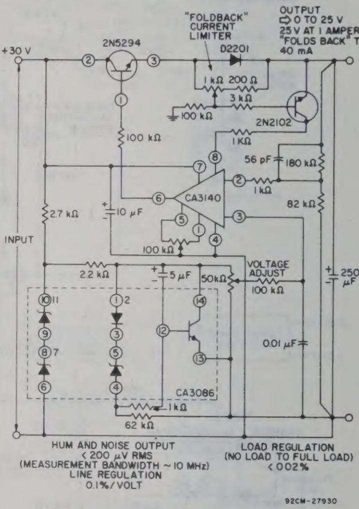
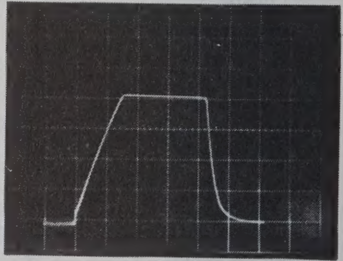


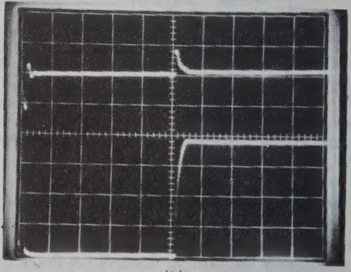
Fig. 28 – Regulated power supply with "foldback" current limiting.



(a)

SUPPLY TURN-ON AND TURN-OFF CHARACTERISTICS
(5 VOLTS / DIV AND ~1 s/DIV.)

92CS-27882



(b)

TRANSIENT RESPONSE
TOP TRACE : OUTPUT VOLTAGE (200 mV/DIV AND 5µs/DIV)
BOTTOM TRACE : COLLECTOR OF LOAD SWITCHING TRANSISTOR, LOAD = 1 AMPERE (5 VOLTS/DIV AND 5µs/DIV)

92CS-27881

Fig. 29 – Waveforms of dynamic characteristics of power supply currents shown in Figs. 29 and 30.

system is a serious consideration, the more usual current-sampling resistor-type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series-pass element for the conventional current-limiting system, Fig. 27, because high-power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat-sink VERSAWATT transistor is used as the series-pass element in the foldback current system, Fig.28, since dissipation levels will only approach 10 watts. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3 kΩ and 100 kΩ divider network connected to the base of the current-sensing transistor.

Both regulators, Figs. 27 and 28, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200 µV as read with a meter having a 10-MHz bandwidth.

Fig.31 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn-on rise is due to the slow rate of rise of the reference voltage. Fig. 29 (b) shows the transient response of the regulator with the switching of a 20-Ω load at 20 volts output.

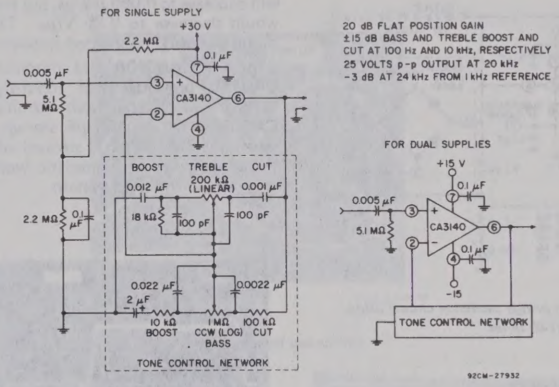
TONE CONTROL CIRCUITS

High-slew-rate, wide-bandwidth, high-output voltage capability and high input impedance are all characteristics required of tone-control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figs. 30 and 31.

The first circuit, shown in Fig. 31, is the Baxandall tone-control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small-size capacitors, as well as reduced load of the driving stage.

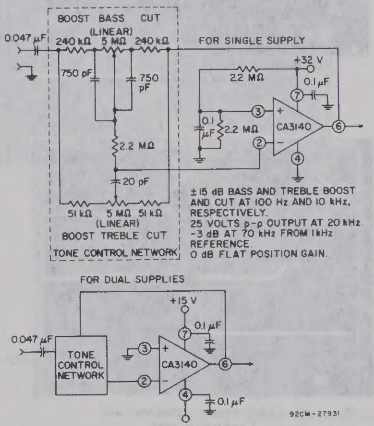
Bass treble boost and cut are ± 15 dB at 100 Hz and 10 kHz, respectively. Full peak-to-peak output is available up to at least 20 kHz due to the high slew rate of the CA3140. The amplifier gain is −3 dB down from its "flat" position at 70 kHz.

Fig. 30 shows another tone-control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20-dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No.3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L, Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No.3, August, 1972.



20 dB FLAT POSITION GAIN
±15 dB BASS AND TREBLE BOOST AND CUT AT 100 Hz AND 10 kHz, RESPECTIVELY
25 VOLTS p-p OUTPUT AT 20 kHz
−3 dB AT 24 kHz FROM 1 kHz REFERENCE

Fig. 30 — Tone control circuit using CA3130 series (20-dB midband gain).



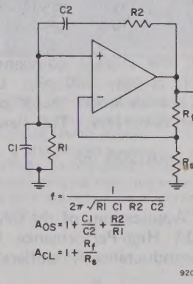
±15 dB BASS AND TREBLE BOOST AND CUT AT 100 Hz AND 10 kHz, RESPECTIVELY.
25 VOLTS p-p OUTPUT AT 20 kHz
−3 dB AT 70 kHz FROM 1kHz REFERENCE
0 dB FLAT POSITION GAIN.

Fig. 31 — Baxandall tone control circuit using CA3140 series.

WIEN BRIDGE OSCILLATOR

Another application of the CA3140 that makes excellent use of its high input-impedance, high-slew-rate, and high-voltage qualities is the Wien Bridge sine-wave oscillator. A basic Wien Bridge oscillator is shown in Fig. 32. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/2\pi RC$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain-bandwidth product of the CA3140.

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_s, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_s is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.



$$f = \frac{1}{2\pi\sqrt{R1\ C1\ R2\ C2}}$$

$$A_{OS} = 1 + \frac{C1}{C2} + \frac{R2}{R1}$$

$$A_{CL} = 1 + \frac{R_f}{R_s}$$

Fig. 32 — Basic Wien bridge oscillator circuit using an operational amplifier.

Fig. 33 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_f of Fig. 32). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1-µF polycarbonate capacitors and 22 MΩ for the frequency determining network, the operating frequency is 0.007 Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180 kHz will reach a slew rate of approximately 9 volts/µs when its amplitude is 16 volts peak-to-peak.

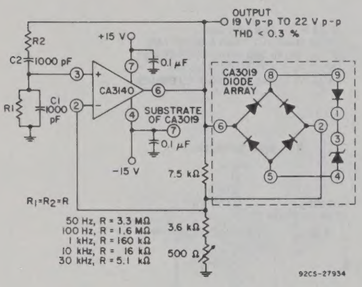


Fig. 33 – Wien bridge oscillator circuit using CA3140 series.

SIMPLE SAMPLE-AND-HOLD SYSTEM

Fig. 34 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.* System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2 kΩ and 30 pF is shown in the schematic.

In this circuit, the storage compensation capacitance (C_1) is only 200 pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate $\frac{dv}{dt} = \frac{i}{c} = 0.5$ mA/200 pF = 2.5 V/µs.

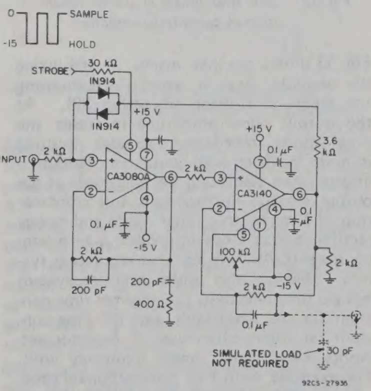
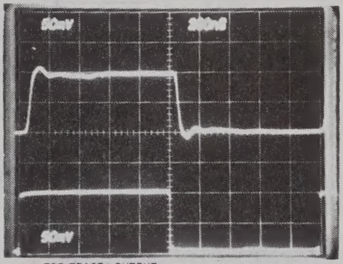
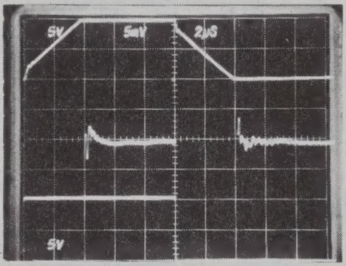


Fig. 34 – Sample- and hold circuit.

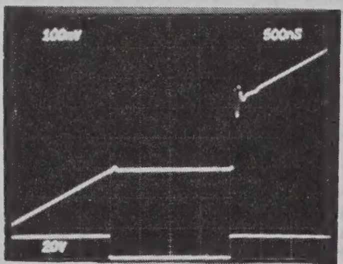
Pulse "droop" during the hold interval is 170 pA/200 pF which is = 0.85 µV/µs; (i.e., 170 pA/200 pF). In this case, 170 pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000 pF, the "hold-droop" rate will decrease to 0.085 µV/µs, but the slew rate would decrease to 0.25 V/µs. The parallel diode network connected between terminal 3 of the CA3080A and terminal 6 of the CA3140 prevents large input-signal feed-through across the input terminals of the CA3080A to the 200 pF storage capacitor when the CA3080A is strobed off. Fig. 35 shows dynamic characteristic waveforms of this sample-and-hold system.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)
92CS-27883



LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 2µs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5V/DIV. AND 2µs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5mV/DIV. AND 2µs/DIV.)
92CS-27884



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL
(20 V/DIV. AND 500 ns/DIV.)
92CS-27885

Fig. 35 – Sample- and hold system dynamic characteristics waveforms.

CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA3140 makes it ideal for use in current-amplifier applications such as the one shown in Fig. 36.● In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 µA; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

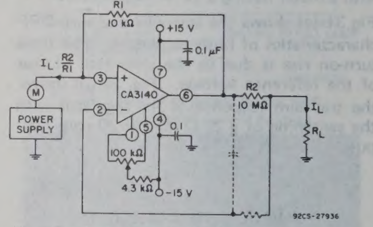


Fig. 36 – Basic current amplifier for low-current measurement systems.

Fig. 37 shows a single-supply, absolute-value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No.6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 37 is satisfied, the full-wave output is symmetrical.

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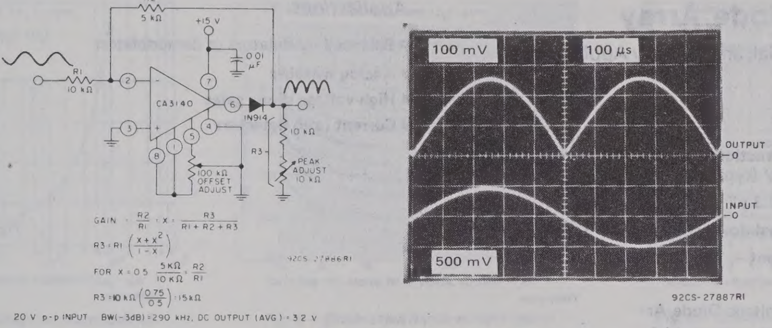
* ICAN-6668 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

● "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 – "Negative Immittance Converter Circuits".



$$\text{GAIN} = \frac{R2}{R1} = X = \frac{R3}{R1 + R2 + R3}$$

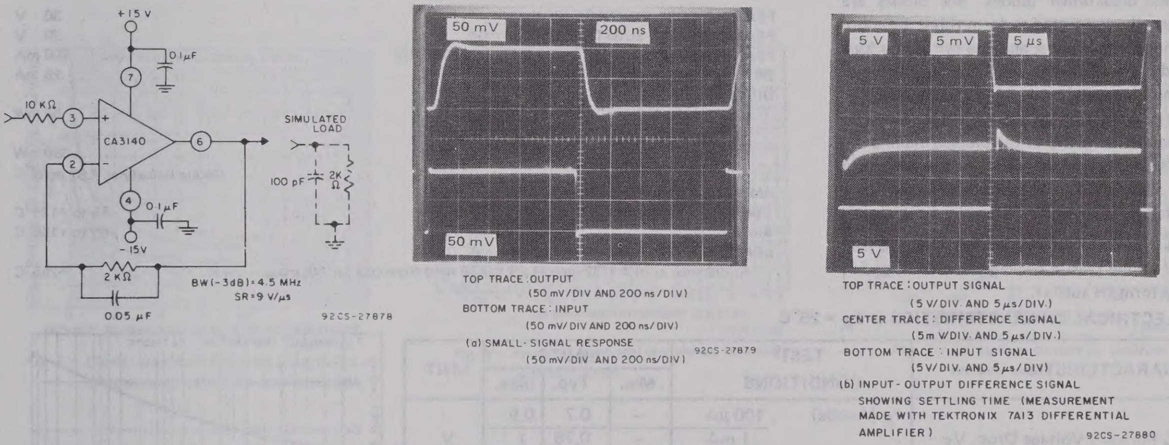
$$R3 = R1\left(\frac{X + X^2}{1 - X}\right)$$

$$\text{FOR } X = 0.5 \quad \frac{5\,\text{K}\Omega}{10\,\text{K}\Omega} = \frac{R2}{R1}$$

$$R3 = 10\,\text{k}\Omega\left(\frac{0.75}{0.5}\right) = 15\,\text{k}\Omega$$

20 V p-p INPUT BW(−3dB) = 290 kHz, DC OUTPUT (AVG) = 3.2 V

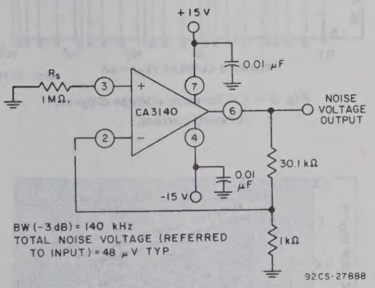
Fig. 37 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.



TOP TRACE: OUTPUT
(50 mV/DIV AND 200 ns/DIV)
BOTTOM TRACE: INPUT
(50 mV/DIV AND 200 ns/DIV)
(a) SMALL-SIGNAL RESPONSE
(50 mV/DIV AND 200 ns/DIV)

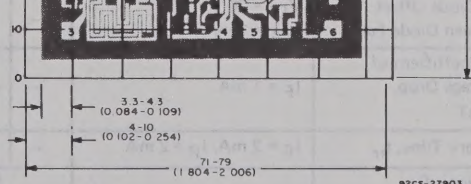
TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 5 μs/DIV.)
CENTER TRACE: DIFFERENCE SIGNAL
(5 mV/DIV. AND 5 μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5 V/DIV. AND 5 μs/DIV)
(b) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)

Fig. 38 — Split-supply voltage-follower test circuit and associated waveforms.



BW(−3dB) = 140 kHz
TOTAL NOISE VOLTAGE (REFERRED TO INPUT) = 48 μV TYP.

Fig. 39 — Test circuit amplifier (30-dB gain) used for wideband noise measurement.



CA3140H Chip

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3141E

High-Voltage Diode Array

For Commercial, Industrial, and Military Applications

Features:

- **Matched monolithic construction — V_F for each diode pair matched to within 0.55 mV (typ.) at I_F = 1 mA**
- **Low diode capacitance — 0.3 pF (typ.) at V_R = 2 V**
- **High diode-to-substrate breakdown voltage — 30 V (min.)**
- **Low reverse (leakage) current — 100 nA (max.)**

Applications:

- **Balanced modulators or demodulators**
- **Analog switches**
- **High-voltage diode gates**
- **Current ratio detectors**

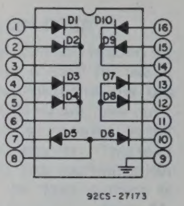


Fig. 1 — Terminal assignment.

The RCA-CA3141E High-Voltage Diode Array consists of ten general-purpose high-reverse-breakdown diodes. Six diodes are internally connected to form three common-cathode diode pairs, and the remaining four diodes are internally connected to form two common-anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141E extremely useful for a wide variety of applications in communications and switching systems.

The CA3141E is supplied in the 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute Maximum Values*

PEAK INVERSE VOLTAGE (PIV)	30 V
PEAK DIODE-TO-SUBSTRATE VOLTAGE	30 V
PEAK FORWARD SURGE CURRENT [I_F (SURGE)]	100 mA
DC FORWARD CURRENT (I_F)	25 mA
DISSIPATION:	
Any one diode unit	50 mW
Total Package:	
Up to 55°C	650 mW
For $T_A > 55^\circ$C	Derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max.	+265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNIT
			Min.	Typ.	Max.	
DC Forward Voltage Drop, V_F	I_F (Anode)	100 µA	–	0.7	0.9	V
		1 mA	–	0.78	1	
		10 mA	–	0.93	1.2	
DC Reverse Breakdown Voltage, $V_{(BR)R}$	I_F = −10 µA		30	50	–	V
DC Breakdown Voltage Between Any Diode and Substrate, $V_{(BR)DI}$	I_{DI} = 10 µA		30	50	–	V
DC Reverse (Leakage) Current, I_R	V_F = −20 V		–	–	100	nA
DC Reverse (Leakage) Current Between Any Diode and Substrate, I_{DI}	V_{DI} = 20 V		–	–	100	nA
Magnitude of Diode Offset Voltage Between Diode Pairs	V_{DI} = 20 V I_{FA} = 1 mA		–	0.55	–	mV
Temperature Coefficient of Forward Voltage Drop, $\Delta V_F/\Delta T$	I_F = 1 mA		–	−1.5	–	mV/°C
Reverse Recovery Time, t_{rr}	I_F = 2 mA, I_R = 2 mA		–	50	–	ns
Diode Capacitance, C_D			See Fig. 5			pF
Diode Anode-to-Substrate Capacitance, C_{DAI}			See Fig. 6			pF
Diode Cathode-to-Substrate Capacitance, C_{DCI}			See Fig. 7			pF
Magnitude of Cathode-to-Anode Current Ratio, $\|I_{FC}/I_{FA}\|$	I_{FA} = 1 mA, V_{DS} = 10 V		0.9	0.96	–	

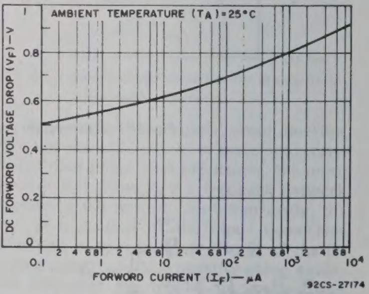


Fig. 2 — DC forward voltage drop vs. forward current.

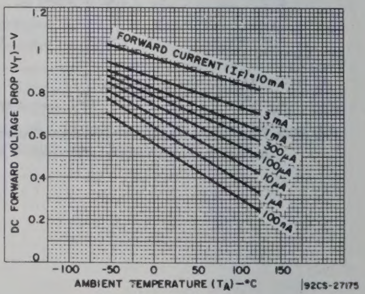


Fig. 3 — DC forward voltage drop vs. ambient temperature.

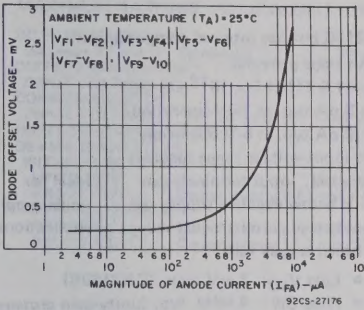


Fig. 4 — Diode offset voltage vs. magnitude of anode current.

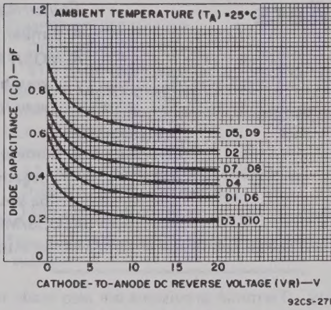


Fig. 5 — Diode capacitance vs. cathode-to-anode reverse voltage.

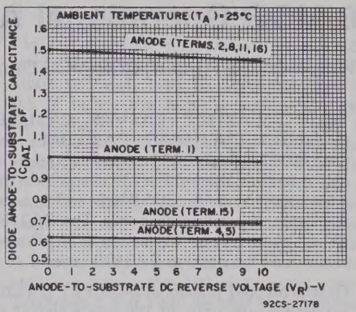


Fig. 6 — Diode anode-to-substrate capacitance vs. reverse voltage.

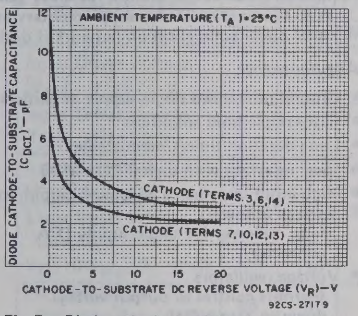


Fig. 7 — Diode cathode-to-substrate capacitance vs. cathode-to-substrate DC reverse voltage.

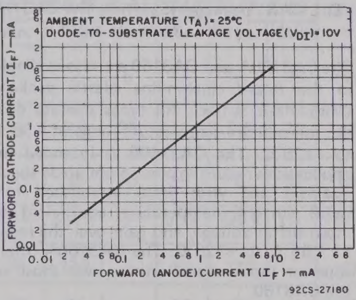


Fig. 8 — Forward (cathode) current vs. forward (anode) current.

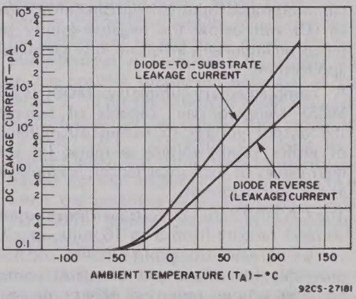


Fig. 9 — DC leakage current vs. ambient temperature.

CA3160, CA3160A, CA3160B Types

BiMOS Operational Amplifiers

With MOS/FET Input, COS/MOS Output

The RCA-CA3160T, CA3160S, CA3160E; CA3160AT, CA3160AS, CA3160AE; and CA3160BT, CA3160BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip. The CA3160 series circuits are frequency-compensated versions of the popular CA3130 series.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3160 Series circuits operate at supply voltages ranging from 5 to 16 volts, or +2.5 to +8 volts when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3160 series is supplied in standard 8-lead TO-5-style packages (T suffix) and 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" packages (S suffix). The CA3160 is available in chip form (H suffix).

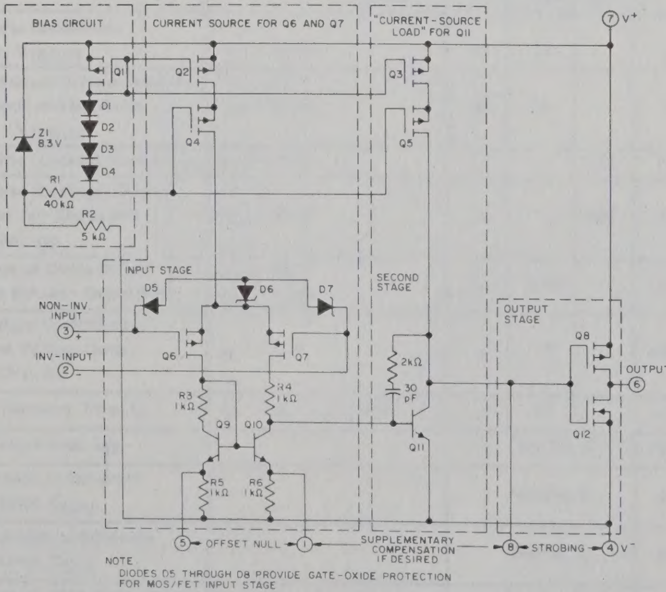
The CA3160A and CA3160 are also available in the 8-lead dual-in-line plastic package (Mini-DIP-E suffix). All types operate over the full military-temperature range of −55°C to +125°C. The CA3160B is intended for applications requiring preminium-grade specifications and with limits established for: input current, temperature coefficient of input-offset voltage, and gain over the range of −55°C to +125°C. The CA3160A offers superior input characteristics over those of the CA3160.

Features:

- **Similar to CA3130 but has internal compensation**
- **MOS/FET input stage provides:**
  - **very high Z_I = 1.5 TΩ (1.5×10^{12} Ω) typ.**
  - **very low I_I = 5 pA typ. at 15-V operation**
  - **2 pA typ. at 5-V operation**
- **Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail** } **Ideal for single-supply applications**
- **COS/MOS output stage permits signal swing to either (or both) supply rails**
- **Low V_{IO}: 2 mV max. (CA3160B)**
- **Wide BW: 4 MHz typ. (unity-gain crossover)**
- **High SR: 10 V/μs typ. (unity-gain follower)**
- **High output current (I_O): 20 mA typ.**
- **High A_{OL}: 320,000 (110 dB) typ.**
- **Internal phase compensation for unity gain (With terminal access for supplementary external phase compensation network if desired)**

Applications:

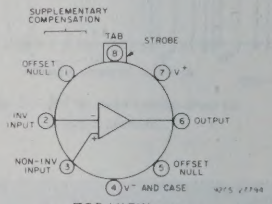
- **Ground-referenced single-supply amplifiers**
- **Fast sample-hold amplifiers**
- **Long-duration timers/monostables**
- **Ideal interface with digital COS/MOS**
- **High-input-impedance wideband amplifiers**
- **Voltage followers**
  - **(e.g., follower for single-supply D/A converter)**
- **Voltage regulators**
  - **(permits control of output voltage down to zero volts)**
- **Wien-Bridge oscillators**
- **Voltage-controlled oscillators**
- **Photo-diode sensor amplifiers**



NOTE
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE

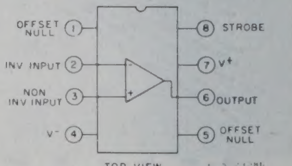
92CM-28536

Fig. 1 – Schematic diagram of the CA3160 Series.



TOP VIEW

S and T Suffixes



TOP VIEW

E Suffix

CA3160 Series devices have an on-chip frequency-compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

Fig.2 – Functional diagrams of the CA3160 Series.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) . . . . 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE . . . . ±8 V
COMMON-MODE DC
INPUT VOLTAGE . . . (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT . . . . 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK –
UP TO 55°C . . . . 630 mW
ABOVE 55°C . . . . Derate linearly 6.67 mW/°C
WITH HEAT SINK –
AT 125°C . . . . 418 mW
BELOW 125°C . . . Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (All Types) . . . . −55 to +125°C
STORAGE (All Types) . . . . . −65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION* . . . . INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 MM) FROM CASE
FOR 10 SECONDS MAX. . . . . +265°C

---

*Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS									Units
	CA3160B (T, S)			CA3160A (T, S, E)			CA3160 (T, S, E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\lvert V_{IO} \rvert$, $V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	6	15	mV
Input Offset Current, $\lvert I_{IO} \rvert$, $V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 V_{p-p}, R_L=2 kΩ	100	110	–	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	86	100	–	80	95	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V
Maximum Output Voltage: At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	12	13.3	–	V
At R_L=2 kΩ V_{OM}^-	–	0.002	0.01	–	0.002	0.01	–	0.002	0.01	
At R_L = ∞ V_{OM}^+	14.99	15	–	14.99	15	–	14.99	15	–	
At R_L = ∞ V_{OM}^-	–	0	0.01	–	0	0.01	–	0	0.01	
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	12	20	45	
Supply Current, I^+: V_O=7.5 V, R_L = ∞	–	10	15	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	–	2	3	
Input Current, I_I*	–	Fig.11	15	–	Fig.11	–	–	Fig.11	–	nA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	5	15	–	6	–	–	8	–	μV/°C
Large-Signal Voltage Gain, A_{OL}*	50 k	320 k	–	–	320 k	–	–	320 k	–	V/V
	94	110	–	–	110	–	–	110	–	dB

* T_A = −55 to +125°C, $V^{\pm}$= ± 7.5 V (I_I and $\Delta V_{IO}/\Delta T$), V_O = 10 V_{p-p} and R_L = 2 kΩ (A_{OL}).

CIRCUIT DESCRIPTION

Fig.3 is a block diagram of the CA3160 series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3160 series circuits are ideal for single-supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in Fig.3, provide the total gain of the CA3160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages – The circuit of the CA3160 is shown in Fig.1. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-Stage – Most of the voltage gain in the CA3160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30-pF capacitor and 2-kΩ resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit – At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS $V^+ = +7.5$ V $V^- = -7.5$ V $T_A = 25^oC$ (Unless Otherwise Specified)		CA3160B (T, S)	CA3160A (T, S, E)	CA3160 (T, S, E)	UNITS
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1		±22	±22	±22	mV
Input Resistance, R_I			1.5	1.5	1.5	TΩ
Input Capacitance, C_I	f = 1 MHz		4.3	4.3	4.3	pF
Equivalent Input Noise Voltage, e_n	BW= 0.2 MHz	R_S=1 MΩ	40	40	40	μV
		R_S=10MΩ	50	50	50	
Equivalent Input Noise Voltage, e_n	R_S= 100 Ω	1 kHz	72	72	72	nV/$\sqrt{Hz}$
		10 kHz	30	30	30	
Unity Gain Crossover Frequency, f_T			4	4	4	MHz
Slew Rate, SR:			10	10	10	V/μs
Transient Response: Rise Time, t_r	C_L = 25 pF R_L = 2 kΩ (Voltage Follower)		0.09	0.09	0.09	μs
Overshoot			10	10	10	%
Settling Time (4 $V_{p\text{-}p}$ Input to <0.1%)			1.8	1.8	1.8	μs

CHARACTERISTIC	TEST CONDITIONS $V^+ = 5$ V $V^- = 0$ V $T_A = 25^oC$ (Unless Otherwise Specified)	CA3160B (T, S)	CA3160A (T, S, E)	CA3160 (T, S, E)	UNITS
Input Offset Voltage, V_{IO}		1	2	6	mV
Input Offset Current, I_{IO}		0.1	0.1	0.1	pA
Input Current, I_I		2	2	2	pA
Common-Mode Rejection Ratio, CMRR		100	90	80	dB
Large-Signal Voltage Gain, A_{OL}	V_O = 4 $V_{p\text{-}p}$ R_L = 5 kΩ	100 k	100 k	100 k	V/V
		100	100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, $R_L = \infty$	300	300	300	μA
	V_O = 2.5 V, $R_L = \infty$	500	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V

CIRCUIT DESCRIPTION (cont'd)

circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage – The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig.6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

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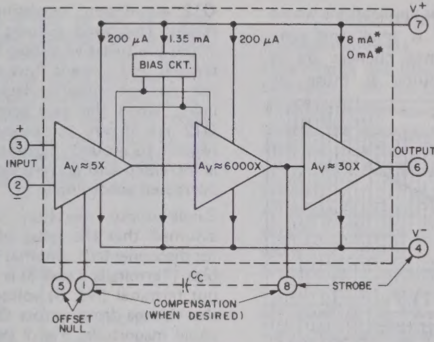
† For general information on the characteristics of COS/MOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array".



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
* WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
# WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

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Fig. 3 — Block diagram of the CA3160 Series.

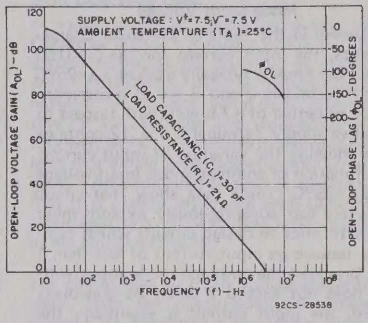

Fig.4 — Open-loop voltage gain and phase shift vs. frequency for various values of C_L and R_L.

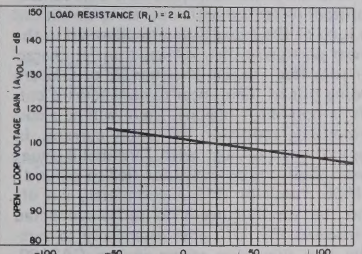

Fig.5 — Open-loop gain vs. temperature.

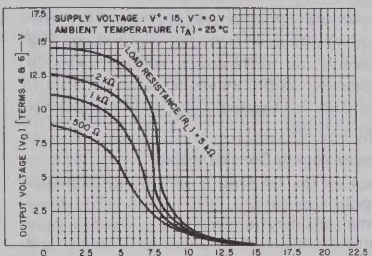

Fig.6 — Voltage transfer characteristics of COS/MOS output stage.

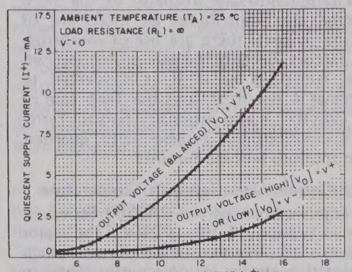

Fig.7 — Quiescent supply current vs. supply voltage.

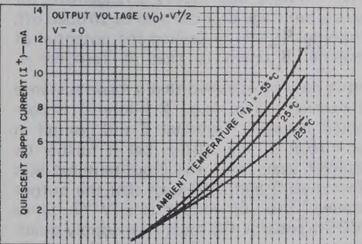

Fig.8 — Quiescent supply current vs. supply voltage at several temperatures.

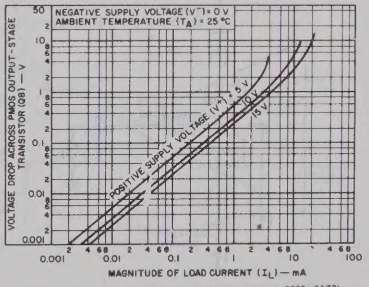

Fig.9 — Voltage across PMOS output transistor (Q8) vs. load current.

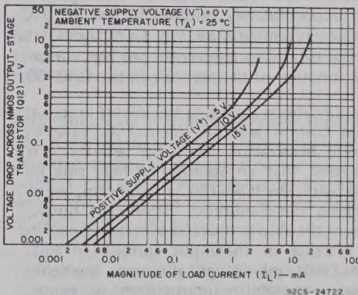

Fig.10 — Voltage across NMOS output transistor (Q12) vs. load current.

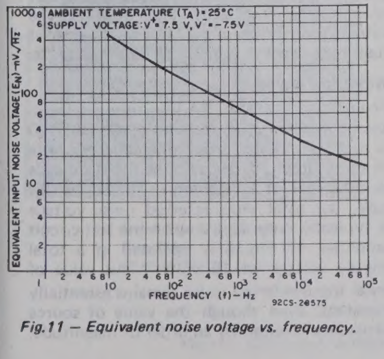

Fig.11 — Equivalent noise voltage vs. frequency.

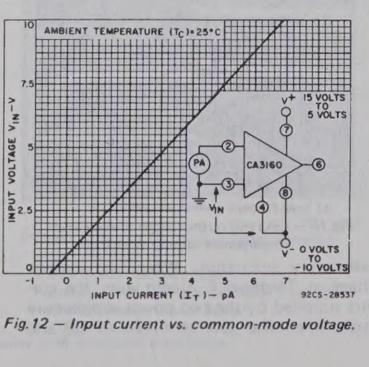

Fig.12 — Input current vs. common-mode voltage.

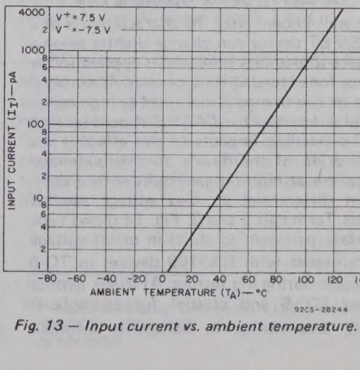

Fig. 13 — Input current vs. ambient temperature.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3160 Series Op-Amps is typically 5 pA at T_A=25°C when Terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 12 contains data showing the variation of input current as a function of common-mode input voltage at T_A=25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3160 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Input-Current Variation with Temperature

The input current of the CA3160 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 13 provides data on the typical variation of input bias current as a function of temperature in the CA3160.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Fig. 14 shows typical data pertinent to shifts in offset voltage encountered with CA3160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

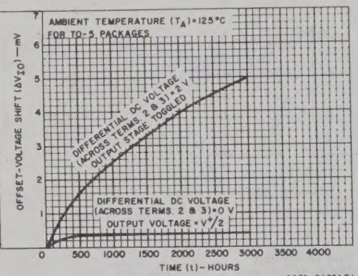

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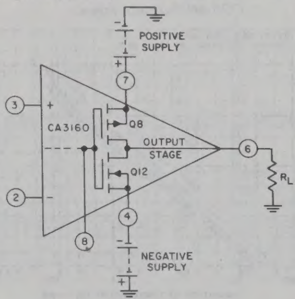
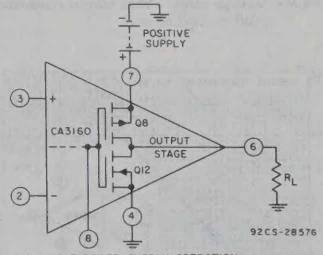
Fig. 14 – Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3160 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 15(a) and 15(b) show the CA3160 connected for both dual- and single-supply operation.



(a) DUAL POWER-SUPPLY OPERATION



(b) SINGLE POWER-SUPPLY OPERATION

Fig. 15 – CA3160 output stage in dual and single power-supply operation.

Dual-supply operation: When the output voltage at Terminal 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3160 operated under these conditions.

Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3160, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 15(a) shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L=\infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Terminal 6 and ground in the circuit of Fig. 15(b). Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3160 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 40 μV when the test-circuit amplifier of Fig. 16 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude.

This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

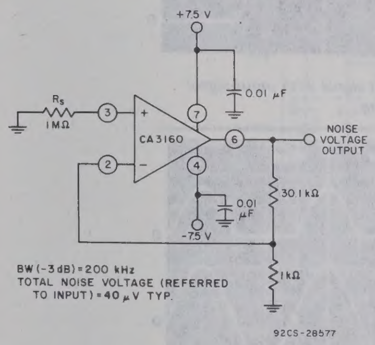


Fig.16 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3160, are particularly suited to service as voltage followers. Fig.17 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3160 in a split-supply configuration.

A voltage follower, operated from a single-supply, is shown in Fig.18 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig.18b with input-signal ramping. The waveforms in Fig.18c show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig.18c also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3160 in a single-supply voltage-follower application.

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.19. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig.19.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

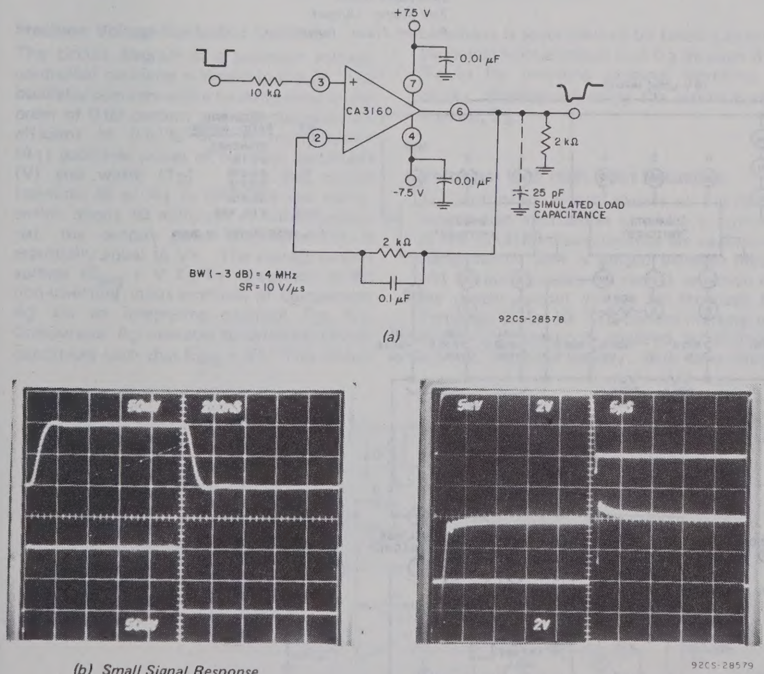
A single 15-volt supply provides a positive bus for the CA3160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Error-Amplifier in Regulated Power Supplies

The CA3160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Fig.20 uses a CA3160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero volts with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.



(b) Small Signal Response
Top Trace: Output
Bottom Trace: Input

(c) Input-Output Difference Signal Showing Settling Time
Top Trace: Output Signal
Center Trace: Difference Signal 5 mV/div
Bottom Trace: Input Signal

Fig.17 – Split-supply voltage follower with associated waveforms.

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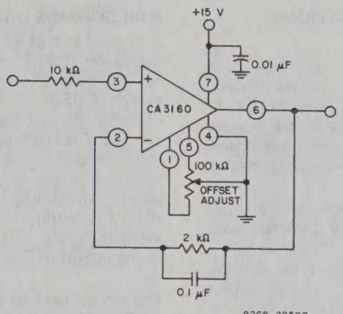
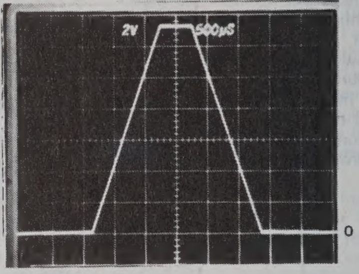
* "Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.

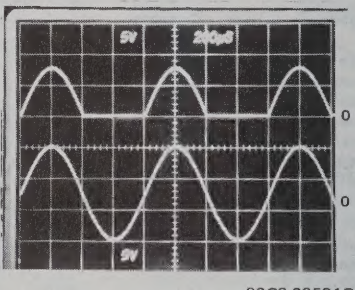


(a)

Fig.18 — Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig.9 in ICAN-6080.)



(b) Output signal with input-signal ramping.



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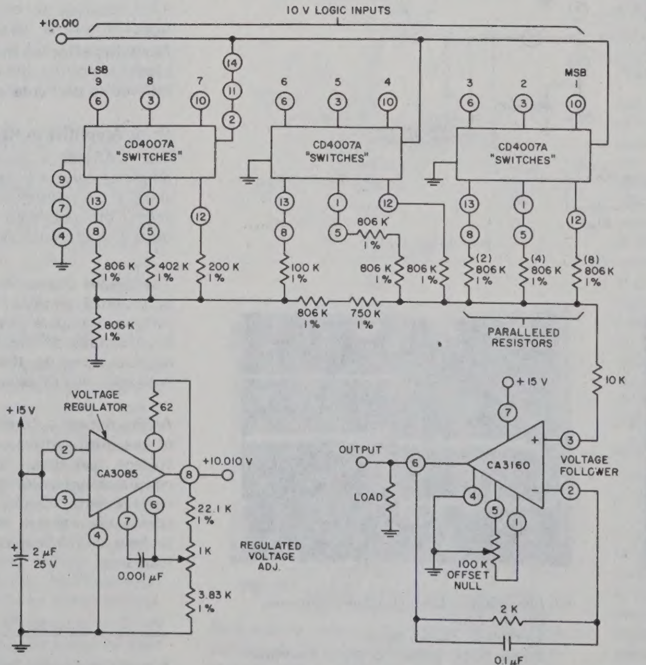
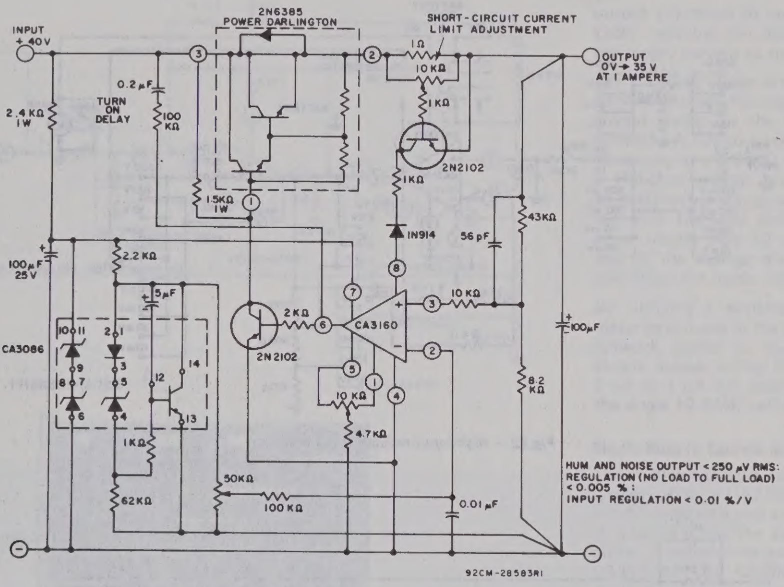
(c) Output-Waveform with Ground-Reference Sine-Wave Input
Top Trace: Output
Bottom Trace: Input



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

Fig.19 — 9-bit DAC using COS/MOS digital switches and CA3160.



HUM AND NOISE OUTPUT < 250 μV RMS:
REGULATION (NO LOAD TO FULL LOAD) < 0.005 % :
INPUT REGULATION < 0.01 %/V

Fig.20 – Voltage regulator circuit (0.1 to 35 V at 1 A).

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig.21. The oscillator operates with a tracking error in the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (terminal 6) of A_1 (a CA3130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{avg} = V\, T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{avg} = V1$. This circuit condition is accomplished by feeding an output signal from terminal 6 of A_2 through R_4, D_4 to the inverting terminal (terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig.22 illustrates an application in which a number of the CA3160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10 KΩ current-limiting resistor. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

Function Generator

A function generator having a wide tuning range is shown in Fig.23. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA3160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500 kHz and 1 MHz. Capacitors C4, C5, and the trimmer potentiometer in series with C5 maintain essentially constant (±10%) amplitude up to 1 MHz.

Staircase Generator

Fig.24 shows a staircase generator circuit utilizing three COS/MOS operational amplifiers. Two CA3130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA3160, is used as a linear staircase generator.

Picoammeter Circuit

Fig. 25 is a current-to-voltage converter configuration utilizing a CA3160 and CA3140 to provide a picoampere meter for ±3 pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA3160 at ground potential,

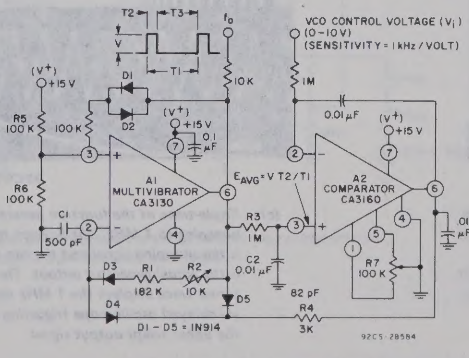


Fig.21 – Voltage-controlled oscillator.

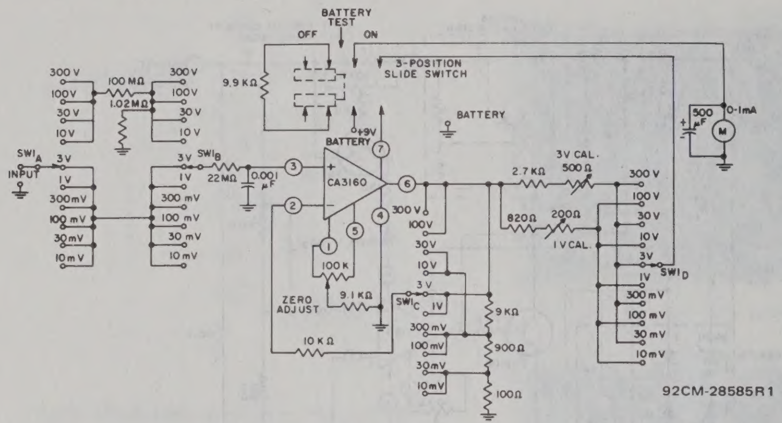
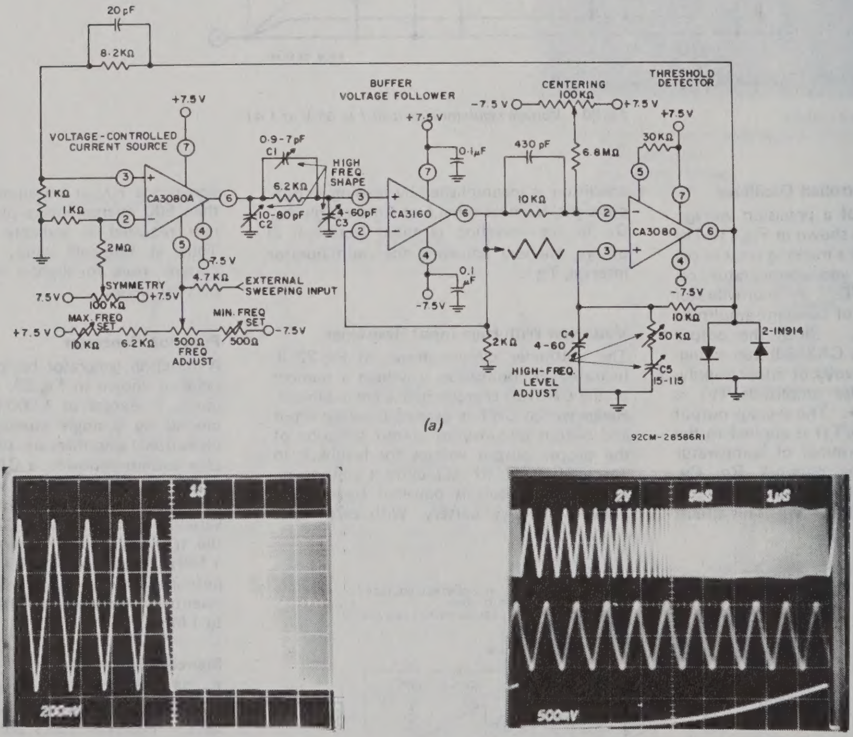


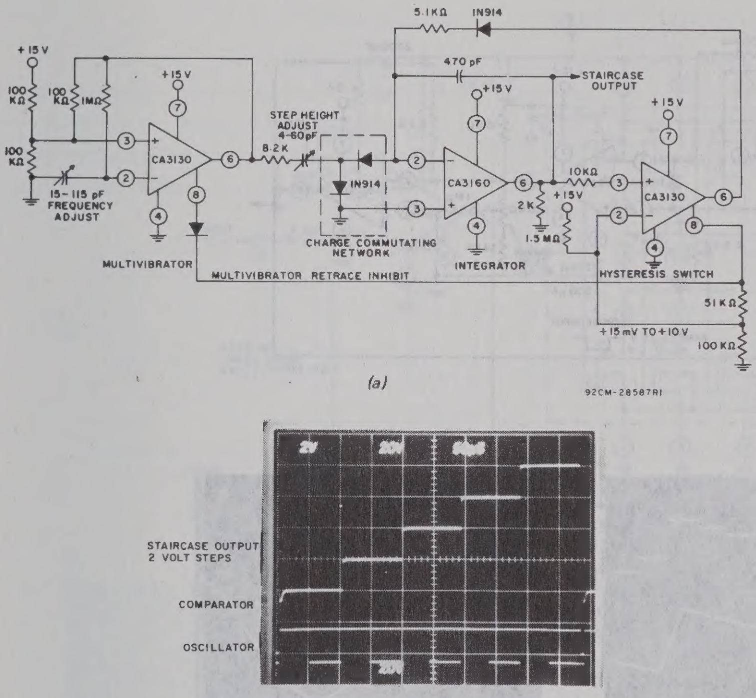
Fig.22 – High-input-resistance DC voltmeter.



(b) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.

(c) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Fig. 23 – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



(b) — Staircase Generator Waveform
Top Trace: Staircase Output
2 Volt Steps
Center Trace: Comparator
Bottom Trace: Oscillator

Fig. 24 — Staircase generator.

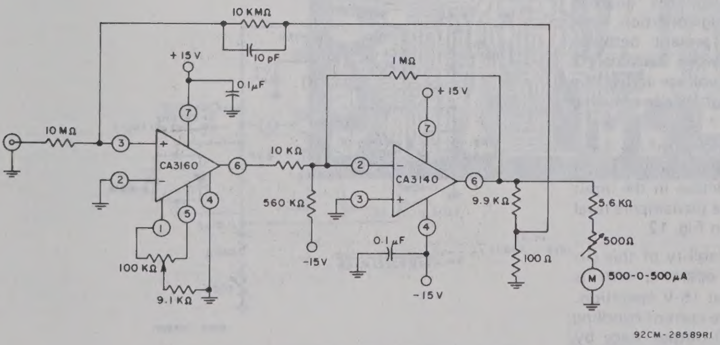


Fig.25 — Current-to-voltage converter to provide a picoammeter with ± 3 pA full-scale deflection.

output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9-KΩ resistor in series with a 100-ohm resistor sets the voltage at the 10-KMΩ resistor (in series with Terminal 3) to ±30 mV full-scale deflection. This 30-mV signal results from ±3 volts appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9 KΩ and 100-ohm network similar to that used in voltmeter circuit shown in Fig. 22, a current range of 3 pA to 1 nA full scale can be handled with the single 10-KMΩ resistor.

Single-Supply Sample-and-Hold System

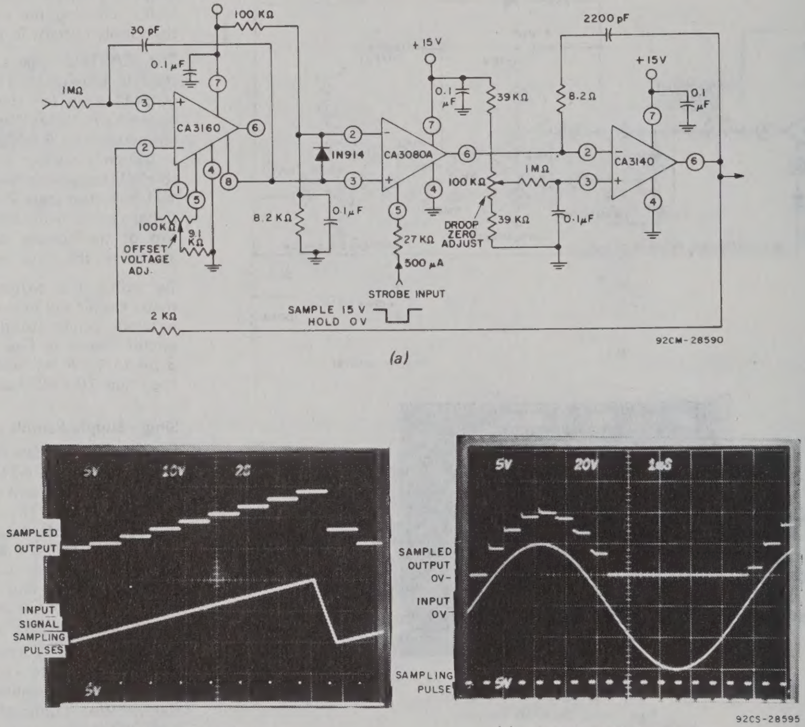
Fig. 26 shows a single-supply sample-and-hold system using a CA3160 to provide a high input impedance and an input-voltage range of 0 to 10 volts. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100-KΩ bias-voltage potentiometer on the positive input of the CA3080A. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320 mV at the amplifier bias circuit terminal (5) at least ± 100 pA of output current will be available.

Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA3160 is shown in Fig. 27. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1 volts. The 500-ohm potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA3160 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig.28, three COS/MOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA3160. In the Class A mode of CA3600E shown, a typical device consumes



(a)

(b) — Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses

(c) — Sample-and-hold waveform.
Top Trace: Sampled Output.
Center Trace: Input
Bottom Trace: Sampling Pulse

Fig. 26 — Single-supply sample-and-hold system—input 0-to-10 volts.

the CA3160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA3160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Fig. 12.

To further enhance the stability of this circuit, the CA3160 can be operated with its 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3160 output stage by about 2.5X.

The amplifier circuit in Fig. 28 employs feedback to establish a closed-loop gain of 20 dB. The typical large-signal-bandwidth (−3 dB) is 190 kHz.

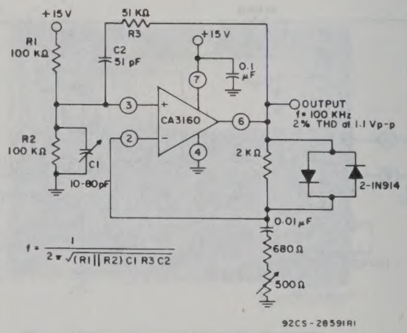


Fig.27 — Single-supply Wien Bridge oscillator.

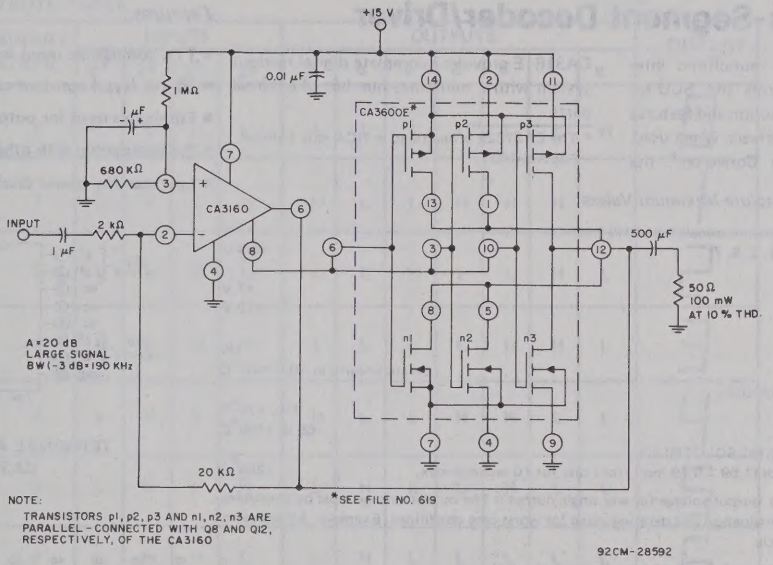
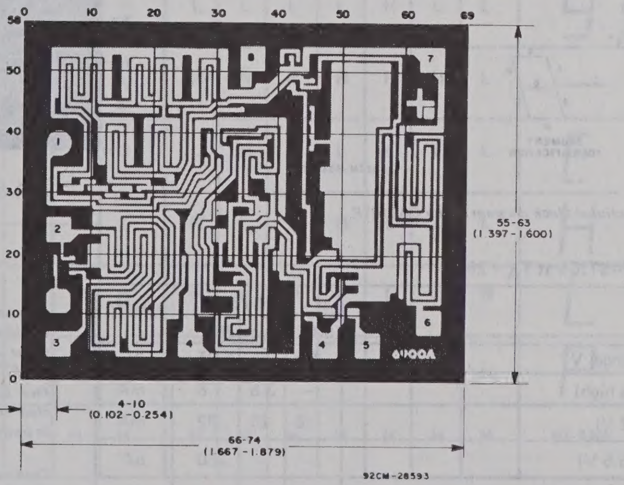


Fig.28 – COS/MOS transistor array (CA3600E) connected as power booster in the output stage of the CA3160.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photograph and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips the cleavage angles are 57^o instead of 90^o with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3161E

BCD-to-Seven-Segment Decoder/Driver

The RCA-CA3161E is a monolithic integrated circuit that performs the BCD-to-seven-segment decoding function and features constant-current segment drivers. When used with the CA3162E A/D Converter* the CA3161E provides a complete digital readout system with a minimum number of external parts.

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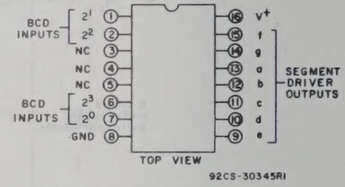
* The CA3162E is described in RCA data bulletin File No. 1080.

Features:

- TTL-compatible input logic levels
- 25-mA (typ.) constant-current segment outputs
- Eliminates need for output current-limiting resistors
- Pin compatible with other industry standard decoder
- Low standby power dissipation – 18 mW (typ.)



TERMINAL ASSIGNMENT
CA3161E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 1 and 10)	+7 V
INPUT VOLTAGE (terminals 1, 2, 6, 7)	+5.5 V
OUTPUT VOLTAGE:	
Output "Off"	+7 V
Output "On" (See note 1)	+10 V
DEVICE DISSIPATION:	
Up to T_A = +55°C	1W
Above T_A = +55°C	derate linearly at 10.5 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +75°C
Storage	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

NOTE 1: This is the maximum output voltage for any single output. The output voltage must be consistent with the maximum dissipation and derating curve for worst-case conditions. Example: All segments "on", 100% duty cycle.

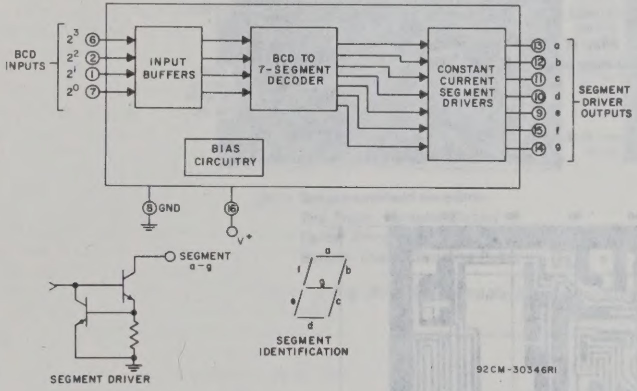
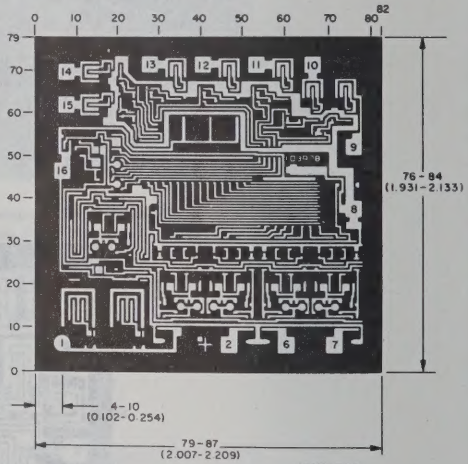


Fig. 1 – Functional block diagram of the CA3161E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage Operating Range, V^+		4.5	5	5.25	V
Supply Current, I^+ (all inputs high)		–	3.5	8	mA
Output Current Low (V_O = 2 V)		18	25	32	mA
Output Current High (V_O = 5.5 V)		–	–	250	μA
Input Voltage High (logic "1" level)		2	–	–	V
Input Voltage Low (logic "0" level)		–	–	0.8	V
Input Current High (logic "1")	2 V	–30	–	–	μA
Input Current Low (logic "0")	0 V	–40	–	–	μA
Propagation Delay Time	t_{PHL}	–	2.6	–	μs
	t_{PLH}	–	1.4	–	



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

TRUTH TABLE

BINARY STATE	INPUTS				OUTPUTS							DISPLAY
	2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	L	L	L	L	L	L	L	L	L	L	H	0
1	L	L	L	H	H	L	L	H	H	H	H	1
2	L	L	H	L	L	L	H	L	L	H	L	2
3	L	L	H	H	L	L	L	L	H	H	L	3
4	L	H	L	L	H	L	L	H	H	L	L	4
5	L	H	L	H	L	H	L	L	H	L	L	5
6	L	H	H	L	L	H	L	L	L	L	L	6
7	L	H	H	H	L	L	L	H	H	H	H	7
8	H	L	L	L	L	L	L	L	L	L	L	8
9	H	L	L	H	L	L	L	L	H	L	L	9
10	H	L	H	L	H	H	H	H	H	H	L	–
11	H	L	H	H	L	H	H	L	L	L	L	E
12	H	H	L	L	H	L	L	H	L	L	L	H
13	H	H	L	H	H	H	H	L	L	L	H	L
14	H	H	H	L	L	L	H	H	L	L	L	P
15	H	H	H	H	H	H	H	H	H	H	H	BLANK

CA3162E

A/D Converter for 3-Digit Digital Readout System

The CA3162E is a monolithic integrated circuit that comprises the A/D converter section of a 3-digit digital readout system. It is used with the CA3161E BCD-to-Seven-Segment Decoder/Driver* and a minimum of external parts to implement a complete system.

Features:

- Dual-slope A/D conversion
- Ultra-stable internal band-gap voltage reference
- Capable of reading 99 mV below ground with single supply
- Differential input
- Internal timing – no external clock required
- Choice of low-speed (4-Hz) or high-speed (96-Hz) conversion rate
- "Hold" inhibits conversion but maintains display
- Multiplexed operation for high efficiency
- Overrange indication – "EEE" for reading greater than +999 mV, "___" for reading more negative than –99 mV when used with CA3161E BCD-to-Seven Segment Decoder/Driver

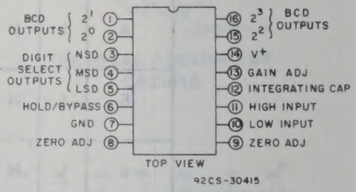
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 5 V, Zero pot centered, gain pot = 2.4 kΩ unless otherwise stated

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Operating Supply Voltage Range, V^+		4.5	5	5.5	V
Supply Current, I^+	100 kΩ to V^+ on terms. 3,4,5	–	–	17	mA
Input Impedance, Z_I		–	100	–	MΩ
Input Bias Current, I_{IB}	Terms. 10 and 11	–	–80	–	nA
Unadjusted Zero Offset	$V_{11}–V_{10}$ = 0V, read decoded output	–12	–	+12	mV
Unadjusted Gain	$V_{11}–V_{10}$ = 900 mV, read decoded output	846	–	954	mV
Linearity	See Notes 1 and 2	–1	–	+1	Count
Conversion Rate:					
Slow Mode	Term. 6 = open or gnd	–	4	–	Hz
Fast Mode	Term. 6 = 5 V	–	96	–	
Conversion Control Voltage (Hold Mode) at Terminal 6		0.8	1.2	1.6	V
Common-Mode Input Voltage Range, V_{ICR}	See Note 3	–0.2	–	+0.2	V
BCD Sink Current at terms. 1,2,15,16	$V_{BCD} \leq 0.5$ V, at logic zero state	0.4	1.6	–	mA
Digit Select Sink Current at terms. 3,4,5	$V_{Digit\ Select}$ = 4V at logic zero state	1.6	2.5	–	mA
Zero Temperature Coefficient	V_I = 0V, zero pot centered	–	10	–	µV/°C
Gain Temperature Coefficient	V_I = 900 mV, gain pot = 2.4 kΩ	–	0.005	–	%/°C

NOTES:

1. Apply zero volts across V_{11} to V_{10}. Adjust zero potentiometer to give 000 mV reading. Apply 900 mV to input and adjust gain potentiometer to give 900 mV reading.
2. Linearity is measured as a difference from a straight line drawn through zero and positive full scale. Limits do not include ±0.5 count bit digitizing error.
3. For applications where negative terminal 10 is not operated at terminal 7 potential, a return path of not more than 100 kΩ resistance must be provided for input bias currents.

TERMINAL ASSIGNMENT
CA3162E



Circuit Description

The functional block diagram of the CA3162E is shown in Fig. 1. The heart of the system is the V/I converter and reference-current generator. The V/I converter converts the input voltage applied between terminals 10 and 11 to a current that charges the integrating capacitor on terminal 12 for a predetermined time interval. At the end of the charging interval, the V/I converter is disconnected from the integrating capacitor, and a band-gap reference constant-current source of opposite polarity is connected. The number of clock counts that elapse before the charge is restored to its original value is a direct measure of the signal induced current.

The restoration is sensed by the comparator, which in turn latches the counter. The count is then multiplexed to the BCD outputs.

The timing for the circuit is derived from a 786-kHz ring oscillator. The oscillator frequency is divided by 2048 to provide the multiplex rate of 384 Hz. This rate is further divided by 96 to obtain the slow-speed conversion rate of 4 Hz (terminal 6 open or grounded). When the "hold" terminal (terminal 6) is biased to ±1.2 V, conversion ceases, but multiplex continues and the reading is held and displayed continuously.

When terminal 6 is biased at +5 V, a portion of the divide-by-96 circuitry is disabled so that the conversion rate increases to 24 times the slow-speed rate (4 x 24 = 96 Hz). Note

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* The CA3161E is described in RCA data bulletin File No. 1079.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 7 and 14)	+7 V
INPUT VOLTAGE (terminal 10 or 11 to ground)	±15 V
DEVICE DISSIPATION:	
Up to T_A = +55°C	750 mW
Above T_A = +55°C	derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +75°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0/79 mm) from case for 10 seconds max.	+265°C

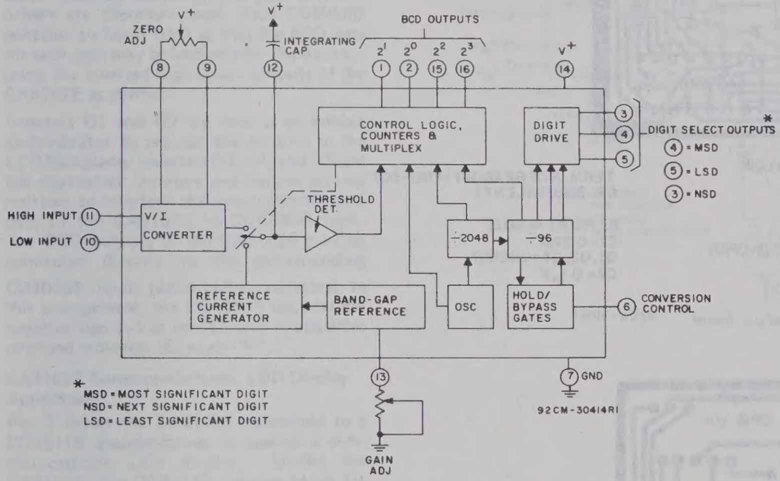


Fig. 1 — Functional block diagram of the CA3162E.

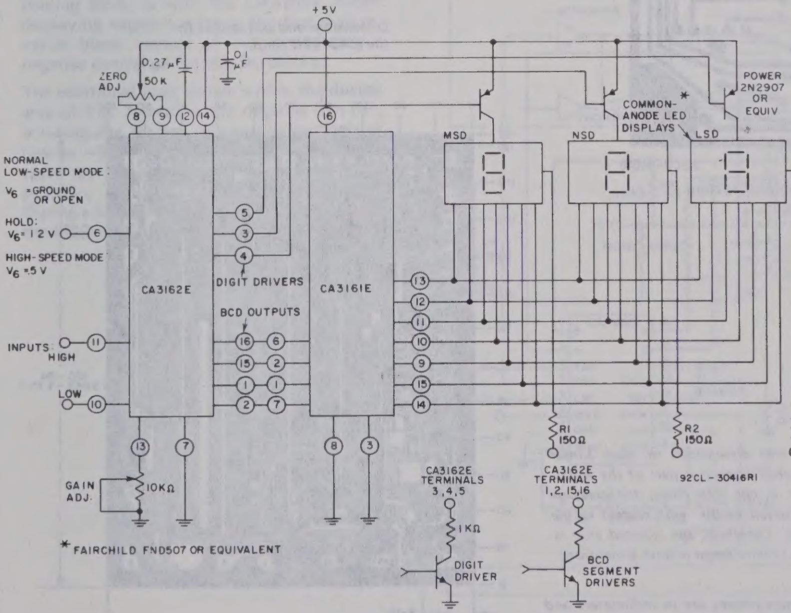


Fig. 2 — Basic digital readout system using the CA3162E and the CA3161E.

that the multiplex rate is unchanged. Fig. 3 shows the timing of conversion and digit select pulses for the high-speed mode. Note that the basic A/D conversion process requires approximately 5 ms in both modes.

The "EEE" or "___" displays indicate that the range of the system has been exceeded in the positive or negative direction, respectively. Negative voltages to −99 mV are displayed with the minus sign in the MSD. The BCD code is 1010 for a negative overrange (___) and 1011 for a positive overrange (EEE).

System Application

Fig. 2 is the block diagram of a basic system using the CA3162E and the CA3161E. An actual-size PC board layout for this circuit is shown in Fig. 4. The BCD outputs of the CA3162E drive the BCD inputs of the CA3161E BCD-to-7-segment decoder directly. The seven-segment outputs are multiplexed to the three LED displays. The digits are selected by terminals 3, 4, and 5 (CA3162E), which provide base current to the external p-n-p transistors. The p-n-p's, in turn, provide current to the anodes of the display. Adjustment procedures for the gain and zero potentiometers are given in Note 1 of the Electrical Characteristics chart.

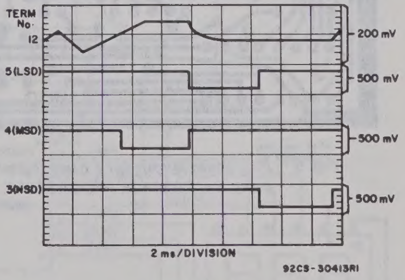
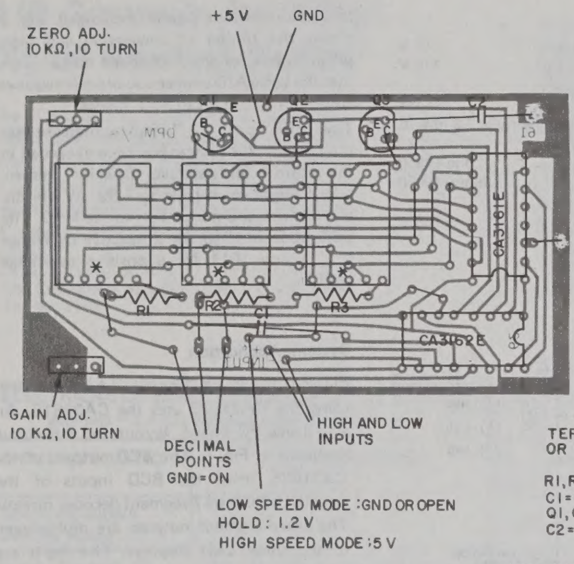


Fig. 3 — High speed mode timing diagram.

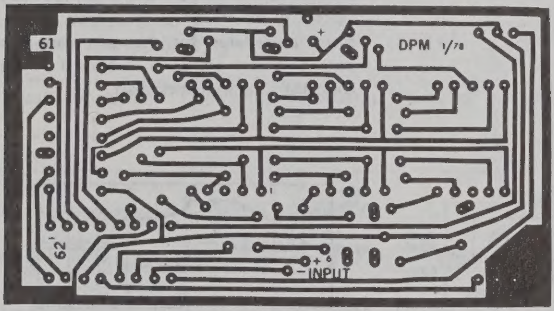


TERM. 3 OF READOUT (FND-507 OR EQUIVALENT)

R1, R2, R3 ≈ 150 Ω
C1 = 0.27 μF
Q1, Q2, Q3 = 2N2907
C2 = 0.1 μF

Fig. 4 — Component side of p.c. board

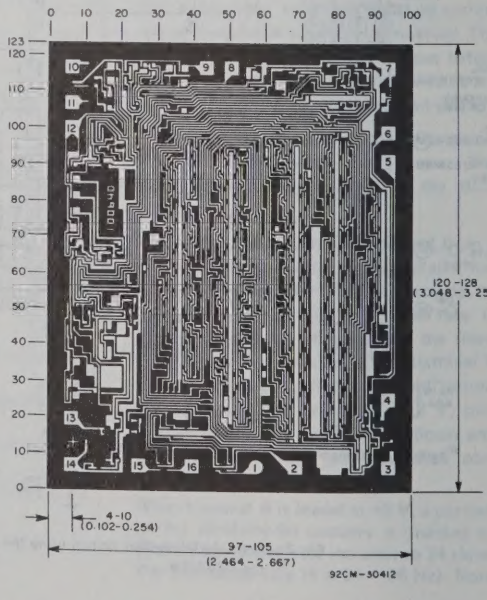
92CS-31017



92CS-31015

Fig. 5 — P.C. board layout for a basic digital readout system using the CA3162E and CA3161E.

Dimensions and pad layout for the CA3162H Chip.



92CM-30412

The photographs and dimensions of each Linear chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3162E Liquid Crystal Display (LCD) Application

Fig. 6 shows the CA3162E in a typical LCD application. LCD's may be used in favor of LED displays in applications requiring lower power dissipation, such as battery-operated equipment, or when visibility in high-ambient-light conditions is desired.

Multiplexing of LCD digits is not practical, since LCD's must be driven by an ac signal and the average voltage across each segment is zero. Three CD4056B liquid-crystal decoder/drivers are therefore used. Each CD4056B contains an input latch so that the BCD data for each digit may be latched into the decoder using the inverted digit-select outputs of the CA3162E as strobes.

Inverters G1 and G2 are used as an astable multivibrator to provide the ac drive to the LCD backplane. Inverters G3, G4, and G5 are the digit-select inverters and require pull-up resistors to interface the open-collector outputs of the CA3162E to COS/MOS logic. The BCD outputs of the CA3162E may be connected directly to the corresponding CD4056B inputs (using pull-up resistors). In this arrangement, the CD4056B decodes the negative sign (–) as an "L" and the positive overload indicator (E) as an "H".

CA3162E Common-Cathode, LED Display Application

Fig. 7 shows the CA3162E connected to a CD4511B decoder/driver to operate a common-cathode LED display. Unlike the CA3161E, the CD4511B remains blank for all BCD codes greater than nine. After 999 mV the display blanks rather than displaying EEE, as with the CA3161E. When displaying negative voltage, the first digit remains blank instead of (–), and during a negative overrange the display blanks.

The additional logic shown within the dotted area of Fig. 7 restores the negative sign (–), allowing the display of negative numbers as low as –99 mV. Negative overrange is indicated by a negative sign (–) in the MSD position. The rest of the display is blanked. During a positive overrange, only segment b of the MSD is displayed.

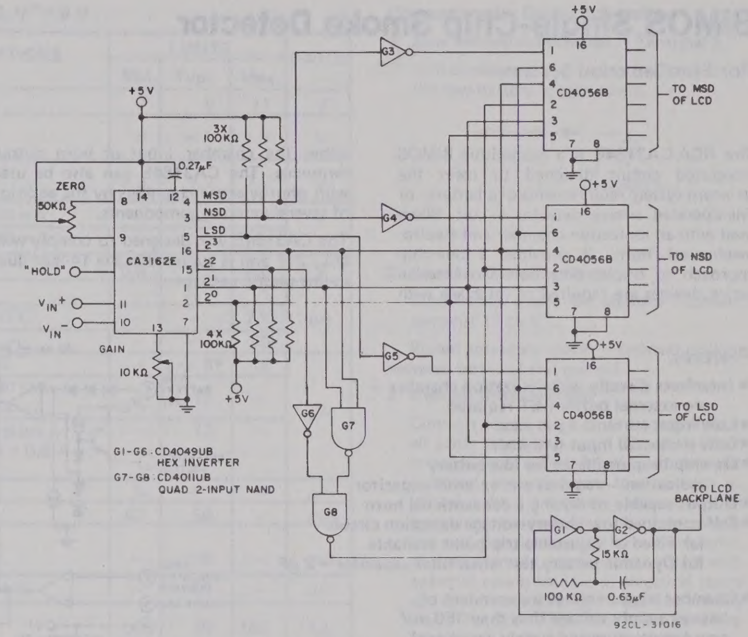


Fig. 6 – Typical LCD application.

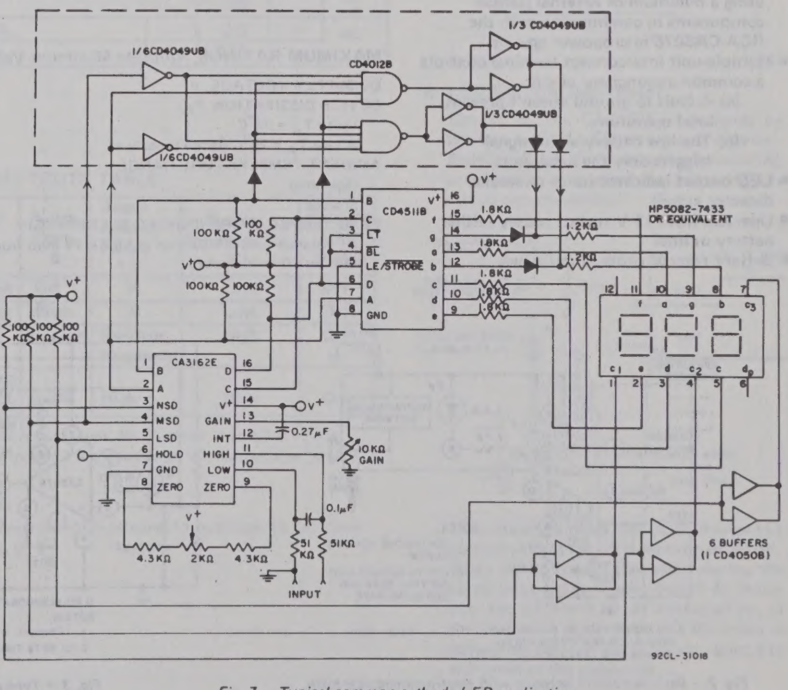


Fig. 7 – Typical common-cathode LED application.

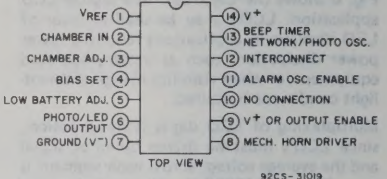
BiMOS Single-Chip Smoke Detector

For Fire Detection Systems

The RCA-CA3164E is a monolithic BiMOS integrated circuit designed to meet the stringent system requirements of a battery- or line-operated smoke detector circuit. When used with an ionization chamber and electromechanical horn, it provides a one-chip approach to smoke detection. No external active devices are required to interface with either the chamber input or horn output terminals. The CA3164E can also be used with photoelectric chambers by the addition of several external components.

The CA3164E was designed to comply with U.L. 217 and is supplied in the 14-lead dual-in-line plastic package.

TERMINAL ASSIGNMENT



Features:

- **Interfaces directly with ionization chamber — no external buffer FET required**
- **Low input current: 1 pA max.**
- **Gate-protected input terminals**
- **On-chip beep oscillator for low battery indication — requires one external capacitor**
- **Output capable of driving a conventional horn**
- **Self-contained low-battery-voltage detection circuit**
  - **(a) Fixed or adjustable trip point available**
  - **(b) Dynamic battery test when filter capacitor = 2 μF**
- **Chamber trigger voltage independent of battery supply voltage (less than 150 mV over temperature and supply variations)**
- **Designed to comply with U.L. 217**
- **Reference source current available = 5 μA (typ.)**
- **Low standby battery current = 8 μA (typ.)**
- **Can be used with photoelectric sensors by using a minimum of external passive components in combination with the RCA-CA3078 micropower op-amp**
- **Multiple-unit interconnect terminal controls a common annunciator circuit**
  - **(a) A fault to ground doesn't prevent local operation.**
  - **(b) The low battery alarm signal triggers only the local unit.**
- **LED output indicates status of smoke-detector circuit**
- **Operates from 11 V (max.) supply (either battery or line)**
- **Battery reversal protection feature**

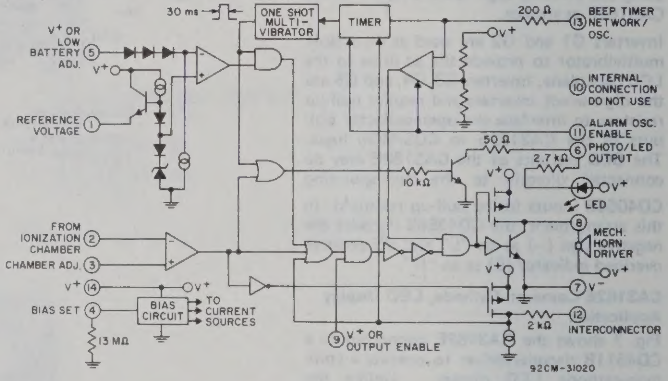
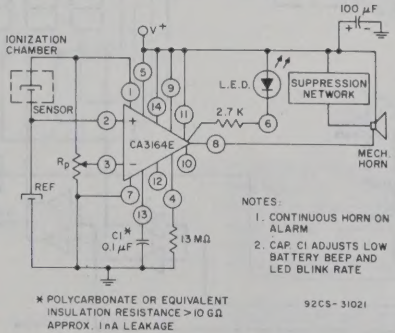


Fig. 1 — Simplified functional diagram for CA3164E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

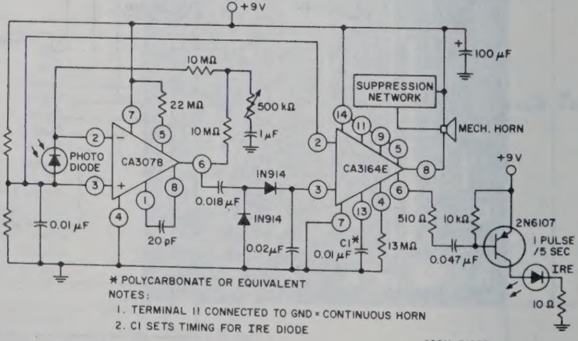
DC SUPPLY VOLTAGE, V^+	+11 V
DEVICE DISSIPATION, P_D:	
Up to T_A = 25°C	600 mW
Above T_A = 25°C derate linearly at	6.7 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +50°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C



NOTES:
1. CONTINUOUS HORN ON ALARM
2. CAP. CI ADJUSTS LOW BATTERY BEEP AND LED BLINK RATE

* POLYCARBONATE OR EQUIVALENT INSULATION RESISTANCE > 10 GΩ APPROX. 1 nA LEAKAGE

Fig. 2 — Basic ionization detector with electro-mechanical horn.



* POLYCARBONATE OR EQUIVALENT

NOTES:
1. TERMINAL 11 CONNECTED TO GND = CONTINUOUS HORN
2. CI SETS TIMING FOR IRE DIODE

Fig. 3 — Typical photoelectric systèm using CA3164E.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 9$ V

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Operating Voltage		7	9	11	V
Common-Mode Input Voltage Range, V_{ICR}	$(V^+ - 2\ V) = 7$ V	0	–	7	V
Low-Battery Trigger Voltage	External adjust (increase only)	7.3	7.7	7.9	V
Horn Driver $V_{CE(SAT)}$	Term. 8 = 100 mA	–	0.5	–	V
	Term. 8 = 300 mA	–	1	–	
Reference Voltage		5.8	6.2	6.6	V
Input Leakage Current, I_L	Term. 2	–	–	1	pA
	Term. 2 at 50°C	–	–	2.5	
	Term. 3	–	–	50	
Standby Current (13 MΩ from Term. 4 to gnd)	No LED connected	–	8*	12	µA
	LED connected–20 mA for 30 ms every 60s	–	18	–	
	Photoelectric operation – LED photocurrent = 0.6 A (5 sec. rate)	–	13	–	
Reference Source Current		5	–	–	µA
LED Driver Sink Current		40	50	–	mA
Interconnect Current Source	$I_{Sink} = 10\ \mu A$ typ.	–	2.8	–	mA
Sink	$I_{Source} = 1.3$ mA typ.	–	50	–	µA
Low-Battery Adjust, Term.5 Input Current		50	70	100	nA
Timing Current	Term. 13	10	–	50	nA
LED Blink Period	Adjustable	–	–	1	PPM
LED Pulse Width	Fixed	–	30	–	ms
Remote Fan-Out		20	–	–	
Alarm Pulse Duty Cycle (4.7 MΩ from Term. II to gnd	On-time	–	95	–	%
	On-time = 95%	–	0.5	–	sec.
	Off-time = 5%	–	0.026	–	

* Adjustable to 5 µA

OPERATING MODES TRUTH TABLE

Condition	Smoke Ionization Chamber	Low Battery	Led 6	Alarm Horn 8	Alarm Enable Pulser 11	System Interconnect 12	Remote Unit Status
Normal	No	No	Blink	Off	X	Low	Off
Low Battery	No	Yes	Blink	Beep	X	Low	Off
Smoke In Chamber	Yes	X	On	Pulsed*	Resistor to ground	High	On
External Input A1 From Remote Unit	No	No	Blink	On**	High	High	On

** Alarm Horn follows mode programmed for internal system input. For example, if terminal 11 has resistor connected to ground, horn will beep. If terminal 11 is connected to V^+, horn will be "on."

X = Don't Care

Blink & Beep = 30 msec (fixed) every 50 sec (ADJ)

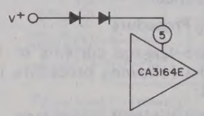
Pulsed = 95% "on" time – Period is determined by resistor from terminal 11 to ground-5% Off Time

* Horn "Continuous" if terminal 11 is connected to V^+

Connections for Optional Functions

1. **Low Battery Adjustment – Terminal 5**

Add diodes as shown below to increase the low-battery trigger point.



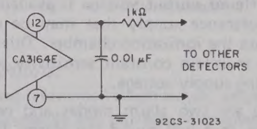
2. **Sounder Operating Mode**

Continuous sound on alarm – connect terminal 11 to V^+.

Pulsed sound on alarm – connect resistor between terminal and ground.

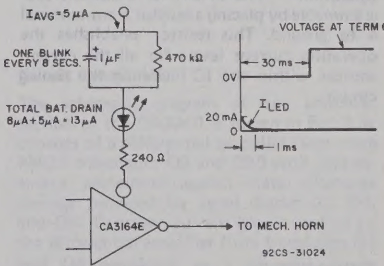
3. **Remote (Interconnect)**

Connect terminal 12 to same terminal on all other units (fan out = 20 units). When interconnecting units for the remote-alarm function, the extremely low currents involved make it extremely important that a provision be made for limiting externally induced transients into the remote terminal. For example, inadvertent contact with external power sources or electrical storm activity may cause triggering of the remote alarm function. The circuit below will reduce the possibility of such occurences.



4. **LED On-Time Adjustment**

Option 1: The CA3164E is designed to provide a fixed LED on-time of approximately 30 ms. For applications requiring a reduction in on-time the following circuit is recommended:



This circuit reduces the LED on-time but does not affect the horn on-time of 30 ms. When using this configuration during the continuous-alarm mode (smoke in chamber) the LED will be off instead of on, as shown in the truth table. If the horn is pulsed during the alarm mode, the LED will blink at the pulse rate.

Option 2: A chip design change can be implemented to generate a 10 ms LED on-time. The sounder would also be pulsed for only 10 ms. A further reduction in this time may result in faulty operation of the sounder.

5. **Cleaning Procedure**

   To insure leakage currents of less than 1 pA the following procedure is recommended:

   (a) degrease in trichlorethylene
   (b) rinse in de-ionized water

Circuit Description

Basic Functions – The CA3164E is designed to interface directly with an ionization-chamber type of smoke detector. Upon being triggered by a decreasing voltage at the ionization-chamber output, the IC operates a mechanical transducer. In addition to this basic smoke-detector function, another circuit monitors and compares the battery voltage to an internal reference-voltage source. Once the battery voltage drops below a defined level, a short 30-ms beep sound is produced in synchronism with an LED indicator every 50 seconds. This rate is determined by a programming resistor connected between terminal 4 and ground and an external 0.1 μF capacitor connected between terminal 13 and ground.

A buffered output voltage is available from the reference supply that may be used to operate the ionization chamber. This voltage helps maintain constant sensitivity with decreasing supply voltage.

There are two alarm modes and two conditions that will sound the alarm. The first alarm condition is the normal smoke in the ionization chamber; the other condition is a high level to the remote input/output terminal of the IC.

The first alarm mode is the customary continuous sound. The second alarm mode is an interrupted or pulsed sound.

Operation – The CA3164E is current programmable by placing a resistor from terminal 4 to ground. This resistor establishes the operating current levels for all the current sources within the IC including the timing circuits.

An operational amplifier configuration is used for the ionization chamber input. P-channel MOS field effect transistors are used on this input in the bootstrap configuration shown in Fig. 4 to drive the protection diodes and maintain the sub-pioampere input current.

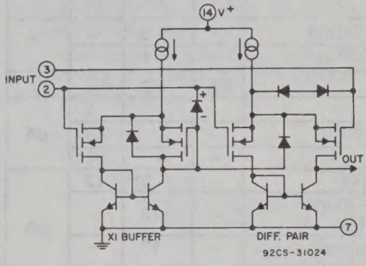


Fig. 4 – Schematic of ionization-chamber amplifier.

A conventional bipolar amplifier is used for the battery monitor circuit. The zener diode is biased at about 3 μA. This zener voltage is raised one V_{AK} and then applied to the base of an emitter-follower transistor to buffer and reflect the zener voltage to the outside reference terminal. By providing an additional input terminal (terminal 5), where three level-shifting diodes are available, an additional external means is provided to raise the voltage level at which the CA3164E goes into the low-voltage alarm mode.

An integrating type of timer is used to generate the one-minute LED power-monitor and battery-function indicator pulse. Fig. 5 shows the system. A constant-current source charges the external 0.1-μF timing amplifier P1, which subsequently triggers the 30-ms one-shot multivibrator composed of n-channel MOS transistor N_3 and n-p-n transistor Q1.

N_3 is then cut off and its drain climbs to the supply rail, linearly charging capacitor CP. When the drain of N_3 reaches the supply rail, the charging current ceases, cutting off the base current of N_3 and discharging the capacitor.

An open-collector n-p-n transistor is used to drive the optional external LED power monitor and battery condition indicator.

When terminal 11 is returned to V^+, the alarm sounds continuously. However, it terminal 11 is returned to ground through a programming resistor as shown in the block diagram, the alarm pulses. The pulse rate is determined by the sum of the current through the programming resistor connected to terminal 11 and the current from the basic timer current source. Thus, when the detector goes into the alarm mode, the nominal 50-second timer is increased to a nominal 0.5-second period. This second 0.5-second rate is a function of the external 4.3-M Ω programming resistor.

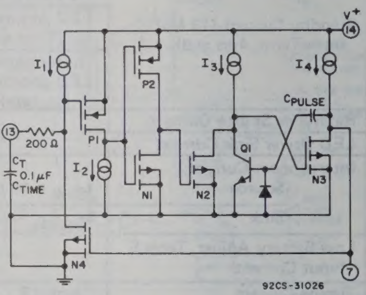


Fig. 5 – Schematic of timer and one-shot multivibrator.

A large n-p-n transistor at terminal 8 is capable of operating the typical mechanical interrupter type sounders. An active pull-up transistor is also incorporated in this circuit. Terminal 9 must be returned directly to V^+.

Terminal 12, the interconnect terminal, is both an input and output for the circuit. When connected by two wires to other units, alarm in any one unit will activate the other units. A small sinking current of only 10 μA keeps the line impedance down while a sourcing current of over 2 mA is available in the alarm mode. This current is more than sufficient to trigger over 20 additional units.

Dual BiMOS Operational Amplifiers

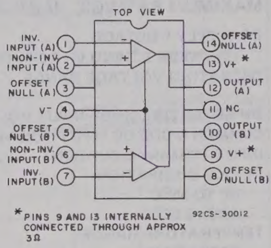
With MOS/FET Input, Bipolar Output

The RCA-CA3240A and CA3240 are dual versions of the popular CA3140-series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5 V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

The CA3240A and CA3240 are supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix), and in the 14-lead dual-in-line plastic package (E1 suffix). They are pin-compatible with the industry standard 747 and 1458 operational amplifiers in similar packages. The CA3240A and CA3240 have an operating-temperature range of −40 to +85°C. The offset null feature is available only when these types are supplied in the 14-lead dual-in-line plastic package (E1 suffix).

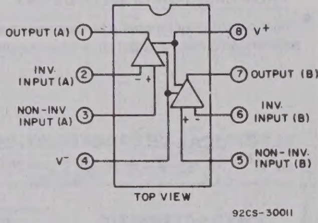
Features:

- Dual version of CA3140
- Internally compensated
- MOS/FET input stage
  - (a) Very high input impedance (Z_{IN}) – 1.5 TΩ typ.
  - (b) Very low input current (I_I) – 10 pA typ. at ± 15 V
  - (c) Wide common-mode input-voltage range (V_{ICR}) – can be swung 0.5 volt below negative supply-voltage rail
  - (d) Rugged input stage – bipolar diode protected
- Directly replaces industry types 747 and 1458 in most applications
- Operation from 4-to-36 volts single or dual supplies
- Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts
- Wide bandwidth – 4.5 MHz unity gain at ± 15 V or 30 V
- High voltage-follower slew rate – 9 V/μs
- Output swings to within 0.5 volt of negative supply at $V^+ = 5$ V, $V^- = 0$



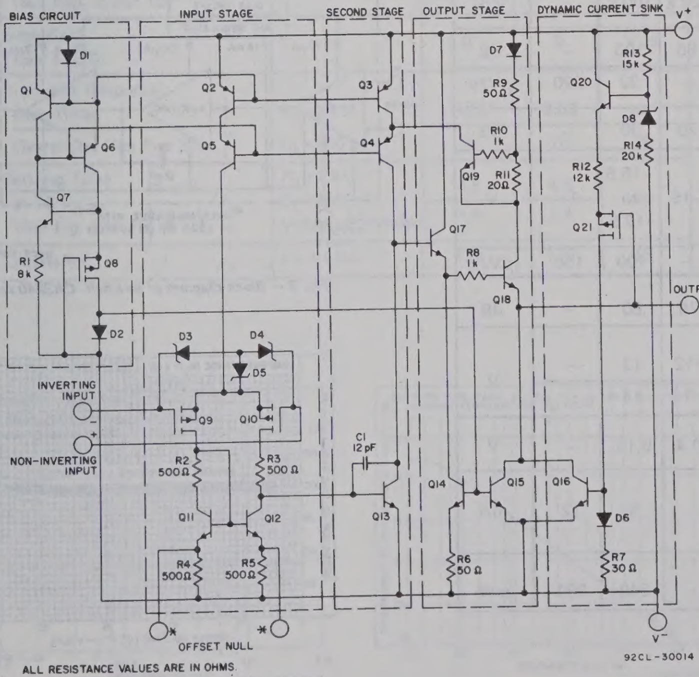
*PINS 9 AND 13 INTERNALLY CONNECTED THROUGH APPROX 3Ω

E1 Suffix
Pin compatible with the industry-standard 747



E Suffix
Pin compatible with the industry-standard 1458

Fig. 1 – Functional diagrams.



ALL RESISTANCE VALUES ARE IN OHMS.
*ONLY AVAILABLE WITH 14-LEAD DIP (E1 SUFFIX)

Fig. 2 – Schematic diagram of one-half CA3240 series.

Applications:

- Ground-referenced single-supply amplifiers in automobile and portable instrumentation
- Sample and hold amplifiers
- Long-duration timers/multivibrators (microseconds–minutes–hours)
- Photocurrent instrumentation
- Active filters
- Intrusion alarm systems
- Comparators
- Instrumentation amplifiers
- Function generators
- Power supplies

Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2 and Q5 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14-lead plastic package (E1 suffix) is provided through the use of this current mirror.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
OPERATING VOLTAGE RANGE	4 to 36 V or ±2 to ±18 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT	1 mA
DEVICE DISSIPATION:	
UP TO 55°C	630 mW
ABOVE 55°C	Derate linearly 6.67 mW/°C
TEMPERATURE RANGE:	
OPERATING	−40 to +85°C
STORAGE	−65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION●	UNLIMITED
LEAD TEMPERATURE (DURING SOLDERING): AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C

● Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 15 V, V^- = 15 V, T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	LIMITS						UNITS
	CA3240A			CA3240			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\lvert V_{IO}\rvert$	–	2	5	–	5	15	mV
Input Offset Current, $\lvert I_{IO}\rvert$	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}● (See Figs. 4, 19)	20 k	100 k	–	20 k	100 k	–	V/V
	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR (See Fig. 9)	–	32	320	–	32	320	µV/V
	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig. 16)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V$ PSRR (See Fig. 11)	–	100	150	–	100	150	µV/V
	76	80	–	76	80	–	dB
Maximum Output Voltage,■ (See Figs. 22, 16) V_{OM}^+	+12	13	–	+12	13	–	V
V_{OM}^-	−14	−14.4	–	−14	−14.4	–	
Maximum Output Voltage,† V_{OM}^-	0.4	0.13	–	0.4	0.13	–	V
Supply Current, I^+ (See Fig. 7) For Both Amps.	–	8	12	–	8	12	mA
Total Device Dissipation, P_D	–	240	360	–	240	360	mW

● At V_O = 26 $V_{p\text{-}p}$, +12 V, −14 V and R_L = 2 kΩ.

■ At R_L = 2 kΩ.

† At V^+ = 5 V, V^- = GND, I_{Sink} = 200 µA.

The gain stage transistor Q13 has a high-impedance active load (Q3 and Q4) to provide maximum open-loop gain. The collector of Q13 directly drives the base of the compound emitter-follower output stage. Pull-down for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q14 and Q15 and (2) dynamic current-sink transistor Q16 and its associated circuitry. *The level of pull-down current is constant at about 1 mA for Q15 and varies from 0 to 18 mA for Q16 depending on the magnitude of the voltage between the output terminal and V^+.* The dynamic current sink becomes active whenever the output terminal is more negative than V^+ by about 15 V. When this condition exists, transistors Q21 and Q16 are turned on causing Q16 to sink current from the output terminal to V^-. This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q18 if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2 V (V_{CE}(sat)) of V^- with a 2-kΩ load to ground. *When the load is returned to V^+, it may be necessary to supplement the 1 mA of current from Q15 in order to turn on the dynamic current sink (Q16).* This may be accomplished by placing a resistor (approx. 2 kΩ) between the output and V^-.

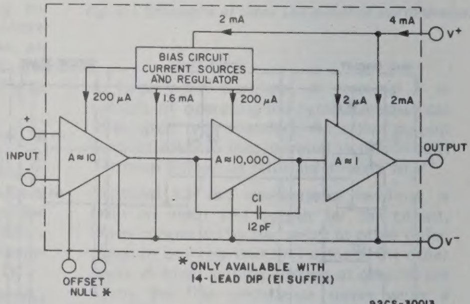


Fig. 3 – Block diagram of one-half CA3240 series.

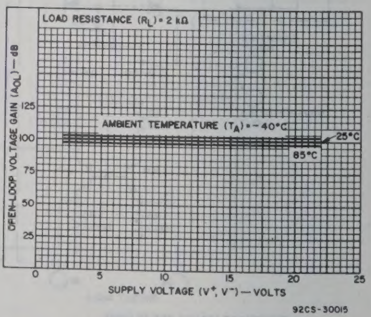


Fig. 4 – Open-loop voltage gain as a function of supply voltage and temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V $V^- = -15$ V $T_A = 25^\circ C$	TYPICAL VALUES CA3240A	CA3240	UNITS
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typ. Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Max. V_{IO}	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 21)	e_n	BW=140 kHz R_S = 1 MΩ	48	48	µV
Equivalent Input Noise Voltage (See Fig. 10)	e_n	f= 1 kHz, R_S= 100 Ω	40	40	nV/$\sqrt{\text{Hz}}$
		f=10 kHz, R_S= 100 Ω	12	12	
Short-Circuit Current to Opposite Supply Source	I_{OM}^+		40	40	mA
Sink	I_{OM}^-		11	11	
Gain-Bandwidth Product (See Figs. 5 and 19)	f_T		4.5	4.5	MHz
Slew Rate (See Fig. 6)	SR		9	9	V/µs
Transient Response: Rise Time	t_r	R_L=2 kΩ	0.08	0.08	µs
Overshoot (See Fig. 20)	t_r	C_L=100 pF	10	10	%
Settling Time at 10 $V_{p\text{-}p}$, (See Fig. 17) 1 mV	t_s	R_L=2 kΩ C_L=100 pF Voltage Follower	4.5	4.5	µs
10 mV	t_s		1.4	1.4	
Crosstalk		f = 1 kHz	120	120	dB

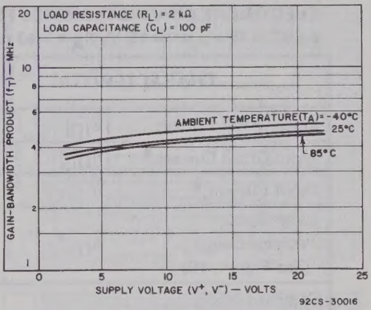


Fig. 5 — Gain-bandwidth product as a function of supply voltage and temperature.

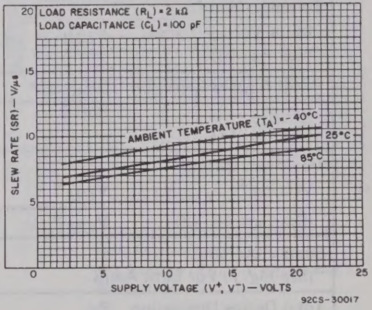


Fig. 6 — Slew rate as a function of supply voltage and temperature.

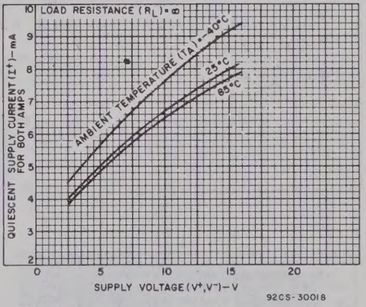


Fig. 7 — Quiescent supply current as a function of supply voltage and temperature.

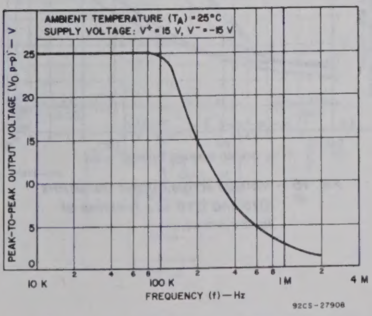


Fig. 8 — Maximum output voltage swing as a function of frequency.

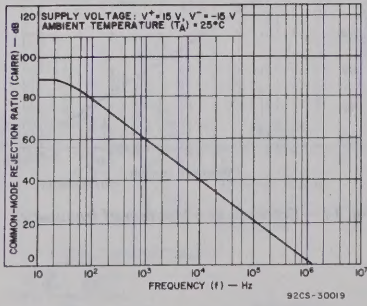


Fig. 9 — Common-mode rejection ratio as a function of frequency.

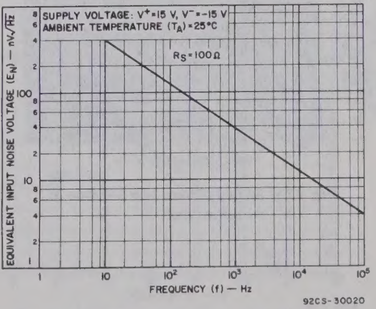


Fig. 10 — Equivalent input noise voltage as a function of frequency.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At $V^+ = 15$ V, $V^- = 15$ V, $T_A = -40$ to $+85\,^\circ C$ Unless Otherwise Specified

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\lvert V_{IO} \rvert$	3	10	mV
Input Offset Current,♠	$\lvert I_{IO} \rvert$	32	32	pA
Input Current,♠	I_I	640	640	pA
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}●	63 k	63 k	V/V
		96	96	dB
Common-Mode Rejection Ratio, (See Fig. 9)	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 16)	V_{ICR}	−15 to +12.3	−15 to +12.3	V
Power-Supply-Rejection Ratio, (See Fig. 11)	$\Delta V_{IO}/\Delta V$	150	150	μV/V
	PSRR	76	76	dB
Maximum Output Voltage,■ (See Figs. 16, 22)	V_{OM}^+	12.4	12.4	V
	V_{OM}^-	−14.2	−14.2	
Supply Current, (See Fig. 7) For Both Amps.	I^+	8.4	8.4	mA
Total Device Dissipation,	P_D	252	252	mW
Temperature Coefficient of Input Offset Voltage,	$\Delta V_{IO}/\Delta T$	15	15	μV/°C

● At $V_O = 26\ V_{p\text{-}p}$, +12 V, −14 V and $R_L = 2\ k\Omega$.

■ At $R_L = 2\ k\Omega$.

♠ At $T_A = 85\,^\circ C$

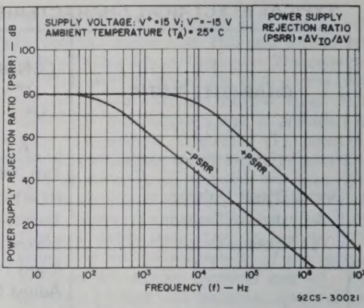


Fig. 11 – Power supply rejection ratio as a function of frequency.

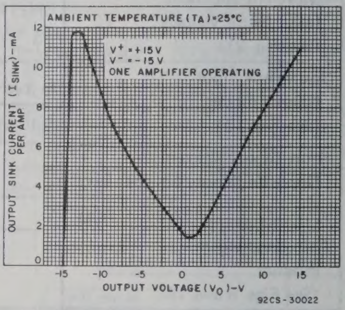


Fig. 12 – Output sink current as a function of output voltage.

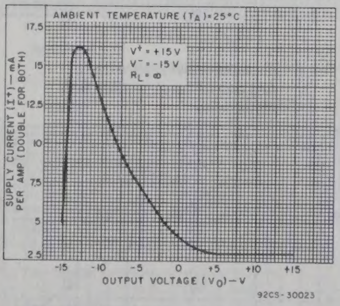


Fig. 13 – Supply current as a function of output voltage.

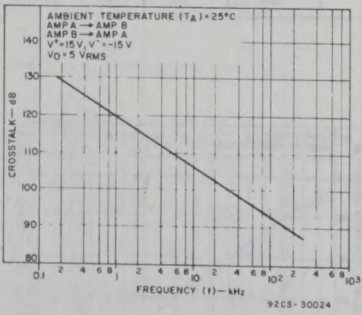


Fig. 14 – Crosstalk as a function of frequency.

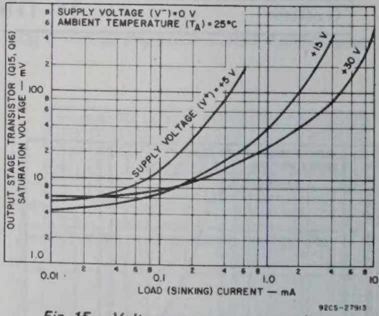
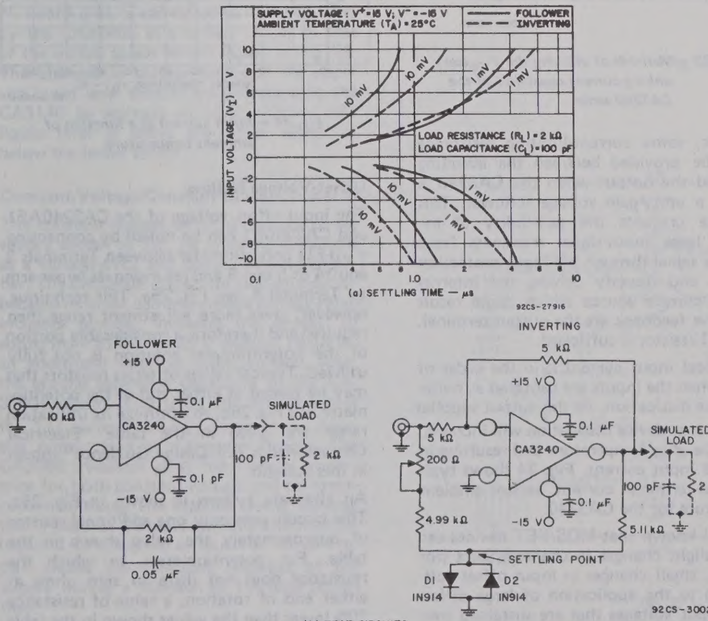


Fig. 15 – Voltage across output transistors Q15 and Q16 as a function of load current.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE
At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25°C$

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\lvert V_{IO} \rvert$	2	5	mV
Input Offset Current,	$\lvert I_{IO} \rvert$	0.1	0.1	pA
Input Current,	I_I	2	2	pA
Input Resistance		1	1	TΩ
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}	100 k	100 k	V/V
		100	100	dB
Common-Mode Rejection Ratio, CMRR		32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 22)	V_{ICR}	–0.5	–0.5	V
		2.6	2.6	
Power-Supply Rejection Ratio, PSRR		31.6	31.6	μV/V
		90	90	dB
Maximum Output Voltage,	V_{OM}^+	3	3	V
(See Figs. 16,22)	V_{OM}^-	0.3	0.3	
Maximum Output Current:				
Source,	I_{OM}^+	20	20	mA
Sink	I_{OM}^-	1	1	
Slew Rate (See Fig. 6)		7	7	V/μs
Gain-Bandwidth Product, (See Fig. 5)	f_T	4.5	4.5	MHz
Supply Current, (See Fig. 7)	I^+	4	4	mA
Device Dissipation,	P_D	20	20	mW



(b) TEST CIRCUITS

Fig. 17 — Input voltage as a function of settling time.

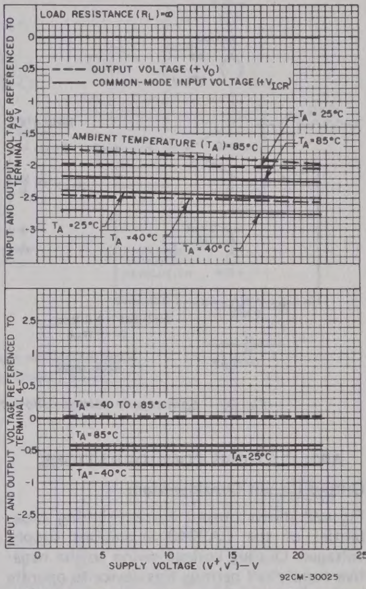


Fig. 16 — Output-voltage-swing capability and common-mode input-voltage range as a function of supply voltage and temperature.

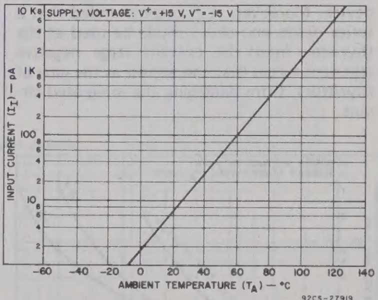


Fig. 18 — Input current as a function of ambient temperature.

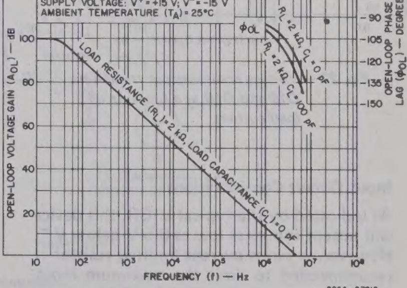


Fig. 19 — Open-loop voltage gain and phase lag as a function of frequency.

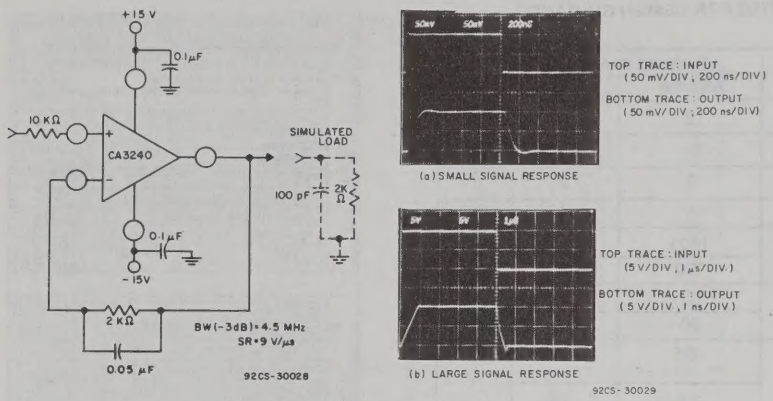

+15 V
0.1 μF
10 KΩ
CA3240
+
−
0.1 μF
−15V
2 KΩ
0.05 μF
SIMULATED LOAD
100 pF
2K Ω
BW(−3dB)=4.5 MHz
SR=9 V/μs
92CS-30028
50mV
50mV
200nS
TOP TRACE: INPUT (50 mV/DIV; 200 ns/DIV)
BOTTOM TRACE: OUTPUT (50 mV/DIV; 200 ns/DIV)
(a) SMALL SIGNAL RESPONSE
5V
5V
1μS
TOP TRACE: INPUT (5 V/DIV, 1 μs/DIV.)
BOTTOM TRACE: OUTPUT (5 V/DIV, 1 ns/DIV)
(b) LARGE SIGNAL RESPONSE
92CS-30029

Fig. 20 — Split-supply voltage-follower test circuit and associated waveforms.

APPLICATIONS CONSIDERATIONS

Output Circuit Considerations

Fig. 22 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig. 23 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

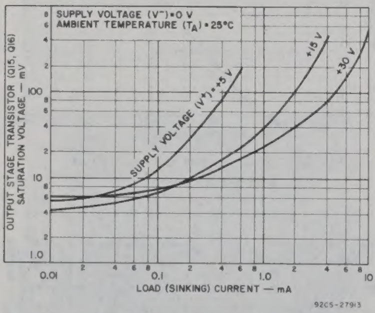


Fig. 22 — Voltage across output transistors Q15 and Q16 as a function of load current.

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as 0.5 V below V⁻. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

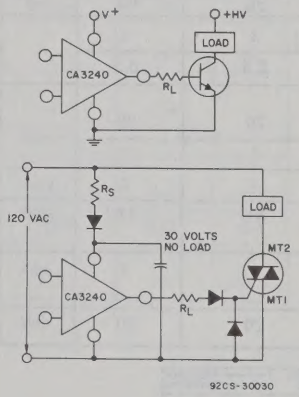


Fig. 23 — Methods of utilizing the $V_{CE}(sat)$ sinking-current capability of the CA3240 series.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig. 24 shows typical input-terminal current versus ambient temperature for the CA3240.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

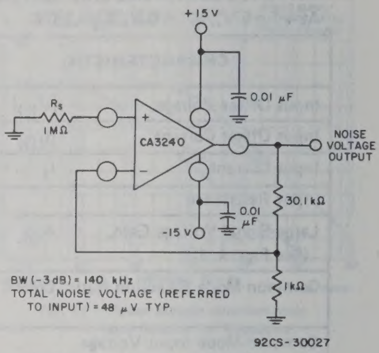


Fig. 21 — Test-circuit amplifier (30-dB gain) used for wideband noise measurement.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

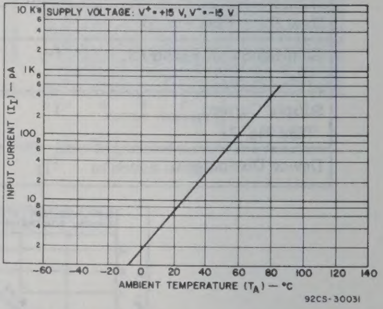


Fig. 24 — Input current as a function of ambient temperature.

Offset-Voltage Nulling

The input-offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10-kΩ potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Fig. 25a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig. 25b, to optimize its utilization range are given in the table "Electrical Characteristics For Design Guidance" shown in this bulletin.

An alternate system is shown in Fig. 25c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

TYPICAL APPLICATIONS

On/Off Touch Switch

The on/off touch switch shown in Fig. 26 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-kΩ resistor and 36-kΩ/42-kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

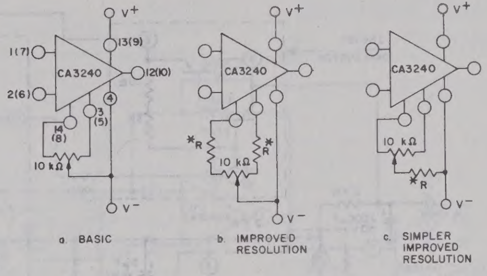
The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

Dual Level Detector (window comparator)

Fig. 27 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5-V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Fig. 26. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

Constant-Voltage/Constant-Current Power Supply

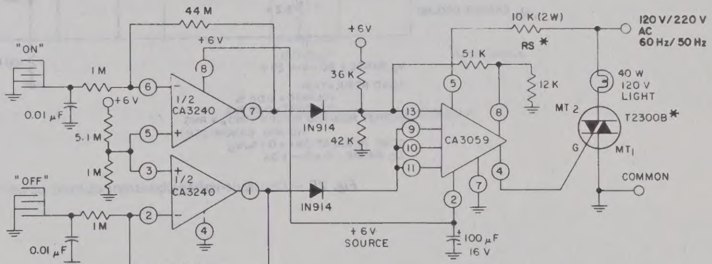
The constant-voltage/constant-current power supply shown in Fig. 28 uses the CA3240E as a voltage-error and current-sensing amplifier. The CA3240E is ideal for this application because its input common-mode voltage-range includes ground, allowing the supply to adjust from 20 mV to 25 V without requiring an additional negative input voltage. Also, the ground reference capability of the CA-3240E allows it to sense the voltage across the 1-Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40 W. Fig. 29 shows the transient response of the supply during a 100-mA to 1-A load transition.



*SEE CHARACTERISTICS CHART FOR VALUE R

92CS-30032

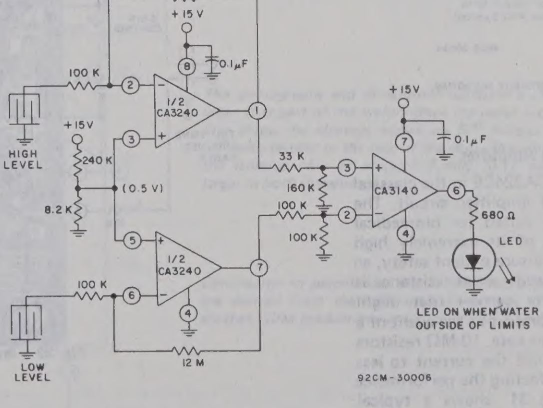
Fig. 25 — Three offset-voltage nulling methods. (CA3240AE1, CA3240E1 only.)



92CM-30005

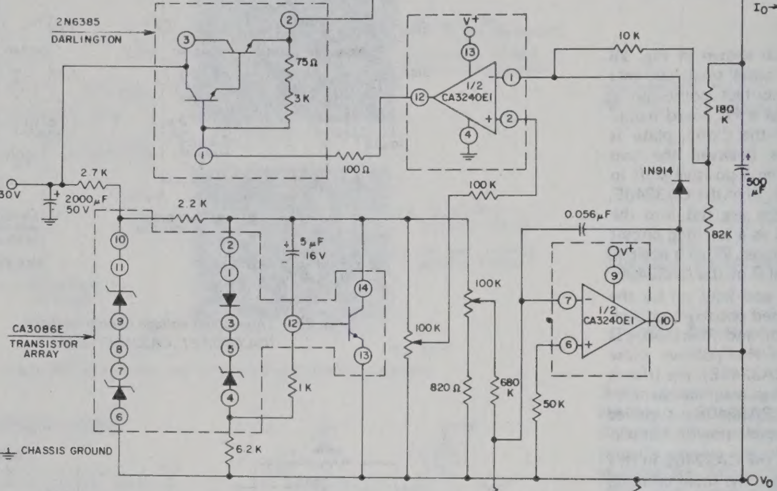
*AT 220 V OPERATION, TRIAC SHOULD BE T2300D, RS= 18 K, 5 W

Fig. 26 — On/off touch switch.



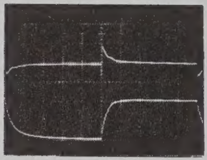
92CM-30006

Fig. 27 — Dual level detector.



VO RANGE = 20 mV — 25 V
LOAD REGULATION:
VOLTAGE < 0.08 %
CURRENT < 0.05 %
OUTPUT HUM AND NOISE = < 150µV RMS
(10 MHz BANDWIDTH)
LINE REGULATION = < 0.1 %/VO
IO RANGE = 10 mA — 1.3A

Fig. 28 — Constant-voltage/constant-current power supply.

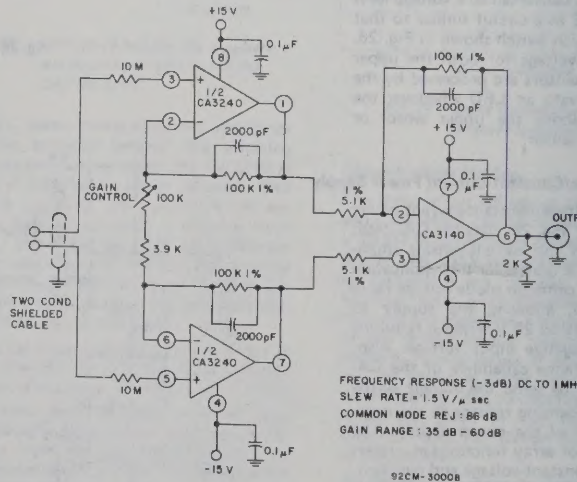


TRANSIENT RESPONSE

TOP TRACE: OUTPUT VOLTAGE
(500 mV/cm AND 5 µs/cm)
BOTTOM TRACE: COLLECTOR OF LOAD SWITCHING TRANSISTOR
LOAD = 100 mA TO 1A
(5 V/cm AND 5 µs/cm)

92CS-30034

Fig. 29 — Transient response.



FREQUENCY RESPONSE (-3dB) DC TO 1MHz
SLEW RATE = 1.5 V/µ sec
COMMON MODE REJ: 86 dB
GAIN RANGE: 35 dB - 60 dB

92CM-30008

Fig. 30 — Precision differential amplifier.

Precision Differential Amplifier

Fig. 30 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10-MΩ resistors have been used to limit the current to less than 2 µA without affecting the performance of the circuit. Fig. 31 shows a typical electrocardiogram waveform obtained with this circuit.

Differential Light Detector

In the circuit shown in Fig. 32, the CA3240E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

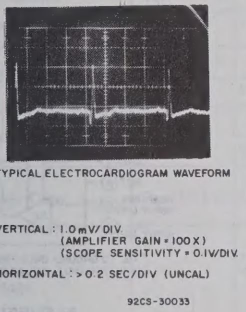


Fig. 31 — Typical electrocardiogram waveform.

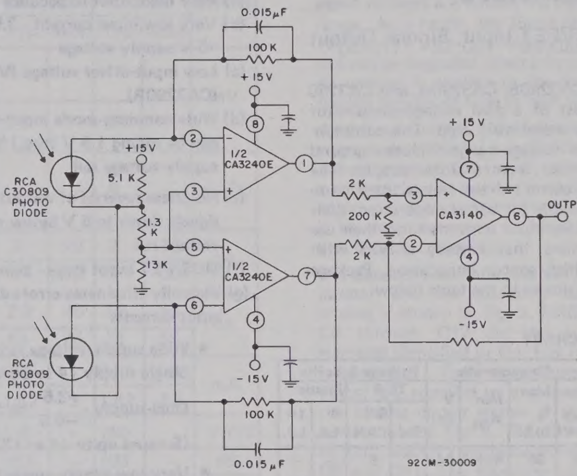
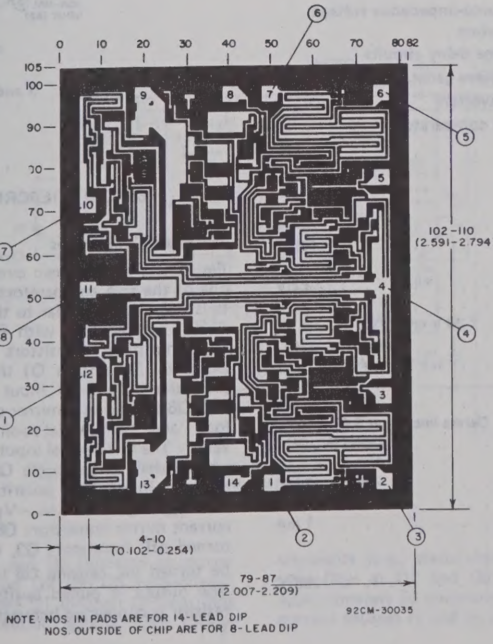


Fig. 32 — Differential light detector.

CA3240H Dimensions and Pad Layout



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3290, CA3290A, CA3290B

BiMOS Dual Voltage Comparators

With MOS/FET Input, Bipolar Output

The RCA-CA3290B, CA3290A, and CA3290 types consist of a dual voltage-comparator on a single monolithic chip. The common-mode input voltage range includes ground when operated from a single supply. The low supply-current drain makes these comparators suitable for battery operation; their extremely low input currents allow their use in applications that employ sensors with extremely high source impedances. Package options are shown in the table below.

SELECTION CHART

Selection	Characteristic				Package & Suffix			
	Max. V_{IO} (mV)	Max. I_I (pA)	Min. A_{OL}	V^+ (V)	TO-5		Plastic	
					Std.	DIL-CAN	8-Ld.	14-Ld.
CA3290B	6	30	50K	44	T	S	–	–
CA3290A	10	40	25K	36	T	S	E	E1
CA3290	20	50	25K	36	T	S	E	E1

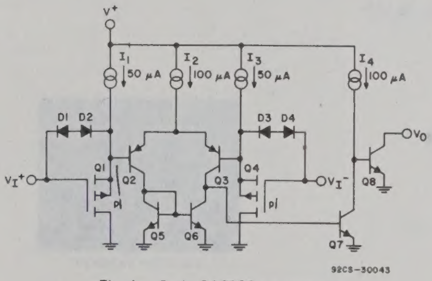


Fig. 1 – Basic CA3290 comparator.

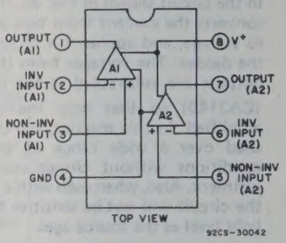
Features:

- MOS/FET input stage:
  - (a) Very high input impedance (Z_{IN}) - 1.7 TΩ typ.
  - (b) Very low input current - 3.5 pA typ. at +5 V supply voltage
  - (c) Low input-offset voltage (V_{IO}) - to 6 mV max. (CA3290B)
  - (d) Wide common-mode input-voltage range (V_{ICR}) - can be swung 1.5 V (typ.) below negative supply-voltage rail
  - (e) No phase reversal of output signal for input signals down to 5 V below negative supply-voltage rail
  - (f) MOS/FET input stage - zener diode protected
  - (g) Virtually eliminates errors due to flow of input currents
- Wide supply-voltage range:
  Single supply - 4 to 36 V dc
  Dual-supply - $\begin{matrix}+3.5\\-0.5\end{matrix}$ to ±18 V dc
  (B-types up to 44 or ±22 V dc)
- Very low supply-current drain - 0.8 mA at +5 V
- Differential input-voltage range - up to ±36 V
- Low output saturation voltage - 120 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS, and CMOS logic systems
- All types are rated for operation over the range of −55 to +125°C
- Stable V_{IO} vs. time due to source-follower inputs

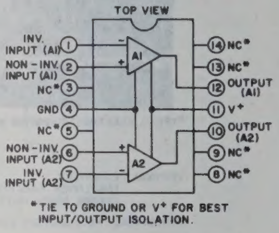
Applications:

- High-source-impedance voltage comparators
- Long time delay circuits
- Square-wave generators
- A/D converters
- Window comparators

TERMINAL ASSIGNMENTS



E SUFFIX



*TIE TO GROUND OR V+ FOR BEST INPUT/OUTPUT ISOLATION.

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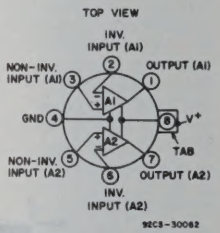
EI SUFFIX



S and T SUFFIX

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
Single Supply:	
CA3290B	+44 V
CA3290A, CA3290	+36 V
Dual Supply:	
CA3290B	±22 V
CA3290A, CA3290	±18 V
DIFFERENTIAL INPUT VOLTAGE	±36 V or ±[(V^+−V^-)+5 V] (whichever is less)
COMMON-MODE INPUT VOLTAGE	V^++5 V to V^-−5 V
DEVICE DISSIPATION:	
Up to 55°C	630 mW
Above 55°C	Derate linearly at 6.67 mW/°C
OUTPUT-TO-V^- SHORT CIRCUIT DURATION*	CONTINUOUS
TEMPERATURE RANGE, ALL TYPES:	
Operating	−55 to +125°C
Storage	−65 to +150°C
INPUT TERMINAL CURRENT	1 mA
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	265°C

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*Short circuits from the output to V^+ can cause excessive heating and eventual destruction of the device.

CIRCUIT DESCRIPTION

The Basic Comparator

Fig. 1 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry-type "139" comparators, with PMOS transistors replacing p-n-p transistors as input stage elements. Transistors Q1 through Q4 comprise the differential input stage, with Q5 and Q6 serving as a mirror-connected active load and differential-to-single-ended converter. The differential input at Q1 and Q4 is amplified so as to toggle Q6 in accordance with the input-signal polarity. For example, if $+V_{IN}$ is greater than $-V_{IN}$, Q1, Q2, and current mirror transistors Q5 and Q6 will be turned off; transistors Q3, Q4, and Q7 will be turned on, causing Q8 to be turned off. The output is pulled positive when a load resistor is connected between the output and V^+.

ELECTRICAL CHARACTERISTICS at T_A = −55 to +125°C

CHARACTERISTIC	TEST CONDITIONS		VALUES						UNITS
			CA3290B		CA3290A		CA3290		
		V^+	Typ.	Max.	Typ.	Max.	Typ.	Max.	
Input Offset Voltage, V_{IO}	V_{IC}=1.4 V, V_O=1.4 V	5 V	3.5	–	4.5	–	8.5	–	mV
	V_{IC}=0 V, V_O=0 V	±15 V	3.5	–	8.5	–	8.5		
Temp. Coefficient of Input Offset Voltage, $\Delta V_{IO}/\Delta T$			8	–	8	–	8	–	µV/°C
Input Offset Current, I_{IO}	V_{IC}=1.4 V	5 V	2	22	2	28	2	32	nA
	V_{IC}=0 V	±15 V	7	22	7	28	7	32	
Input Current, I_I▲	V_{IC}=1.4 V	5 V	2.8	32	2.8	45	2.8	55	nA
	V_{IC}=0 V	±15 V	13	32	13	45	13	55	
Supply Current, I^+*	$R_L = \infty$	5 V	0.85	1.6	0.85	1	0.85	1.6	mA
		30 V	1.62	3.5	1.62	3	1.62	3.5	
Voltage Gain, A_{OL}	R_L=15 kΩ	±15 V	150	–	150	–	150	–	V/mV
			103	–	103	–	103	–	dB
Saturation Voltage	V^+=5 V, 4 mA, $+V_I$=0 V, $-V_I$=1 V	+125°C	0.22	0.7	0.22	0.7	0.22	0.7	V
		−55°C	0.1	–	0.1	–	0.1	–	
Output Leakage Current, I_{OL}		15 V	65	–	65	–	65	–	nA
		36 V	130	1k	130	1k	130	1k	

▲At T_A = +125°C

*At T_A = −55°C

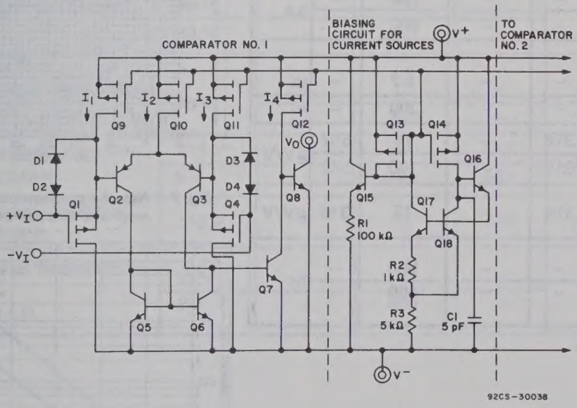


Fig. 2 – Schematic diagram of CA3290 (only one is shown).

In essence, Q1 and Q4 function as source-followers to drive Q2 and Q3, respectively, with zener diodes D1 through D4 providing gate-oxide protection against input voltage transients (e.g., static electricity). The current flow in Q1 and Q2 is established at approximately 50 microamperes by constant-current sources I_1 and I_3, respectively. Since Q1 and Q4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode range. As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential dc voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q7 and Q8. The collector of Q8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink-current capability.

The detailed schematic diagram for one comparator and the common current-source biasing is shown in Fig. 2. PMOS transistors Q9 through Q12 are the current-source elements identified in Fig. 1 as I_1 through I_4, respectively. Their gate-source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right-hand portion of the Fig. 2. The currents supplied by Q10 and Q12 are twice those supplied by Q9 and Q11. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q9 through Q12.

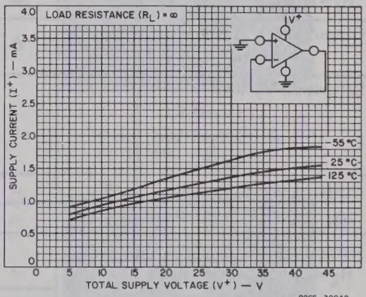


Fig. 3 – Supply current as a function of supply voltage (both amplifiers).

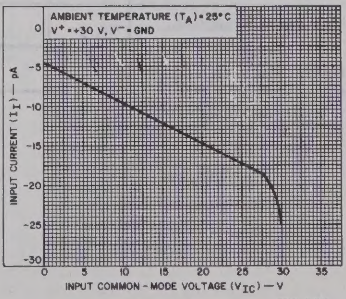


Fig. 4 – Input current as a function of input common-mode voltage.

CA3290, CA3290A, CA3290B

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$

CHARACTERISTIC	TEST COND.	LIMITS						UNITS
		CA3290B			CA3290A			
	V^+	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO} V_{IC}=1.4 V V_O=1.4 V	5 V	–	3	6	–	4	10	mV
V_{IC}=0 V V_O=0 V	±15 V	–	3	6	–	4	10	
Input Current, I_I V_{IC}=1.4 V	5 V	–	3.5	30	–	3.5	40	pA
V_{IC}=0 V	±15 V	–	12	30	–	12	40	
Input Offset Current, I_{IO} V_{IC}=1.4 V	5 V	–	2	20	–	2	25	pA
V_{IC}=0 V	±15 V	–	7	20	–	7	25	
Common-Mode Input-Voltage Range, V_{ICR} V_O=1.4 V	5 V	$V^+-3.5$ V^-	$V^+-3.1$ $V^--1.5$	–	$V^+-3.5$ V^-	$V^+-3.1$ $V^--1.5$	–	V
V_O=0 V	±15 V	$V^+-3.8$ V^-	$V^+-3.4$ $V^--1.6$	–	$V^+-3.8$ V^-	$V^+-3.4$ $V^--1.6$	–	
Supply Current, I^+	30 V	–	1.35	3	–	1.35	3	mA
$R_L = \infty$	5 V	–	0.8	1.4	–	0.8	1.4	
Voltage Gain, A_{OL} R_L=15 kΩ	±15 V	50	800	–	25	800	–	V/mV
		94	118	–	88	118	–	dB
Output Sink Current V_O=1.4 V	5 V	6	30	–	6	30	–	mA
Saturation Voltage $+V_I$=0 V, $-V_I$=1 V, 4 mA	5 V	–	0.12	0.4	–	0.12	0.4	V
Output Leakage Current, I_{OL}	15 V	–	100	–	–	100	–	pA
	36 V	–	500	–	–	500	–	
Response Time R_L=5.1 kΩ Rising Edge	15 V	–	1.2	–	–	1.2	–	µs
Falling Edge		–	200	–	–	200	–	ns
Common-Mode Rejection Ratio, CMRR	±15 V	–	44	316	–	44	562	µV/V
	5 V	–	100	316	–	100	562	
Power-Supply Rejection Ratio, PSRR	±15 V	–	15	316	–	15	316	µV/V
Large-Signal Response Time R_L=5.1 kΩ	15 V	–	500	–	–	500	–	ns
	5 V	–	400	–	–	400	–	

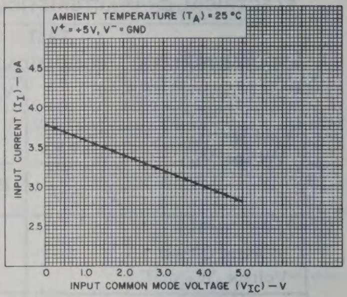


Fig. 5 — Input current as a function of input common-mode voltage.

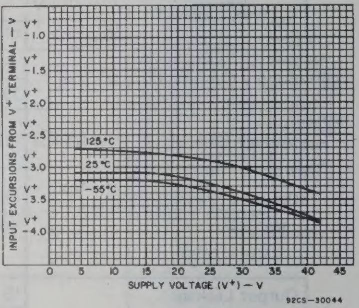


Fig. 6 — Positive common-mode input voltage range as a function of supply voltage.

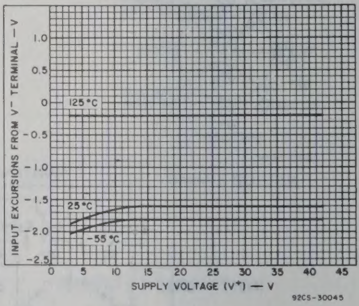


Fig. 7 — Negative common-mode input voltage range as a function of supply voltage.

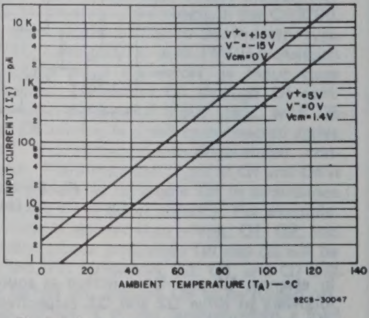


Fig. 8 — Input current as a function of ambient temperature.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTIC	TEST COND. V^+	LIMITS CA3290 Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO} V_{IC}=1.4 V V_O=1.4 V	5 V	–	7.5	20	mV
V_{IC}=0 V V_O=0 V	±15 V	–	7.5	20	
Input Current, I_I V_{IC}=1.4 V	5 V	–	3.5	50	pA
V_{IC}=0 V	±15 V	–	12	50	
Input Offset Current, I_{IO} V_{IC}=1.4 V	5 V	–	2	30	pA
V_{IC}=0 V	±15 V	–	7	30	
Common-Mode Input-Voltage Range, V_{ICR} V_O=1.4 V	5 V	$V^+-3.5$ V^-	$V^+-3.1$ $V^--1.5$	–	V
V_O=0 V	±15 V	$V^+-3.8$ V^-	$V^+-3.4$ $V^--1.6$	–	
Supply Current, I^+ $R_L = \infty$	30 V	–	1.35	3	mA
	5 V	–	0.8	1.4	
Voltage Gain, A_{OL} R_L = 15 kΩ	±15 V	25	800	–	V/mV
		88	118	–	dB
Output Sink Current V_O=1.4 V	5 V	6	30	–	mA
Saturation Voltage $+V_I$=0 V, $-V_I$=1 V, 4 mA	5 V	–	0.12	0.4	V
Output Leakage Current, I_{OL}	15 V	–	100	–	pA
	36 V	–	500	–	
Response Time R_L=5.1 kΩ Rising Edge	15 V	–	1.2	–	μs
Falling Edge		–	200	–	ns
Common-Mode Rejection Ratio, CMRR	±15 V	–	44	562	μV/V
	5 V	–	100	562	
Power-Supply Rejection Ratio, PSRR	±15 V	–	15	316	μV/V
Large-Signal Response Time R_L=5.1 kΩ	15 V	–	500	–	ns
	5 V	–	400	–	

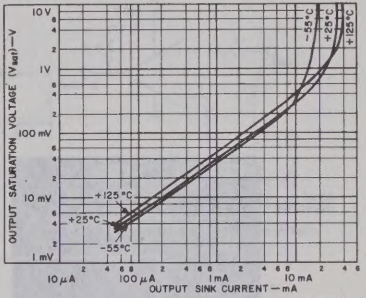
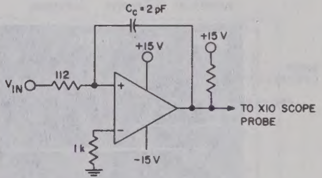
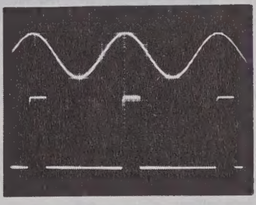
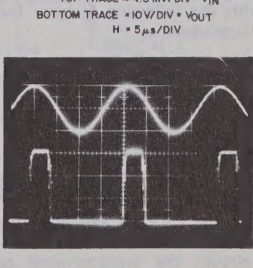


Fig. 9 — Output saturation voltage as a function of output sink current.





WITH C_c
TOP TRACE ≈ 4.5 mV/DIV • V_{IN}
BOTTOM TRACE • 10 V/DIV • V_{OUT}
H • 5 μs/DIV



WITHOUT C_c
TOP TRACE ≈ 4.5 mV/DIV
BOTTOM TRACE • 10 V/DIV
H • 5 μs/DIV

92CM-30059

Fig. 10 — Parasitic-oscillations test circuit and associated waveforms.

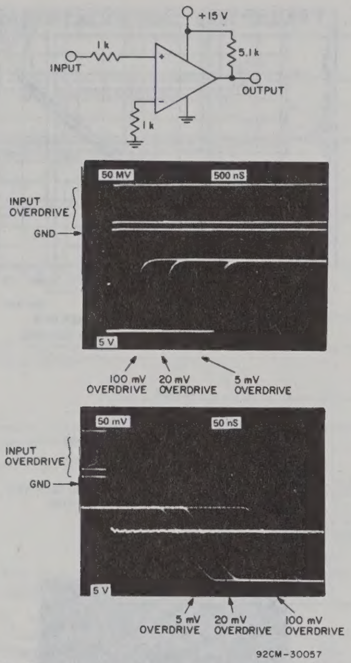


Fig. 11 – Non-inverting comparator response-time test circuit and waveforms.

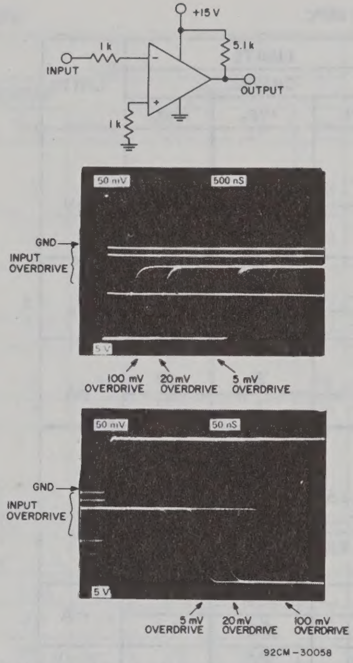


Fig. 12 – Inverting comparator response-time test circuit and waveforms.

OPERATING CONSIDERATIONS

Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra-high input impedance ($\cong 1.7\ T\Omega$);
2. The availability of common-mode rejection for input signals at potentials below that of the negative power-supply rail;
3. Retention of the in-phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input-terminal currents should not exceed 1 mA. Appropriate series-connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel-connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the V^+ terminal of the CA3290.

Parasitic Oscillations

The ideal comparator has, among other features, ultra-high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1 to 10 mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8-lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1 pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, toggling rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1 kΩ a capacitor ($\geqslant$ 1-2 pF) be connected between the appropriate input terminal and the output terminal. (See Fig. 10.)

The CA3290A and CA3290 are also supplied in a 14-lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the V^+ or V^- supply rail. If either comparator is unused, its input terminals should also be tied to either the V^+ or V^- supply rail.

TYPICAL APPLICATIONS

Light-Controlled One-Shot Timer

In Fig. 13 one comparator (A1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A2) is configured as a one-shot timer and is triggered by the output of A1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R1 and R2. The ratio of R1 to R2 should be constant to insure constant reverse voltage bias on the photo diode.

Low-Frequency Multivibrator

In this application, one-half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading.

Window Comparator

Both halves of the CA3290 can be used in a high input-impedance window comparator as shown in Fig. 15. The LED will be turned "on" whenever the input signal is above the lower limit (V_L) but below the upper limit (V_U), as determined by the R1/R2/R3 resistor divider.

LED Bar Graph Driver

The circuit in Fig. 16 demonstrates the use of the CA3290 in a bar graph display. The non-inverting inputs of both comparators are tied to the voltage divider reference and the input signal is applied to both of the inverting inputs. The LED for a particular comparator will be turned "on" when the input voltage reaches the voltage on the resistor divider reference. The CA3290 is ideal for this application where input-signal loading is critical even though many comparator inputs are driven in parallel.

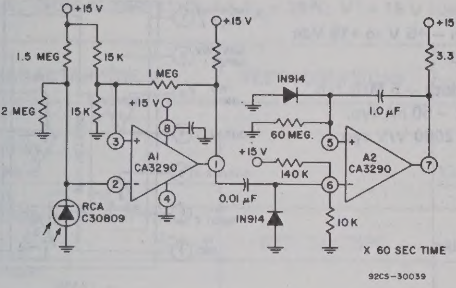


Fig. 13 – Light-controlled one-shot timer.

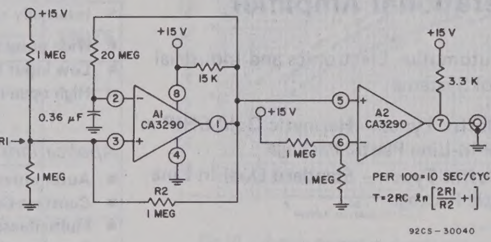


Fig. 14 – Low-frequency multivibrator.

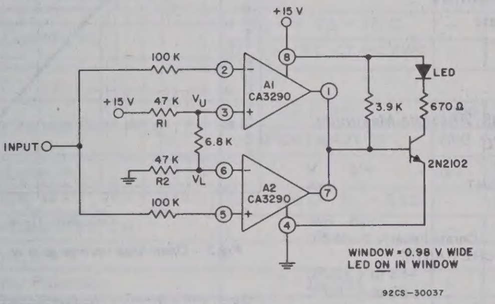


Fig. 15 – Window comparator.

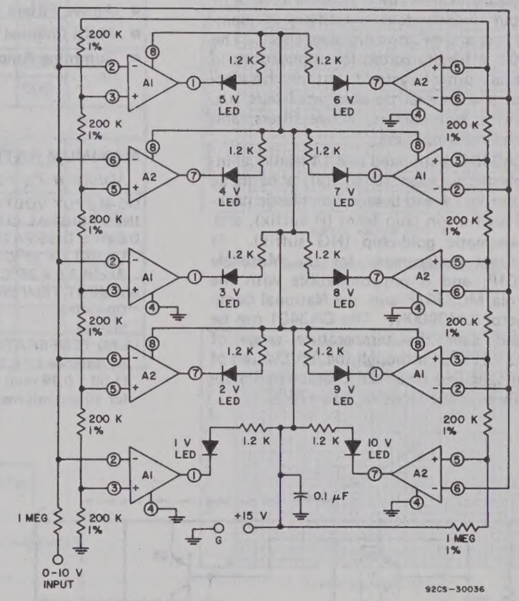
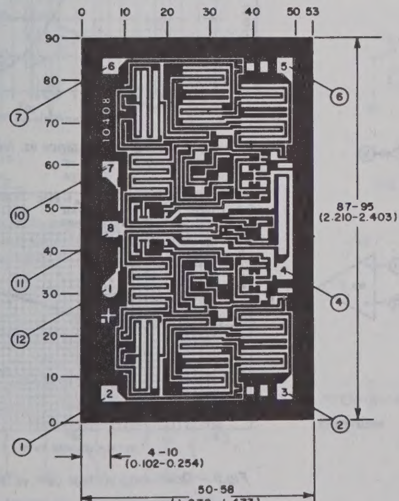


Fig. 16 – LED bar-graph driver.



NOTE: NOS. IN PADS ARE FOR 8-LEAD DIP AND TO-5
NOS. OUTSIDE OF CHIP ARE FOR 14-LEAD DIP

92CM-30091

Dimensions and pad layout for the CA3290H.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3401E, CA3401G

Quad Single-Supply Operational Amplifier

For Automotive Electronics and Industrial Control Systems

"G" Suffix Types — Hermetic Gold-CHIP in Dual-In-Line Plastic Package

"E" Suffix Types — Standard Dual-In-Line Plastic Package

The RCA-CA3401 is a high-gain monolithic quad operational amplifier designed specifically for applications using a single positive power supply. No external compensation is necessary. Closed-loop stability in each of the four independent amplifiers is maintained by a 3-pF on-chip capacitor. The CA3401 is ideally suited for applications in industrial control systems, automotive electronics, and general purpose amplifiers, e.g. oscillators, tachometers, active filters, and multichannel amplifiers.

The CA3401 is supplied in a 14-lead dual-in-line plastic package (E suffix), a hermetic gold-chip in 14-lead dual-in-line plastic package (G suffix), in chip form (H suffix), and as a hermetic gold-chip (HG suffix). It is a direct replacement for the Motorola MC3401P, and is pin-compatible with the Motorola MC3301P and the National Semiconductor LM3900N. The CA3401 can be operated over the temperature range of −55 to +125°C, although the limit values of certain specified electrical characteristics apply only over the range of 0 to +75°C.

Features:

- **Single-supply operation — +5 V to +18 Vdc**
- **Internally compensated**
- **Wide unity-gain bandwidth — 5 MHz typ.**
- **Low input bias current — 50 nA typ.**
- **High open-loop gain — 2000 V/V typ.**

Applications:

- **Automotive**
- **Constant-Current Sources**
- **Multivibrators**
- **Sample and Hold**
- **Square-Wave Generator**
- **Oscillators**
- **Tachometers**
- **Active Filters**
- **Multi-Channel Amplifiers**
- **Summing Amplifiers**

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC SUPPLY VOLTAGE	+18	V
INPUT SIGNAL CURRENT . . .	5	mA
DEVICE DISSIPATION:		
Up to $T_A = 25^oC$	625	mW
Above $T_A = 25^oC$ . . Derate linearly	5	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−55 to + 125	°C
Storage	−65 to + 150	°C
LEAD TEMPERATURE (During soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	300	°C

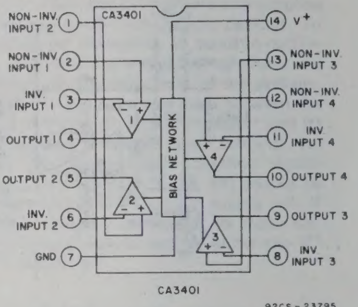


Fig.1 — Block diagram of CA3401.

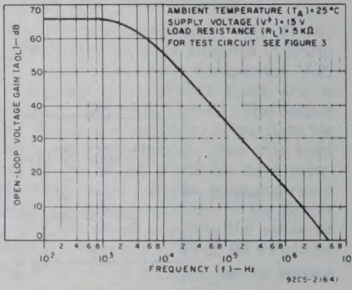


Fig.2 — Open-loop voltage gain vs. frequency.

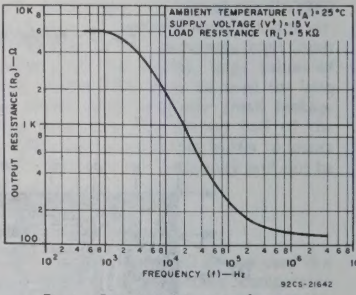


Fig.3 — Output resistance vs. frequency.

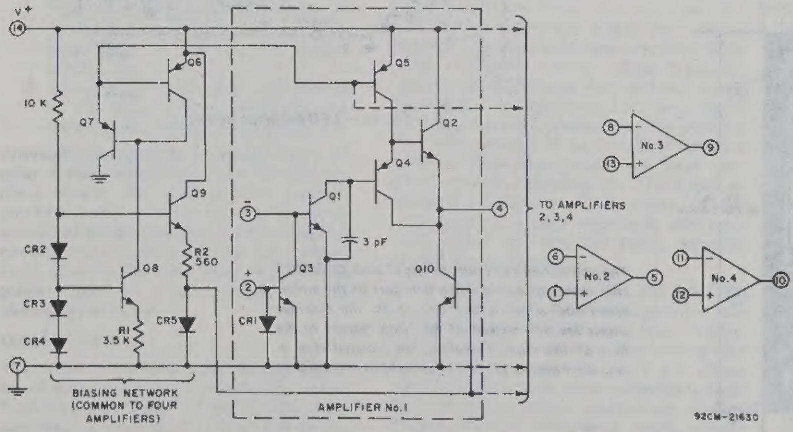


Fig.4 — Schematic diagram of CA3401.

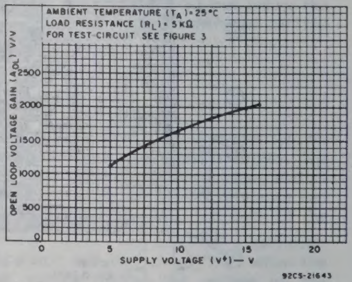


Fig.5 — Open-loop voltage gain vs. supply voltage

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $V^+ = 15$ V (Unless Indicated Otherwise)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
STATIC					
Output Voltage:					
High, V_{OH}		13.5	14.2	–	V
Low, V_{OL}		–	0.03	0.1	
Max. Undistorted Output Swing, V_{OP-P}	$0^oC<T_A<75^oC$	10	13.5	–	
Output Current:					
Source, I_{SOURCE}		5	10	–	mA
Sink, I_{SINK}		0.5	1	–	
Total Quiescent Current: I_Q					
Noninverting inputs open		–	6.9	10	mA
Noninverting inputs grounded		–	7.8	14	
Input Bias Current, I_{IB}	$R_L = \infty$ $T_A = 25^oC$	–	50	300	nA
	$R_L = \infty$ $0^oC \leqslant T_A \leqslant 75^oC$	–	–	500	
DYNAMIC					
Open-Loop Voltage Gain, A_{OL}	$T_A = 25^oC$	1000	2000	–	V/V
	$0^oC \leqslant T_A \leqslant 75^oC$	800	–	–	
Input Resistance, R_I		0.1	1	–	MΩ
Slew Rate, SR	$C_L = 100$ pF, $R_L = 5$ kΩ	–	0.6	–	V/µs
Unity Gain Gandwidth, BW		–	5	–	MHz
Phase Margin, ϕ		–	70	–	Degrees
Power Supply Rejection	f = 100 Hz	–	55	–	dB
Channel Separation, e_{01}/e_{02}	f = 1 kHz	–	65	–	dB

TEST CIRCUITS

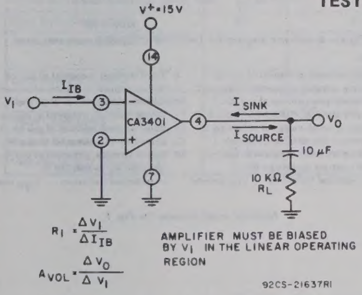

V+=15V
14
I_{IB}
V_I
3
2
CA3401
4
7
I_{SINK}
I_{SOURCE}
V_O
10 µF
10 KΩ
R_L
$R_I = \frac{\Delta V_I}{\Delta I_{IB}}$
$A_{VOL} = \frac{\Delta V_O}{\Delta V_I}$
AMPLIFIER MUST BE BIASED BY V_I IN THE LINEAR OPERATING REGION
92CS-21637RI

Fig.6 – Open-loop gain and input resistance, input bias current and output current test circuit.

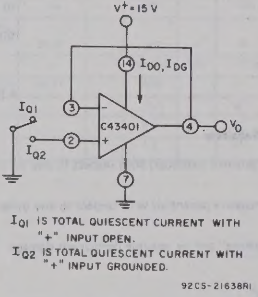

V+=15 V
14
I_{DO}, I_{DG}
I_{Q1}
I_{Q2}
3
2
C43401
4
7
V_O
I_{Q1} IS TOTAL QUIESCENT CURRENT WITH "+" INPUT OPEN.
I_{Q2} IS TOTAL QUIESCENT CURRENT WITH "+" INPUT GROUNDED.
92CS-21638RI

Fig.7 – Quiescent power supply current test circuit.

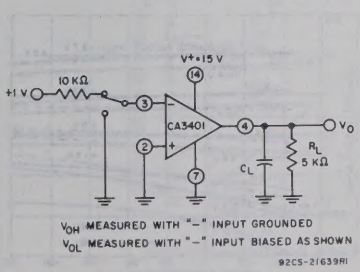

V+=15 V
14
+1 V
10 KΩ
3
2
CA3401
4
7
V_O
C_L
R_L
5 KΩ
V_{OH} MEASURED WITH "–" INPUT GROUNDED
V_{OL} MEASURED WITH "–" INPUT BIASED AS SHOWN
92CS-21639RI

Fig.8 – Output voltage swing test circuit.

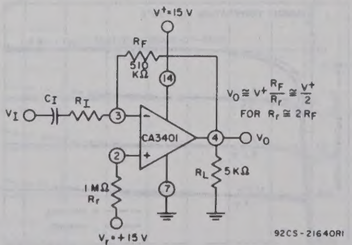


Fig.9 – Peak-to-peak output voltage test circuit.

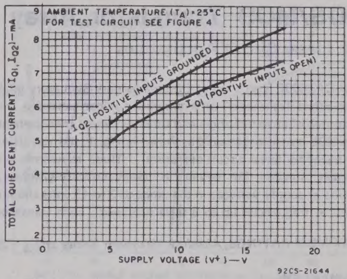


Fig.10 – Supply current vs. supply voltage.

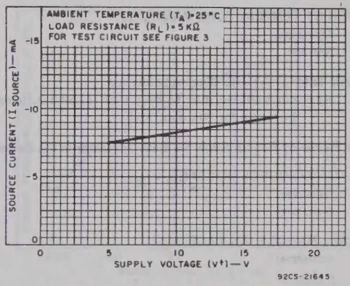


Fig.11 – Source current vs. supply voltage.

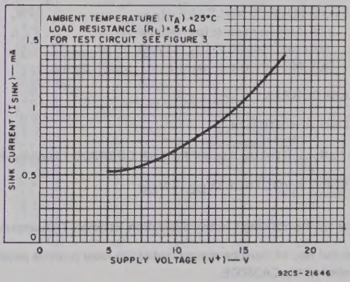


Fig.12 – Sink current vs. supply voltage.

CA3600E

COS/MOS Transistor Array

For Linear Circuit Applications

RCA-CA3600E is an array of COmplementary-Symmetry MOS Field-Effect Transistors* on a monolithic silicon substrate. It is comprised of three n-channel and three p-channel enhancement-type MOS transistors arrayed as shown in Fig. 1, and specified and tested for linear circuit operation. These transistors are uniquely suitable for service in complementary-symmetry circuits at supply voltages in the range of 3 to 15 volts and are useful at frequencies up to 5 MHz (untuned). Each transistor in the CA3600E can conduct currents up to 10 mA. This device is supplied in the 14-lead dual-in-line plastic package.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DISSIPATION:	
Any one transistor at T_A up to 55°C	150 mW
Total package at T_A up to 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering)	
At distance not less than 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

The Following Ratings Apply for Each Transistor in the Device:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}:	
n-channel	+15 V
p-channel	−15 V
DRAIN-TO-GATE VOLTAGE, V_{DG}:	
n-channel	+15 V
p-channel	−15 V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}:	
n-channel	+15 V
p-channel	−15 V
GATE-TO-SOURCE VOLTAGE, V_{GS}:	
p-channel transistors (p_1, p_2, p_3)	0 V(min.),$-V_D$(max.)
n-channel transistors (n_1, n_2, n_3)	0 V(min.),$+V_D$(max.)
COS/MOS transistor-pairs (p_1-n_1, p_2-n_2, p_3-n_3)	0 V(min.),$+V_{DD}$(max.)
DRAIN CURRENT, $\lvert I_D \rvert$	10 mA
GATE CURRENT, $\lvert I_G \rvert$	100 μA

The Following Rating Applies for Each COS/MOS Transistor-Pair in the Device:

DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$)	+15 V

Rules for Maintaining Electrical Isolation Between Transistors and Monolithic Substrate

Terminal No. 14 must be maintained at the most positive potential (or equally positive potential) with respect to any other terminal in the CA3600E.

Terminal No. 7 must be maintained at the most negative potential (or equally negative potential) with respect to any other terminal in the CA3600E.

Violation of these rules will result in improper transistor operation, circuit "latching," and/or possible permanent damage to the CA3600E.

Note: Users should observe the "Considerations in Handling CA3600E Devices"

Features:

- **High input resistance . . . . . . 100 GΩ (typ.)**
- **Low gate-terminal current . . . . 10 pA (typ.)**
- **Matched p-channel pair:**
  - **Gate-voltage differential (I_D = -100 μA) ±20 mV (max.)**
- **No "Popcorn" (burst) noise**
- **Stable transfer characteristics over an operating temperature range of −55°C to +125°C when operated in complementary circuit configuration at supply voltages in the 5 to 15 volt range (see Fig. 14)**
- **Integrated integral gate-protection system (see Fig. 34)**
- **High voltage gain (see Fig. 11). . . up to 53 dB (typ.) per COS/MOS stage**
- **Individual MOS transistors have square-law characteristics, superior cross-modulation performance, and greater dynamic range than bipolar transistors**

Applications:

- **High input impedance, general-purpose amplifiers**
- **Pre-amplifiers**
- **Differential amplifiers**
- **Op-amps and comparators**
- **Constant-current sources and current mirrors**
- **Micropower amplifiers and oscillators**
- **Control of lamps, LED's, relays, and thyristors**
- **Timers**
- **Choppers**
- **Mixers**

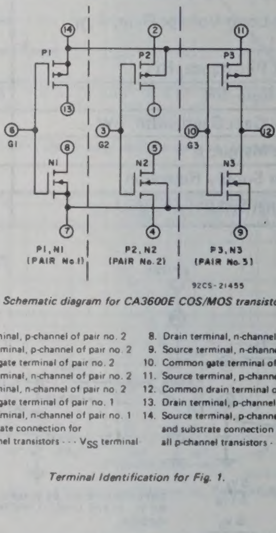


Fig.1 – Schematic diagram for CA3600E COS/MOS transistor array.

1. Drain terminal, p-channel of pair no. 2
2. Source terminal, p-channel of pair no. 2
3. Common gate terminal of pair no. 2
4. Source terminal, n-channel of pair no. 2
5. Drain terminal, n-channel of pair no. 2
6. Common gate terminal of pair no. 1
7. Source terminal, n-channel of pair no. 1 and substrate connection for all n-channel transistors · · · V_{SS} terminal
8. Drain terminal, n-channel of pair no. 1
9. Source terminal, n-channel of pair no. 3
10. Common gate terminal of pair no. 3
11. Source terminal, p-channel of pair no. 3
12. Common drain terminal of pair no. 3
13. Drain terminal, p-channel of pair no. 1
14. Source terminal, p-channel of pair no. 1 and substrate connection for all p-channel transistors · · · V_{DD} terminal

Terminal Identification for Fig. 1.

TYPICAL CHARACTERISTICS CURVES

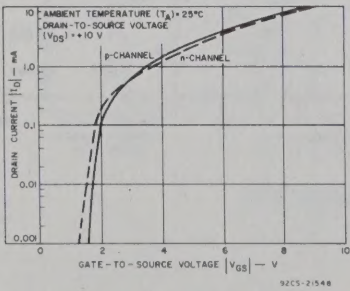


Fig. 2– Drain current vs. gate-to-source voltage.

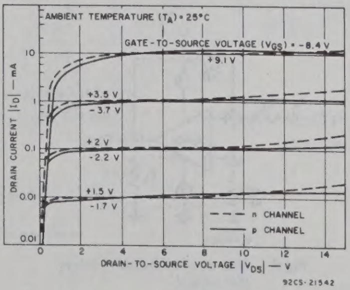


Fig. 3– Drain current vs. drain-to-source voltage.

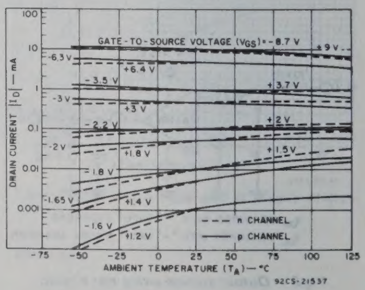


Fig. 4– Drain current vs. ambient temperature.

Formerly RCA Dev. No. TA6368.

* The theory and construction of COS/MOS transistors are described in the "RCA COS/MOS Integrated Circuits Manual," RCA Solid State Division Technical Series Publication No. CMS-271.

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYPICAL CURVE OR CIRCUIT FIG. NO.	LIMITS			UNIT
				Min.	Typ.	Max.	
For Each p-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=−10 V,V_{GS}=−3.6 V	2,3,4	−0.5	−1.1	−2.0	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=−10 μA	–	–	−1.75	–	V
Gate-to-Source Voltage Differential (p_1 vs. p_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=−100 μA,V_{DS}=−10 V	5	–	±4	±20	mV
Forward Transconductance	g_{fs}	I_D=−1 mA,f=1 kHz	6	–	920	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=−1 mA,f=1 kHz,R_s=0 Ω	7	–	0.03	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=−1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.2	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (p_1/p_2)	I_{MTR}	I_1=−100 μA,V_{DS}=−10 V	30	0.7	1.1	1.5	–
Gate-Terminal Current	I_{GT}	V_{DS}=−10 V,V_{GS}=−3.5 V	–	–	±0.015	−40	nA
Input Capacitance	C_I	–	–	–	6.3	–	pF
Output Capacitance	C_O	–	–	–	3	–	pF
Input-to-Output Capacitance	$C_{I\text{-}O}$	–	–	–	0.75	–	pF
For Each n-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=+10 V,V_{GS}=+3.6 V	2,3,4	0.4	0.9	1.6	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=10 μA	–	–	1.5	–	V
Gate-to-Source Voltage Differential (n_1 vs n_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=100 μA,V_{DS}=+10 V	5	–	±30	–	mV
Forward Transconductance	g_{fs}	I_D=1 mA,f=1 kHz	6	–	860	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=1 mA,f=1 kHz,R_s=0 Ω	7	–	0.2	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.3	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (n_1/n_2)	I_{MTR}	I_1=100 μA,V_{DS}=+10 V	29	0.7	1.3	2.0	–
Gate-Terminal Current	I_{GT}	V_{DS}=+10 V,V_{GS}=+3.7 V	–	–	±0.01	+40	nA
Input Capacitance	C_I	–	–	–	5.5	–	pF
Output Capacitance	C_O	–	–	–	2.0	–	pF
Input-to-Output Capacitance	$C_{I\text{-}O}$	–	–	–	0.35	–	pF
For Each COS/MOS Transistor Pair							
Drain Current	I_{DD}	V_{DD}=+10 V	9,10	1.0	2.2	4.0	mA
Drain-to-Source Cutoff Current	$I_{DD(off)}$	V_{DD}=+10 V,V_{SS}=0 V Gate Voltage(V_G)=+10 V or 0 V	8	–	0.5	100	nA
DC Output Voltage	V_O	V_{DD}=+10 V	10	4.2	5.0	5.8	V
Forward Transconductance	g_{fs}	V_{DD}=+10 V, f = 1 kHz	6	–	2300	–	μmho
Slew Rate (Open-Loop)	SR	V_{DD}=+15 V	10	–	95	–	V/μs
Amplifier Voltage Gain	A_{OL}	V_{DD}=+10 V,f=1 kHz,R_b=22 MΩ R_s=50 Ω	10,11	–	32	–	dB
Gate-Terminal Current	I_{GT}	V_{DD}=+10 V	10	–	±0.005	±20	nA
Broadband Output Noise Voltage	E_{ON}	V_{DD}=+10 V,R_b=22 MΩ,R_s=10 kΩ	10,11	–	500		μV
Input Capacitance	C_I	–	–	–	11.8		pF
Output Capacitance	C_O	–	–	–	5.0		pF
Input-to-Output Capacitance	$C_{I\text{-}O}$	–	–	–	1.1		pF

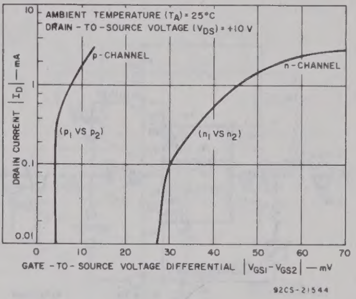


Fig. 5– Gate-to-source voltage differential vs. drain current.

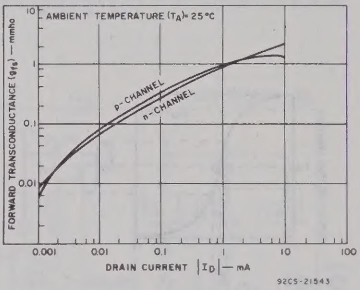


Fig. 6– Forward transconductance vs. drain current.

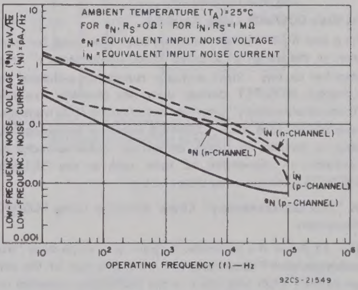


Fig. 7– Noise voltage and noise current vs. operating frequency.

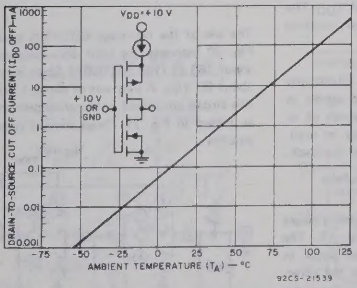


Fig. 8– Drain-to-source cutoff current vs. ambient temperature.

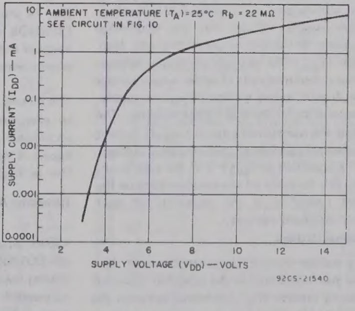


Fig. 9 – Typical V_{DD} vs. I_{DD} characteristics for amplifier circuits of Fig. 10 and Fig. 15.

APPLICATIONS

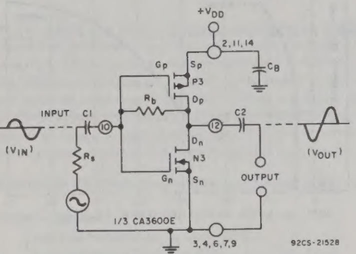


Fig. 10– COS/MOS transistor-pair biased for linear-mode operation.

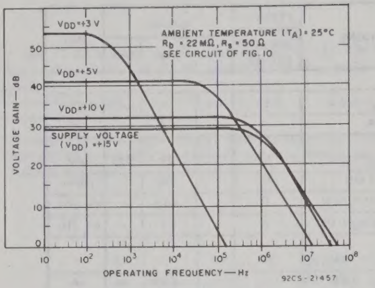


Fig. 11– Typical voltage gain vs. frequency characteristics for amplifier circuit of Fig. 10.

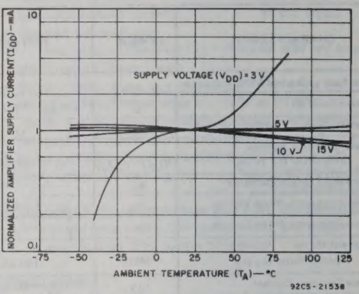


Fig. 12– Normalized amplifier supply current vs. ambient temperature characteristics for amplifier circuit of Fig. 10.

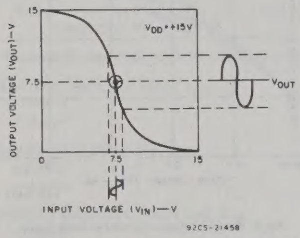


Fig. 13 – Representation of voltage-transfer characteristics for COS/MOS transistor pair.

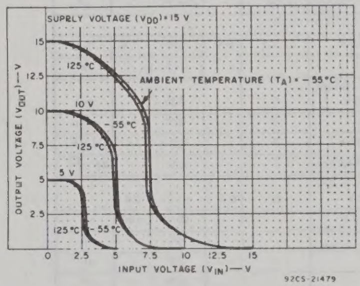


Fig. 14– Voltage transfer characteristics for COS/MOS transistor-pair amplifier in Fig. 10.

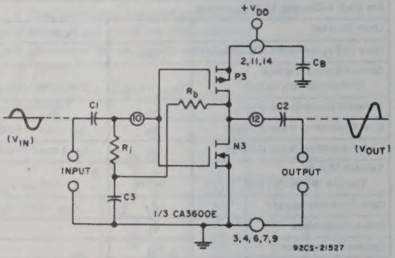


Fig. 15– Alternate method of biasing COS/MOS transistor-pair for linear-mode operation.

The Basic COS/MOS Linear Amplifier

P-n-p and n-p-n bipolar transistors have been used for many years in the design of so-called "true-complementary" linear amplifier circuits . Since mutually compatible p-channel and n-channel MOS/FET devices were not generally available, "true-complementary" amplifier circuits using MOS transistors were seldom used. Now, COS/MOS transistor technology[5] has made it possible to supply compatible p-channel/n-channel transistors in monolithic IC form such as the CA3600E COS/MOS transistor array shown in Fig. 1.

A "True-Complementary" Linear Amplifier Using COS/MOS Transistors

Fig. 10 shows the schematic diagram of a single-stage "true-complementary" linear amplifier using one pair of the complementary MOS transistors in the CA3600E, connected in a common-source circuit. Resistor R_b is used to bias the complementary pair for Class A operation, as described subsequently, and R_s represents the source resistance of the signal source. This generic amplifier is suitable for operation with a single or split voltage supply in the range of 3 to 15 volts. Fig. 11 shows voltage gain as a function of operating frequency at various supply voltages for the single-stage amplifier. This amplifier is capable of producing very high output-swing voltages (V_{out}); for example, its output voltages can be swung to within several millivolts of either supply-voltage "rail". Fig. 9 shows typical supply voltage (V_{DD}) vs. supply current (I_{DD}) characteristics for the single-stage amplifier. The curves in Fig. 12 show the normalized amplifier supply current as a function of ambient temperature at various supply voltages. When the amplifier is operating at V_{DD} = 3 V, the supply current changes rapidly as a function of temperature because the MOS transistors are operating in the proximity of their individual gate-source threshold voltages.

Voltage-Transfer Characteristics

Fig. 13 illustrates a voltage-transfer characteristic curve of a COS/MOS transistor pair connected in the amplifier circuit of Fig. 10, with a biasing resistor (R_b) connected between the drain and gate terminals (10,12). If the p- and n-channel transistors have identical characteristics, their channel resistances are equal, and the biasing method shown establishes a steady-state condition such that terminal 12 is at mid-potential between V_{DD} and ground. Thus, with negligibly small gate-source leakage resistances, under zero-signal conditions, the biasing resistor (R_b) establishes gate potential at the mid-point between V_{DD} and ground, i.e., $V_{in} = V_{out}$. Under these conditions the amplifier is biased for operation about the mid-point ("0") in the linear segment on the steep transition of the voltage-transfer characteristic as shown in Fig. 13. When the input signal (V_{in}) swings in the positive direction, there is a reduction in the instantaneous output voltage (V_{out}) with respect to ground. Negative-going input signals have inverse effects. Thus, phase-inversion occurs in the COS/MOS-pair amplifier. Power-supply current is constant during dynamic linear operation, i.e., Class A amplifier service. When the signal input-voltage level (V_{in}) becomes very large, the output signal (V_{out}) waveforms become distorted because the transistors are driven into the non-linear portions of their voltage-transfer characteristics. If the positive-going input-signal is sufficiently large, for example, the p-channel transistor can be driven to cutoff and the amplifier supply current (I_{DD}) is reduced to essentially zero.

Fig. 14 shows typical voltage-transfer characteristics of each COS/MOS pair in the CA3600E at several values of V_{DD}. The shape of these transfer characteristics is comparatively constant despite temperature changes from −55 to +125°C.

The biasing arrangement used in the circuit of Fig. 10 provides an easy method of establishing feedback for ac signals in accordance with the R_b/R_s ratio. When the feedback of ac signals is not desirable, the circuit of Fig. 15 may be used. The ac bypass capacitor (C_3) minimizes ac signal feedback.

Cascading Amplifier Stages of COS/MOS Transistor Pairs

Ultra-high-gain amplifiers can be designed by cascading stages of COS/MOS transistor pairs as shown in Fig. 16. The biasing system used is similar to that described above in connection with Fig. 10. The supply current for the three-stage amplifier shown in Fig. 16 is typically three times the values shown in Fig. 9. Gain and frequency-response characteristics of the amplifier are shown in Fig. 17.

Post-Amplifiers For Op-Amps

COS/MOS transistor-pairs can be advantageously applied as post-amplifiers for op-amps. Because the input impedance of the COS/MOS pair is comparatively high, the op-amp operates under essentially unloaded conditions. Each COS/MOS pair can sink and source output current up to about 10 mA. Additionally, the op-amp output can be directly coupled to bias the COS/MOS pair. A detailed description of the subject has been published previously.

The schematic diagram in Fig. 18 shows a COS/MOS transistor-pair serving as a post-amplifier to an RCA-CA3080 Operational Transconductance Amplifier. The approximate 30-dB gain in a single COS/MOS transistor-pair is an added increment to the 100-dB gain in the CA3080, yielding a total forward gain of about 130 dB. The open-loop slew rate of the circuit in Fig. 19 is approximately 65 V/µs. When compensated for the unity-gain voltage-follower mode shown in Fig. 19, the slew rate is about 1 V/µs. For greater current output, the two remaining transistor pairs of the CA3600E may be connected in parallel with the single stages shown in Figs. 18 and 19.

The use of the two-stage COS/MOS post-amplifier shown in Fig. 20 increases the total open-loop gain of the system to about 160 dB (100,000,000X). Open-loop slew rate remains at about 65 V/µs. A slew rate of about 1 V/µs is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 21. These circuits operate in concert with stability.

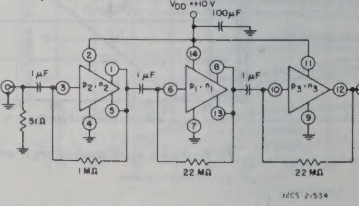


Fig. 16– High-gain amplifier uses cascaded COS/MOS transistor-pair in CA3600E.

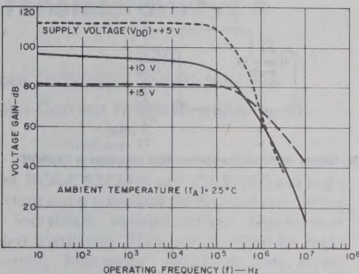


Fig. 17– Typical voltage gain vs. operating frequency characteristics for three-stage COS/MOS transistor-pair amplifier in Fig. 16.

Multivibrators, Threshold Detectors, and Comparators

Descriptions of several circuits using COS/MOS transistor-pairs in both monostable and astable multivibrators have been published. The characteristics of COS/MOS pairs are also ideal for mating with micropower op-amps in circuits such as the precision multistable circuits shown in Fig. 22. In these circuits precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080 Operational Transconductance Amplifier. Moreover, speed vs. power consumption tradeoffs can be made by adjustment of the Amplifier-Bias-Current (I_{ABC}) supplied to terminal 5 of the CA3080. The quiescent power consumption of the circuits shown in Fig. 22 is typically 6 mW, but can be made to operate in the micropower region by suitable modifications.

The schematic diagram of a programmable micropower comparator, shown in Fig. 23 employs the combination of an op-amp (CA3080A) and COS/MOS transistor-pairs in the CA3600E. Quiescent power consumption of the circuit is about 10 μW(typ.). When the comparator is strobed "ON", transistor P1 is driven into conduction and the OTA becomes active. Under these conditions, the circuit consumes 420 μW and responds to a differential-input signal in about 8 μs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 ns but the power consumption is increased to 21 mW. The differential amplifier input common-mode range for this circuit is −1 V to +10.5 V. Voltage gain of this micropower comparator is typically 130 dB.

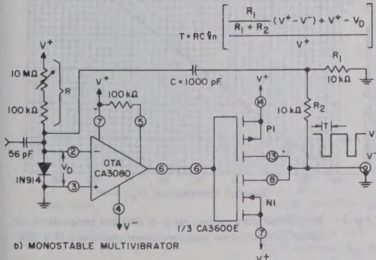


Fig. 22– Multistable circuits using COS/MOS transistor-pairs.

APPLICATIONS – Post-Amplifiers for Op-Amps (Cont'd)

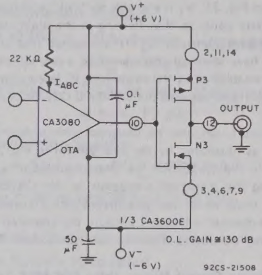


Fig. 18– COS/MOS transistor-pair used as post-amplifier to op-amp in open-loop circuit.

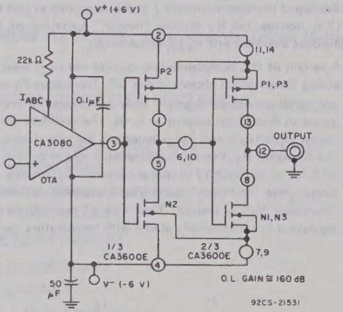
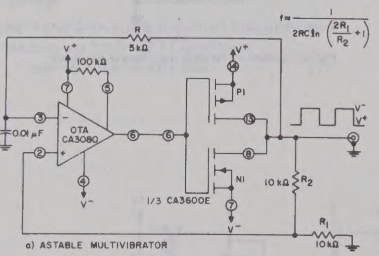


Fig. 20– COS/MOS transistor-pairs used as two-stage post-amplifier to op-amp in open-loop circuit.



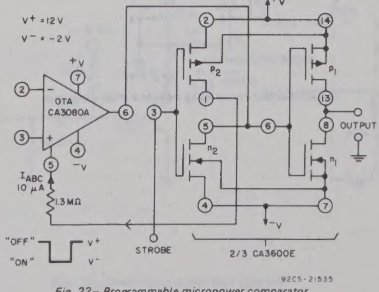


Fig. 23– Programmable micropower comparator.

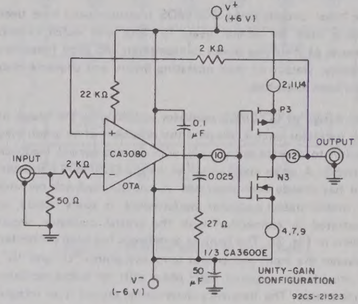


Fig. 19– COS/MOS transistor-pair used as post-amplifier to op-amp in unity-gain circuit.

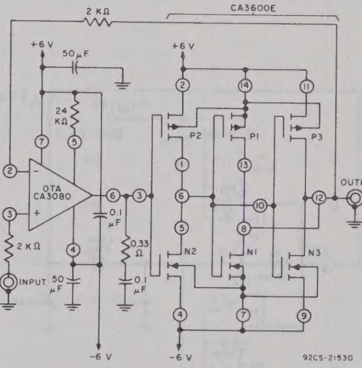
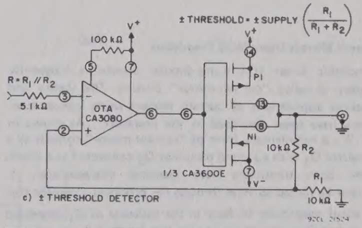


Fig. 21– Unity-gain amplifier uses COS/MOS transistor-pairs as two-stage post-amplifier to op-amp.



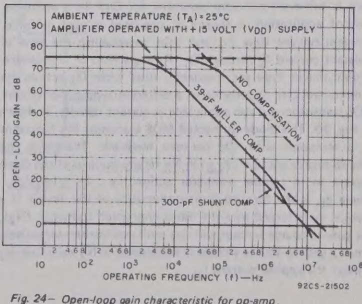


Fig. 24– Open-loop gain characteristic for op-amp.

Oscillator Circuits

Oscillator circuits using COS/MOS transistor-pairs have been widely used for several years in clock and watch circuits because of their low power consumption and good frequency stability. Details of their operating theory and characteristics have been published.

The design of COS/MOS oscillator circuits, like the design of any oscillator circuit, involves the provision of an amplifying section to operate compatibly with an appropriaté feedback network. A single stage amplifier using a COS/MOS transistor-pair has already been described. A suitable feedback network to insure stable oscillator performance is easily added, as illustrated in connection with the crystal oscillator circuit shown in Fig. 25. The familiar pi-network has been connected between the input and output terminals, points "D" and "G", to provide the required 180° phase shift for stable oscillator performance. The frequency-determining crystal is an integral part of the pi-network feedback circuit. The resistors R_1 and R_2 decrease the total power consumption of the oscillator at a particular supply voltage and enhance the frequency stability. Variable frequency oscillators can be built by replacing the crystal with an appropriate inductance and tuning the pi-network by conventional means.

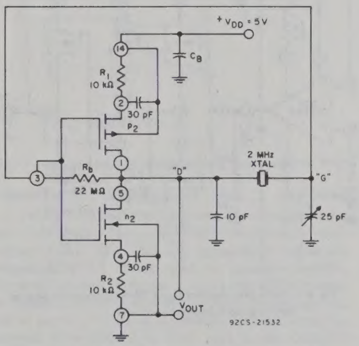


Fig. 25– Typical crystal-oscillator circuit using COS/MOS transistor-pair (1/3 CA3600E).

Current Mirrors Using MOS Transistors

Monolithic linear IC's using bipolar transistors frequently employ so-called "current-mirror" circuits. The theory and practical applications of current mirrors using bipolar transistors have been described in the literature. As shown in Fig. 26, a rudimentary form of "current-mirror" consists of a transistor Q_1 with a second transistor Q_2 connected as a diode. When both transistors have identical characteristics, a current I_1 forced to flow through Q_2 produces a current (I_2) of equal magnitude to flow in the collector of Q_1 (provided there is sufficient collector potential for Q_1). In a common form of application, a source of potential is used to force constant-current flow I_1, and thus to establish the flow of constant current I_2 through Q_1. Arrangements of this generic current-mirror type are frequently used when Q_1 acts as the common-emitter impedance in a differential-amplifier circuit. MOS transistors are also applicable as current mirrors, as shown in Fig. 29. The diode-connected MOS transistor N_2 functions as a transistor with 100 per-cent feedback. Therefore, the gate-to-source voltage (V_{GS}) in N_2 retains control of the drain current as in normal transistor action, i.e., $I_D \cong g_{fs}V_{GS}$, where g_{fs} is the forward transconductance of the device. If a current I_1 is forced into the diode-connected transistor (N_2), the gate-to-source voltage will rise until equilibrium is reached. Thus, a gate-to-source voltage is established in N_2 such that N_2 "sinks" the applied current I_1.

If the gate and source terminals of another transistor (N_1) are connected in shunt with the gate and source terminals of N_2, as shown in Fig. 27, N_1 is also able to "sink" a mirror current approximately equal to that flowing in the drain lead of the diode-connected transistor N_2. It is assumed that both MOS transistors have identical characteristics, a prerequisite that is essentially established by the monolithic IC fabrication technology used in manufacturing the CA3600E COS/MOS transistor array.

Current mirrors can also be designed with p-channel MOS transistors as illustrated by the arrangement in Fig. 30 using transistors in the CA3600E. The characteristics of a current mirror using the p-channel transistors in the CA3600E are superior to those which can be achieved with a current mirror using the n-channel transistors because the characteristics of the p-channel transistors are more nearly matched. The data

Complementary Current Mirrors Using COS/MOS Transistor-Pairs

COS/MOS transistor-pairs can be applied advantageously in the design of Complementary Current-Mirrors, as shown in Fig. 30. Transistors P_1 and N_1 are series-connected and biased for linear operation as previously described, so that there is a current flow I_{D1} through P_1 and N_1. The potential developed between terminals 13 and 14 is applied as gate-source (2,3) voltage for P_2, forcing "mirror" operation of P_2 to produce a current source $I_{D2\text{-}P}$ equal to I_{D1}. Likewise, the potential developed between terminals 7 and 8 is applied as gate-source (3,4) voltage for N_2 forcing "mirror" operation of N_2 to produce a current-sink $I_{D2\text{-}N}$ equal to I_{D1}.

A variant of this complementary current mirror is used in the analog timer circuit shown in Fig. 28. Transistors P_2 and N_2 are series-connected together with a 60-megohm resistor to establish their drain current at 5 nA. The potential developed across terminals 1 and 2 also appears as the gate-source voltage for transistor P_1, thereby establishing a mirror-current source of 5 nA at terminal 13 to charge capacitor C_1 linearily. In this circuit, the "mirrored" current-sink available at terminal 8 (transistor N_1) is unused. This type of current-mirror configuration is exceptionally stable with temperature variations.

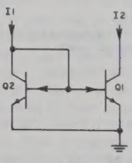


Fig. 26– Current mirror using n-p-n bipolar transistors.

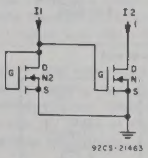


Fig. 27—Current mirror using n-channel MOS transistors.

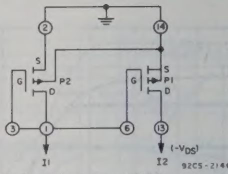


Fig. 28--Current mirror using p-channel MOS transistors in CA3600E.

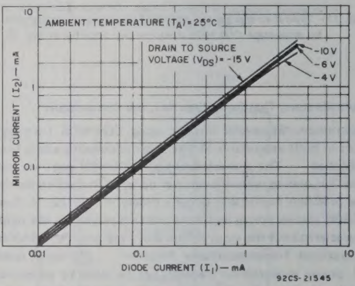


Fig. 29– Characteristics of current mirror circuit of Fig. 30 using p-channel transistors.

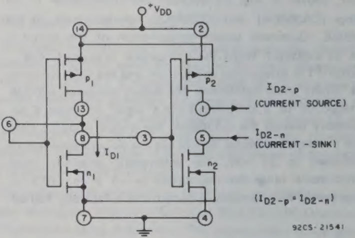


Fig. 30– Complementary current mirrors using COS/MOS transistor-pairs in CA3600E.

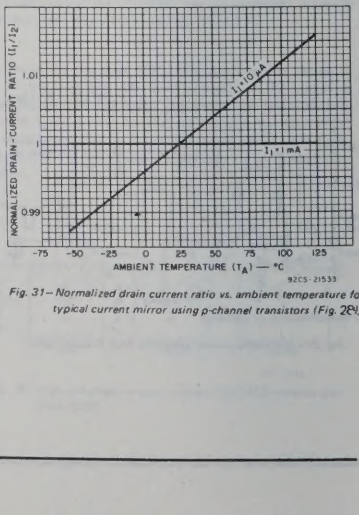


Fig. 31– Normalized drain current ratio vs. ambient temperature for typical current mirror using p-channel transistors (Fig. 28).

CA3724G, CA3725G

High-Current N-P-N Transistor Arrays

Four Individual Sealed-Junction High-Current N-P-N Transistors

The RCA-CA3724G and -CA3725G are high-current n-p-n transistor arrays each containing 4 individual sealed-junction high-current n-p-n transistors. They are intended for high-current, high-speed switching and driver applications.

These devices are alike except for breakdown voltage ratings.

The CA3724G and CA3725G are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of −55°C to +125°C. The transistor chips used in these packages are of the sealed-junction type to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure.

The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

Applications:

- Core-Memory Driver
- High-Speed Switching
- High-Current LED Driver
- High-Voltage Switching
- Relay and Solenoid Driver
- Lamp Driver

Features:

- High Current – 1 A
- High Breakdown Voltage:
  CA3725G = 80 V dc min. $V_{(BR)CES}$ @ I_C = 10 µA
  CA3724G = 70 V dc min. $V_{(BR)CES}$ @ I_C = 10 µA
- Fast Switching Speeds:
  t_{on} = 30 ns typ. @ I_C = 500 mA
  t_{off} = 36 ns typ. @ I_C = 500 mA
- "Hermetic Chip" Construction
- Silicon Nitride Passivated
- Platinum Silicide Ohmic Contacts
- Gold Chip-Metallization
- Electrically similar and pin compatible with industry types MPQ3724, MPQ3725; FPQ3724, FPQ3725; DH3724, DH3725; SP3724, SP3725 in similar packages

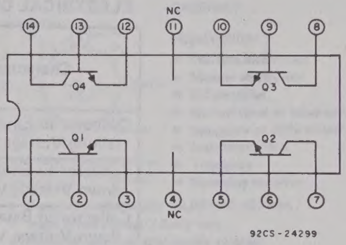


Fig. 1—Terminal diagram (top view).

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

		CA3724G	CA3725G	
COLLECTOR-TO-EMITTER VOLTAGE With Base Open	V_{CEO}	40	50	V
COLLECTOR-TO-BASE VOLTAGE With Emitter Open	V_{CBO}	70	80	V
EMITTER-TO-BASE VOLTAGE With Collector Open	V_{EBO}	6	6	V
COLLECTOR CURRENT	I_C	1.0	1.0	A
POWER DISSIPATION: At T_A up to 25°C:	P_D			
For Each Transistor		1.0	1.0	W
Total Package		2.0	2.0	W
At T_A above 25°C derate linearly		20		mW/°C
AMBIENT TEMPERATURE RANGE:				
Operating		−55 to +125	−55 to +125	°C
Storage		−65 to +150	−65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/32" (3.17 mm) from seating plane for 10 s max.		300	300	°C

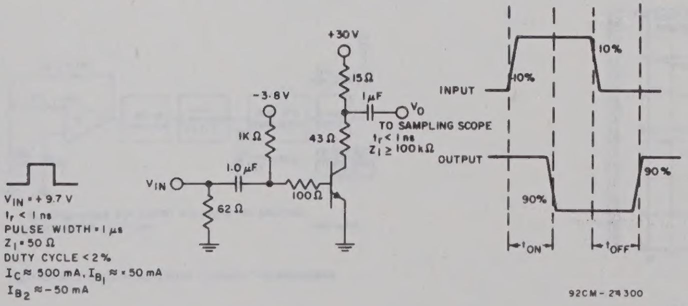


Fig. 2—Switching time test circuit.

CA3724G, CA3725G

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

Characteristic	Test Conditions	Limits						Units
		CA3724G			CA3725G			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO}(sus)$*	I_C=10 mA, I_B=0	40	–	–	50	–	–	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C=10 μA, I_B=0	70	–	–	80	–	–	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	I_C=10 μA, I_E=0	70	–	–	80	–	–	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	I_E=10 μA, I_C=0	6	–	–	6	–	–	V
Base-to-Emitter Saturation Voltage, $V_{BE}(sat)$*	I_C=500 mA, I_B=50 mA	0.75	–	1.0	0.75	–	1.0	V
Collector-to-Emitter Saturation Voltage, $V_{CE}(sat)$*	I_C=500 mA, I_B=50 mA	–	–	0.5	–	–	0.5	V
Collector-Cutoff Current, I_{CBO}	V_{CB}=40 V, I_E=0	–	–	1.7	–	–	1.7	μA
Static Forward-Current Transfer Ratio (Beta), h_{FE}	I_C=100 mA, V_{CE}=1.0 V	35	–	–	35	–	–	
	I_C=500 mA, V_{CE}=1.0 V	30	–	–	30	–	–	
	I_C=1 A, V_{CE}=1.0 V	20	–	–	20	–	–	
Small-Signal Forward-Current Transfer Ratio, h_{fe}	I_C=50 mA, V_{CE}=10 V, f=100 MHz	2.0	–	–	2.0	–	–	
Turn-On Time (See Test Ckt. Fig. 2), t_{on}	I_C=500 mA, I_{B1}=50 mA	–	–	40	–	–	40	ns
Turn-Off Time (See Test Ckt. Fig. 2), t_{off}	I_C=500 mA, I_{B1}=I_{B2}=50 mA	–	–	60	–	–	60	ns
Emitter-to-Base Capacitance, C_{eb}	I_C=0, V_{EB}=0.5 V	–	95	–	–	95	–	pF
Collector-to-Base Capacitance, C_{cb}	I_E=0, V_{CB}=10 V	–	12	–	–	12	–	pF

*Pulse Conditions: width = 300 μs; duty cycle = 1%.

CA6078, CA6741 Types

Operational Amplifiers

CA6078AT – Micropower Type
CA6741T – General-Purpose Type

For Applications where Low Noise (Burst + 1/f) is a Prime Requirement

Virtually free from "popcorn" (burst) noise: device rejected if any noise burst exceeds 20 μV (peak), referred to input over a 30-second time period.

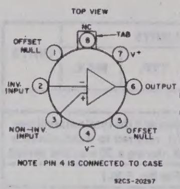
RCA-CA6078AT and CA6741T are low-noise linear IC operational amplifiers that are virtually free of "popcorn" (burst) noise.

These low-noise versions of the CA3078AT and CA3741T are a result of improved processing developments and rigid burst-noise inspection criteria. A highly selective test circuit (See Fig. 2) assures that each type meets the rigid low-noise standards shown in the data section. This low-burst-noise property also assures excellent performance throughout the 1/f noise spectrum.

In addition the CA6078AT and CA6741T offer the same features incorporated in the CA3078AT and CA3741T respectively, including output short-circuit protection, latch-free operation, wide common-mode and differential-mode signal ranges, and low-offset nulling capability.

For detailed data, characteristics curves, schematic diagram, dimensional outline, and test circuits, refer to the Operational Amplifier Data Bulletins File No. 531 and 535. In addition, for details of considerations in burst-noise measurements, refer to Application Note, ICAN-6732, "Measurement of Burst ("Popcorn") Noise in Linear IC's".

The CA6078AT and CA6741T utilize the hermetically sealed 8-lead TO-5 type package. The CA6078AT and the CA6741T can also be supplied on request with dual-in-line formed leads. These types are identified as the CA6078AS and CA6741S. This formed-lead configuration conforms to that of the 8-lead dual-in-line (Mini–Dip) package.



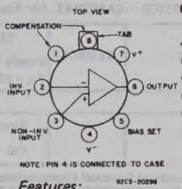
CA6741T

Applications:

- Low-noise AC amplifier
- Narrow-band or band-pass filter
- Integrator or differentiator
- DC amplifier
- Summing amplifier

Features:

- Internal phase compensation
- Input bias current: 500 nA max.
- Input offset current: 200 nA max.
- Open-loop voltage gain: 50,000 (94 dB) min.
- Input offset voltage: 5 mV max.



CA6078AT

Applications:

- Portable electronics
- Medical electronics
- DC amplifier
- Narrow-band or band-pass filter
- Integrator or differentiator
- Instrumentation
- Telemetry
- Summing amplifier

Features:

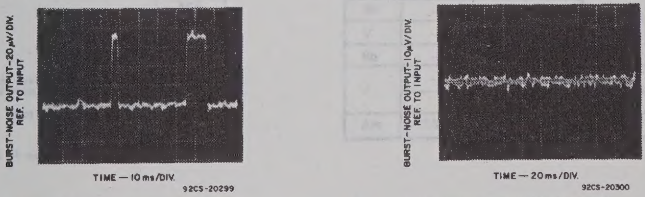
- Open-loop voltage gain: 40,000 (92 dB) min.
- Input offset voltage:3.5 mV max.
- Operates with low total supply voltage: 1.5 V min. (± 0.75 V)
- Low quiescent operating current: adjustable for application optimization
- Input bias current: adjustable to below 1 nA

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

	CA6741T	CA6078AT
DC Supply Voltage (between V+ and V– terminals)	44 V	36 V
Differential-Mode Input Voltage	±30 V	±6 V
Common-Mode DC Input Voltage▲	±15 V	V+ to V–
Device Dissipation:		
Up to 75°C (CA6741T), Up to 125° (CA6078AT)	500 mW	250 mW
Above 75°C	Derate linearly 5 mW/°C	–
Temperature Range:		
Operating	–55 to +125 °C	–55 to +125 °C
Storage	–65 to +150 °C	–65 to +150 °C
Output Short-Circuit Duration●	No limitation	No limitation
Lead Temperature (During soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	300 °C	300 °C

▲If Supply Voltage is less than ±15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

●Short circuit may be applied to ground or to either supply.



a. Typ. device with high-burst-noise characteristic.

b. Typ. device controlled for burst noise.

Fig.1–Typ. waveforms of type with high burst noise and type controlled for burst noise.

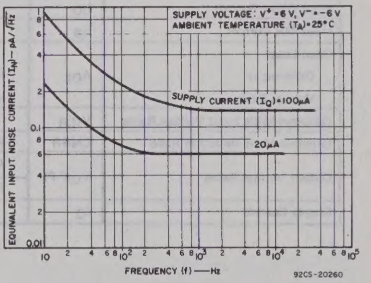


Fig.3–I_N vs. Frequency for CA6078AT.

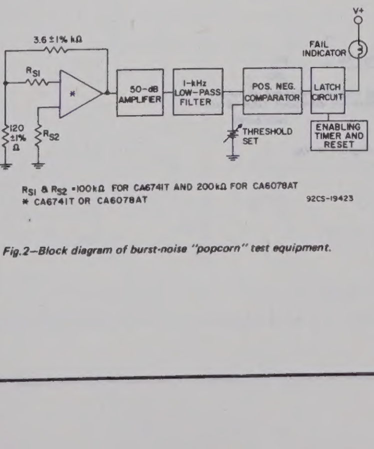


Fig.2–Block diagram of burst-noise "popcorn" test equipment.

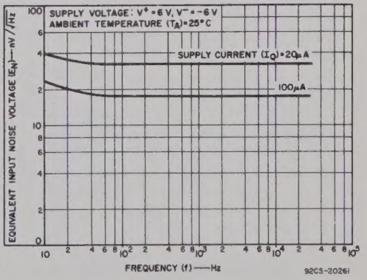


Fig.4–E_N vs. Frequency for CA6078AT.

CA6078, CA6741 Types

ELECTRICAL CHARACTERISTICS – CA6078AT, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts: $V^+ = 6$, $V^- = -6$ $T_A = 25^oC$, $I_Q = 20\ \mu A$	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{SI} = R_{S2} = 200\ k\Omega$	Device is rejected if the total noise voltage (burst + 1/ƒ), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3078AT Data Bulletin, File No. 535.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	0.7	3.5	mV
Input Offset Current	I_{IO}		–	0.5	2.5	nA
Input Bias Current	I_{IB}		–	7	12	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 10\ k\Omega$	40,000	100,000	–	
		$V_O = \pm 4V$	92	100	–	dB
Common-Mode Input Voltage Range	V_{ICR}	$V^+ = V^- = 15\ V$	±14	–	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	80	115	–	dB
Output Voltage Swing	$V_{O(P\text{-}P)}$	$R_L \geq 10\ \Omega$	±13.7	±14.1	–	V
		$R_L \geq 2\ k\Omega$	–	±14	–	
Supply Current	I_Q		–	20	25	μA

ELECTRICAL CHARACTERISTICS – CA6741T, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts; $V^+ = 15$, $V^- = -15$ $T_A = 25^oC$	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{S1} = R_{S2} = 100\ k\Omega$	Device is rejected if the total noise voltage (burst + 1/ƒ), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3741T Data Bulletin, File No. 531.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	1	5	mV
Input Offset Current	I_{IO}		–	20	200	nA
Input Bias Current	I_{IB}		–	80	500	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2\ k\Omega$	50,000	200,000	–	
		$V_O = \pm 10\ V$	94	106	–	dB
Common-Mode Input Voltage Range	V_{ICR}		±12	±13	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\ \Omega$	70	90	–	dB
Output Voltage Swing	$V_{O(P\text{-}P)}$	$R_L \geq 10\ k\ \Omega$	±12	±14	–	V
		$R_L \geq 2\ k\ \Omega$	±10	±13		
Supply Current	I_Q		–	1.7	2.8	mA

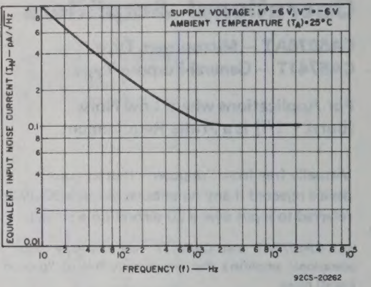


Fig.5–I_N vs. Frequency for CA6741T.

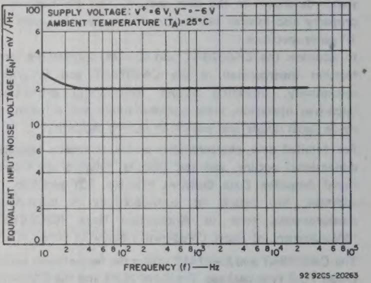


Fig.6–E_N vs. Frequency for CA6741T.

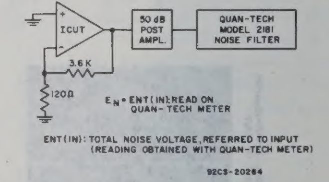
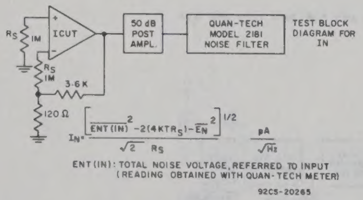

+
ICUT
−
50 dB
POST
AMPL.
QUAN-TECH
MODEL 2181
NOISE FILTER
3.6 K
120Ω
EN = ENT(IN): READ ON QUAN-TECH METER
ENT(IN): TOTAL NOISE VOLTAGE, REFERRED TO INPUT (READING OBTAINED WITH QUAN-TECH METER)
92CS-20264

Fig.7–Test block diagram for E_N.



$$I_N = \frac{\left[\overline{ENT(IN)}^{\,2} - 2(4KTR_S) - \overline{E_N}^{\,2}\right]^{1/2}}{\sqrt{2}\ R_S}\qquad \frac{pA}{\sqrt{Hz}}$$

Fig.8–Test block diagram for I_N.

Linear Integrated Circuits for Consumer Applications

Technical Data

CA270 Types

TV Synchronous Demodulators

For Color and Black-and White TV Systems

The RCA-CA270AW, CA270BW, and CA-270CW are integrated circuits which perform the functions of synchronous detection of the TV if, video amplification and buffering, and noise inversion on dual-polarity waveforms. These devices also offer agc and afc facilities for use with n-p-n transistor if amplifiers and tuners. Both positive and negative polarities of video output are available. This feature provides great flexibility by permitting the designer to use either output for deriving the video and sound channels.

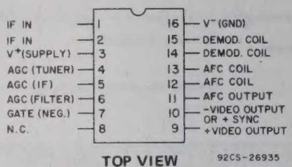
The RCA-CA270 series is pin-compatible and electrically similar to the industry series TCA270, but incorporates several improved features. In particular, improved white noise inversion and sync inversion systems force overshoots in the video waveform to be returned to accurately defined potentials. This design effectively removes dependence on both the degree of overshoot and temperature variations. In addition, reduced current consumption assures lower over-all power dissipation, thereby improving reliability.

The three types are electrically identical in most parameters. The CA270B has the most stringent limits on white level, video inversion, and afc dc offset. The CA270C has the least stringent limits on white level and video inversion, and no afc limits.

The CA270 series is supplied in a 16-lead staggered quad-in-line plastic package ("W" suffix).

Features:

- **Synchronous detector with single tuned coil**
- **Provides rf and if agc (forward)**
- **Tuner afc available with single quadrature coil**
- **Dual-polarity noise inverters**
- **Video amplifier**
- **Positive- and negative-polarity buffered video**
- **Differential if input**
- **Optional use of gating pulse**
- **Low-voltage, single-polarity power supply**



Terminal assignment.

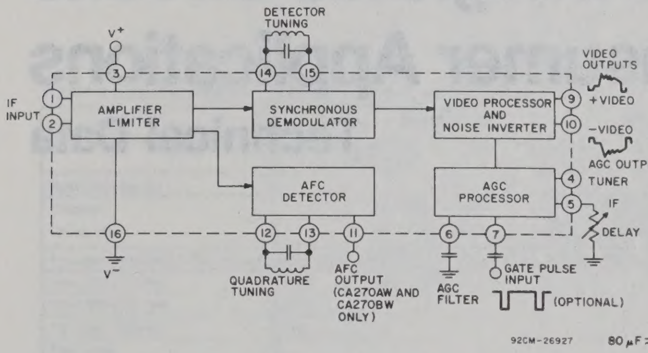


Fig. 1—Functional block diagram of CA270AW, CA270BW, and CA270CW TV synchronous demodulator.

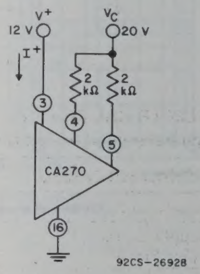


Fig. 2—Supply-current test circuit.

MAXIMUM RATINGS,

Absolute-Maximum Values at T_A=25°C:

DC SUPPLY VOLTAGE (Between Terminals 3 and 16 for 10 s max., with current limited to 100 mA) .... 18 V

DEVICE DISSIPATION:

Up to T_A = 55°C .... 750 mW

Above T_A = 55°C ... derate linearly 7.9 mW/°C

OPERATING TEMPERATURE RANGE

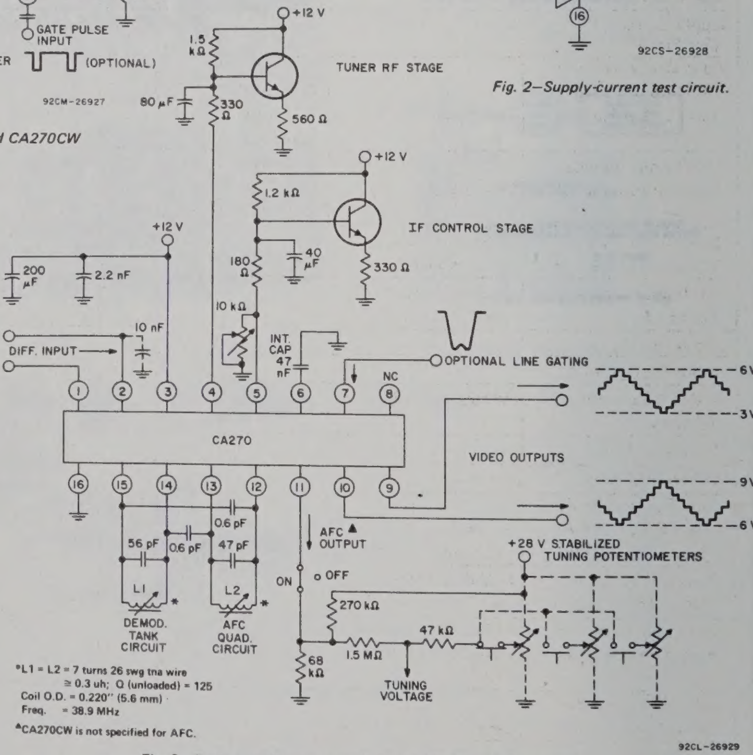
.... −40 to +55°C

STORAGE TEMPERATURE RANGE

.... −65 to +150°C

LEAD TEMPERATURE (During Soldering)

At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C



*L1 = L2 = 7 turns 26 swg tna wire ≅ 0.3 uh; Q (unloaded) = 125
Coil O.D. = 0.220" (5.6 mm)
Freq. = 38.9 MHz

▲CA270CW is not specified for AFC.

Fig. 3—Typical application circuit for CA270AW and CA270BW.

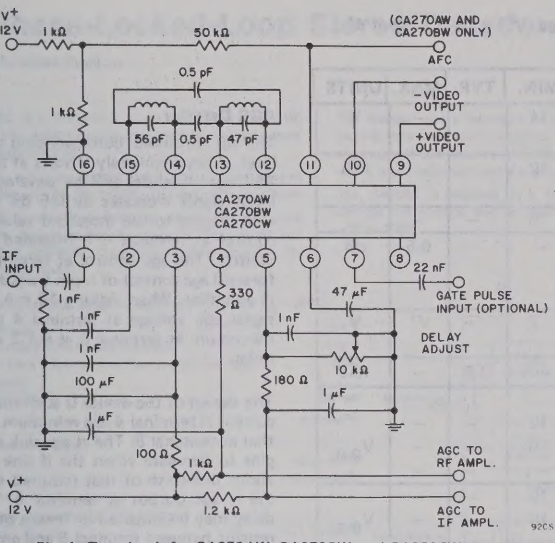


Fig. 4—Test circuit for CA270AW, CA270BW, and CA270CW.

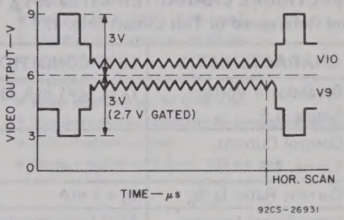


Fig. 5—Typical waveforms for video outputs.

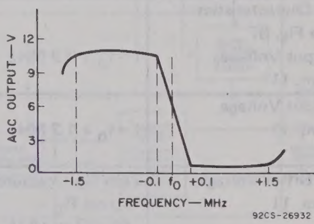


Fig. 6—Typical AFC characteristic.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Supply Voltage (V^+) = 12 V, and Referenced to Test Circuit (Fig. 4).

CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Voltage, V^+	V^+=12 V		10.2	12	13.8	V
Supply Current, I^+ (See Fig. 2)	V^+=12 V		22	40	56	mA
Video Characteristics: DC Output Voltage, Term.9 (See Fig. 5)	Zero Signal	CA270AW CA270BW CA270CW	5.7 5.8 5.5	6 6 6	6.3 6.2 6.5	V
DC Output Voltage, Term.10 (See Fig. 5)	Zero Signal	CA270AW CA270BW CA270CW	5.6 5.7 5.5	6 6 6	6.4 6.3 6.5	V
Sync Tip Output Voltage, Term.9	Output=AGC threshold (non-gated)		–	3	–	V
AC Input Voltage, Terms.1,2	Input for output= AGC threshold		50	70	100	mV
Input Res.,Term.1			–	3.3	–	KΩ
Input Res.,Term.2			–	3.3	–	KΩ
Video Bandwidth, Term.9	At output = −3 dB		–	5	–	MHz
Differential Gain	See Note 1		–	–	10	%
Differential Phase	See Note 1		–	–	10	deg
Intermod. Products: Beat Freq.,1.6 MHz Beat Freq.,2.8 MHz	See Note 1 (95% sat. blue colour bar)		– –	– –	−60 −67	dB dB
Rejection at Carrier Freq., Terms.9,10,11	F=Video Carrier;V_{IN} for Term.9(dc)=3.7V		−40	–	–	dB
Rejection,Twice Carrier Freq.,Terms.9,10,11	F=2X Video Carrier; V_{IN} for Term.9(dc) =3.7 V		−40	–	–	dB
AGC Characteristics: Sat.Voltage, Term.4	Zero Sig.; I_4 = 10 mA		–	–	0.3	V
Sat. Voltage, Term.5	Zero Sig.; I_5 = 10 mA		0.7	–	1.2	V

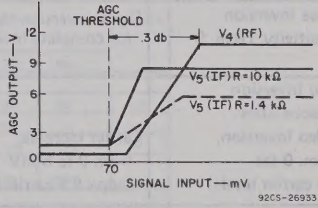


Fig. 7—Typical AGC characteristics.

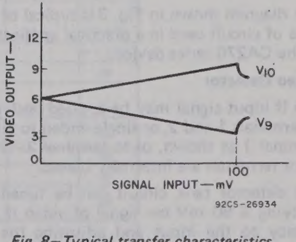


Fig. 8—Typical transfer characteristics.

CA270 Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Supply Voltage (V^+) = 12 V, (Cont'd) and Referenced to Test Circuit (Fig. 4).

CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Breakdown Voltage, Terms. 4,5	I_4 or I_5=1 mA (sink)		14	–	–	V
Control Current, Terms. 4,5			10	–	–	mA
Current Ratio I_4/I_5	I_5 = 1 mA		6	–	–	
Input Signal Increase with resp. to AGC Threshold (See Fig.7)	AGC from threshold to max.		–	–	0.5	dB
AGC Gating Pulse Input, Term. 7 (optional)	Pulse voltage=$V^+$to 0; See Note 2		2	–	V^+	V
Input Res.,Term.7			–	1.8	–	KΩ
AFC Characteristics: (See Fig. 6) Output Voltage, Term. 11	f = f_o ± 0.2 MHz	CA270AW CA270BW CA270CW	10 10 –	– – –	– – –	V_{p-p}
Output Voltage, Term. 11	f = f_o ± 1.2 MHz	CA270AW CA270BW CA270CW	10 10 –	– – –	– – –	V_{p-p}
DC Offset Voltage, Term. 11	Zero Sig.; measured across R_L = 50 KΩ to +6 V	CA270AW CA270BW CA270CW	–1.7 –1 –	– – –	1.7 1 –	V
Noise Inverter Characteristics: Inversion Threshold, Term. 9	Positive noise pulses		–	6.6	–	V
Inversion Threshold, Term. 9	Negative noise pulses		–	2.2	–	V
Noise Inversion Sensitivity,Term. 9	Signal inversion threshold for complete inversion		–	10	–	mV
Video Inversion Characteristics: Video Inversion, Term. 9 (at low carrier levels)	Carrier increase from 0 to 5 mV (appx.8% carrier)	CA270AW CA270BW CA270CW	– – –	– – –	0.2 0.1 0.3	V

Note 1: CCIR modulation system, peak white = 10% carrier.

Note 2: Maximum pulse amplitude must never exceed the suppiy voltage (V^+).

APPLICATIONS

The diagram shown in Fig. 3 is typical of the type of circuit used in a practical application of the CA270 series devices.

Video Detector

The if input signal may be applied push-pull to terminals 1 and 2, or single-ended to either terminal 1 as shown, or to terminal 2. These input terminals are internally biased.

The detector tank circuit can be tuned by applying a 50 mV cw signal of video if frequency to the input and adjusting the inductor L1 for maximum differential output between terminals 9 and 10. The input signal is then reduced to 25 mV and L1 is readjusted for maximum output.

AFC Detector

The afc quadrature tank circuit should be tuned only after the detector adjustment has been made. Using the same input signal, inductor L2 should be adjusted for 6 V dc output at terminal 11. The 0.5-pF quadrature phase-shift coupling capacitors can affect symmetry and actual values will depend on the layout used. When L1 and L2 are properly tuned, the output swing at terminal 11 will be 10 volts minimum for frequencies of ±0.2 MHz to ±1.2 MHz about the if carrier frequency.

AGC Detector

The agc threshold, corresponding to sync tip level, is approximately 3 volts at terminal 9. Full agc potential will be developed if the input signal increases by 0.5 dB maximum with respect to the threshold value. The agc control at terminal 4 is intended for tuner control. The agc control at terminal 5 is for forward agc control of n-p-n transistors in the if amplifier. When sinking 10 mA, the zero-signal agc voltage at terminal 4 is 0.3 volt maximum; at terminal 5, it is 1.2 volts maximum.

The design of the device is such that the sink current at terminal 4 is a minimum of 6 times that at terminal 5. The rf agc sink current begins to decrease when the if sink current is about one-sixth of that required to saturate the rf agc output at terminal 4. The rf agc delay may be adjusted by means of a variable resistor between terminal 5 and ground. This adjustment modifies the if system gain, thus affecting the rf delay threshold. At maximum gain the current into terminal 5 is large compared to the current in the variable resistor and adjustment is ineffective. As the signal increases and rf agc is applied, the terminal 5 sink current approaches zero and the if agc is determined by the value of the variable resistor.

A horizontal gating pulse may be applied to terminal 7 to gate the agc detector. The agc threshold (sync tip) decreases approximately 0.3 volt at terminal 9 when gating is used. The gating pulses must be negative-going with a recommended minimum amplitude of 3 volts. They may be ac or dc coupled, but the maximum peak value must not exceed the dc supply voltage at terminal 3. If dc coupling is used, the potential during flyback should be less than 0.5 volt and during scan, greater than 1.5 volts.

Noise Inverter

Noise pulses in excess of 6.6 volts at terminal 9, which would result in "white spots", are processed in the device by inverting and clamping them to near black level (approx. 3.6 V). Noise pulses at levels of less than 2.2 volts at terminal 9 which would result in sync noise interference, are inverted and returned to black level.

Complete inversion occurs for signals 10 mV above the inversion threshold.

RC Phase-Locked-Loop Stereo Decoder

For FM Multiplex Systems

Features:

- Low distortion (THD): 0.4% (typ.)
- Excellent SCA rejection: 70 dB typ.
- RC oscillator
- High-audio-channel separation: 45 dB
- Power supply range: 10 to 16 V dc
- Requires only one adjustment for complete alignment
- Low-impedance outputs
- Stereo indicator lamp drive: 150 mA typ.

RCA-CA758E is a monolithic silicon integrated circuit RC phase-lock loop stereo decoder intended for FM solid-state stereo multiplex systems.

The CA758E is pin compatible and electrically equivalent to industry types μA758, MC1311P, LM1800, and ULX2244.

The CA758E decodes the multiplexed stereo input signal into left and right channel audio output signals. The decoder also suppresses SCA (storecast) transmissions when present in the composite stereo signal.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC Supply Voltage	+18 V
DC Supply Voltage (for ⩽a 15-second period)	+22 V
DC Voltage at Term. 7 (Lamp Driver Circuit with Lamp "OFF")	+22 V
Device Dissipation:	
Up to $T_A = 70^oC$	730 mW
Above $T_A = 70^oC$ derate linearly	9.1 mW/°C
Ambient Temperature Range:	
Operating	−40 to +85°C
Storage	−65 to +150°C
Lead Temperature (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C

The decoder uses a minimum of external components, and requires one adjustment (oscillator frequency) for complete alignment. In addition, the CA758E provides automatic mono-stereo mode switching and energizes a stereo indicator lamp.

The CA758E is supplied in a 16-lead dual-in-line plastic package and operates over an ambient temperature range of −40 to +85°C.

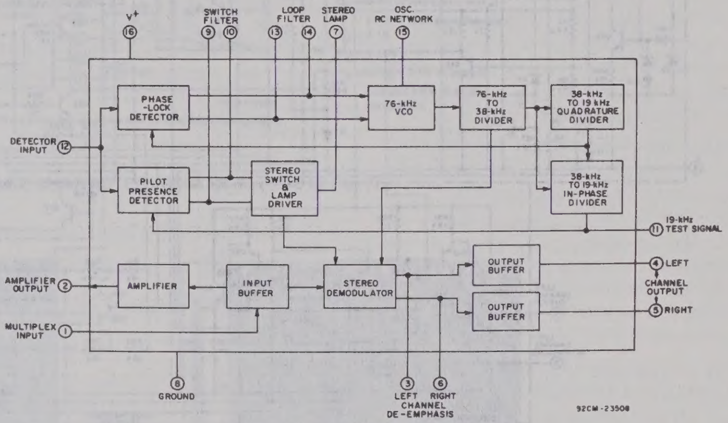


Fig. 1 – Functional block diagram of the CA758E.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig 7 unless otherwise specified)	LIMITS			UNITS
	$V^+ = 12$ V, $T_A = 25^oC$ Multiplex Input Signal (L=R, pilot "OFF") = 300 mV RMS 19-kHz Pilot Level = 30 mV RMS f (modulation) = 400 Hz or 1 kHz	Min.	Typ.	Max.	
Static Characteristics					
Total Current	Lamp "OFF"	–	26	35	mA
Maximum Available Lamp Current		75	150	–	mA
DC Voltage at Term. 7 (Lamp Driver)	I (Lamp) = 50 mA	–	1.3	1.8	V
DC Voltage Shift at either Term. 4 or 5 (Output)	Stereo-to-Mono Operation	–	30	150	mV
Dynamic Characteristics					
Power Supply Ripple Rejection	For a 200-Hz, 200-mV RMS Signal	35	45	–	dB
Input Resistance		20	35	–	kΩ
Output Resistance		0.9	1.3	2.0	kΩ
Channel Separation (Stereo)	At f = 100 Hz	–	40	–	dB
	f = 400 Hz	30	45	–	dB
	f = 10 kHz	–	45	–	dB
Channel Balance (Monaural)		–	0.3	1.5	dB
Voltage Gain	At f = 1 kHz	0.5	0.9	1.4	V/V
Pilot Input Level: 19-kHz Input	Lamp "ON"	–	15	20	mV RMS
19-kHz Input	Lamp "OFF"	2.0	7.0	–	mV RMS
Hysteresis	Lamp "OFF"	3.0	7.0	–	dB
Capture Range (Deviation from 76-kHz Center Frequency)		± 2.0	± 4.0	± 6.0	%
Total Harmonic Distortion	Multiplex Input Signal = 600 mV RMS (Pilot "OFF")	–	0.4	1.0	%
19-kHz Rejection		25	35	–	dB
38-kHz Rejection		25	45	–	dB
SCA (Storecast) Rejection	Measured Composite Signal: 80% Stereo, 10% Pilot, 10% SCA	–	70	–	dB
Voltage-Controlled Oscillator (VCO) Tuning Resistance	Total Resistance (Term. 15 to 8) required to set $f_{REF} = 19$ kHz ± 10 Hz (Term. 11)	21.0	23.3	25.5	kΩ
Voltage-Controlled Oscillator Frequency Drift	$0^o \leqslant T_A \leqslant 25^oC$	–	+0.1	± 2	%
	$25^o \leqslant T_A \leqslant 70^oC$	–	−0.4	± 2	%

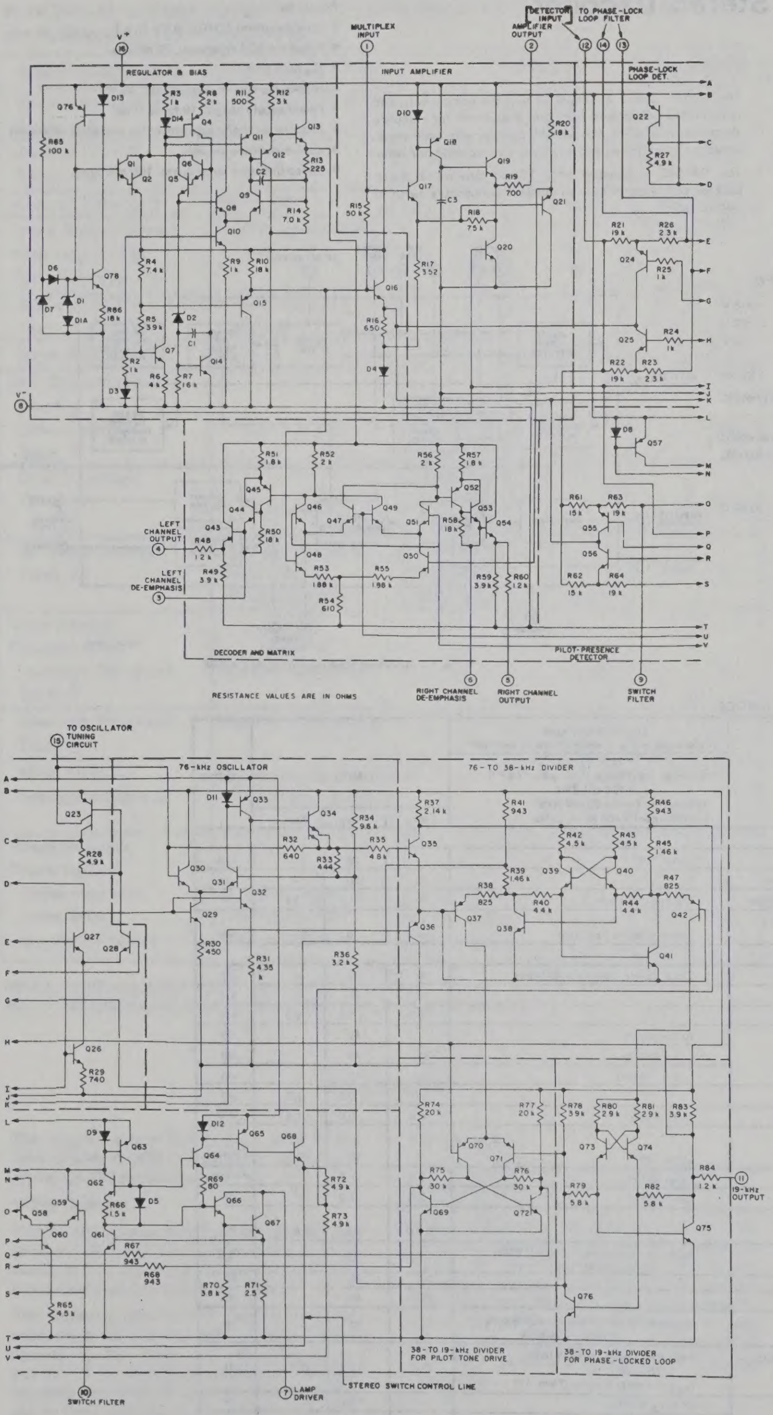


Fig. 2 – Schematic diagram of the CA758E.

92CL-23177

TYPICAL PERFORMANCE CHARACTERISTICS

(Referenced to Fig. 7)

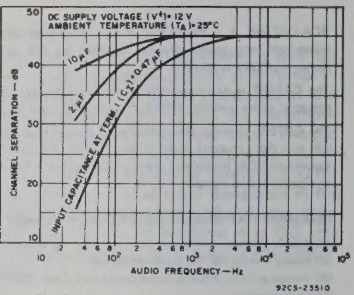


Fig. 3 — Channel separation vs. audio frequency.

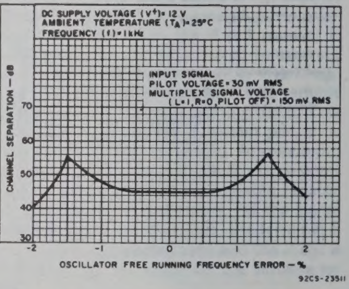


Fig. 4 — Channel separation vs. oscillator free running frequency error.

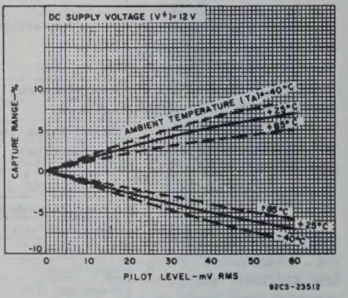


Fig. 5 — Capture range vs. pilot level.

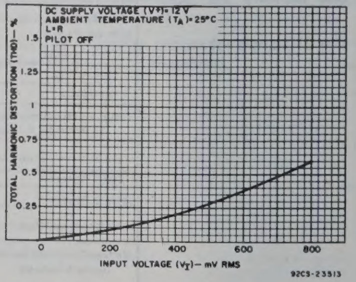


Fig. 6 — Total harmonic distortion vs. input level.

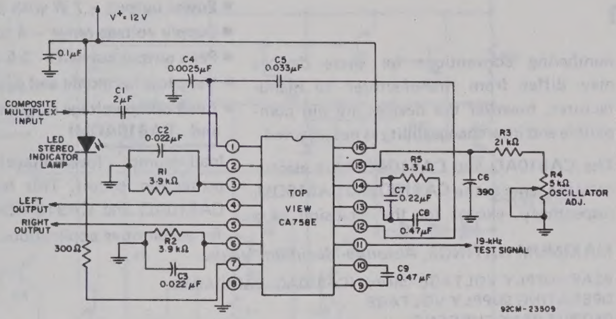


Fig. 7 — Test circuit for measurement of dynamic characteristics.

NOTES:

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified.

C_1 = +100%, −20%

C_6 = ±1% in test circuit and ±5% in typical application.

R_3 = ±1%

R_4 = ±10%

R_1 and R_2 = ±1% in test circuit and ±5% in typical application.

TYPICAL PERFORMANCE CHARACTERISTICS (Referenced to Fig. 7)

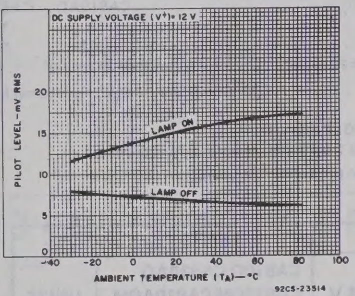


Fig. 8 — Lamp turn-on and turn-off sensitivity vs. ambient temperature.

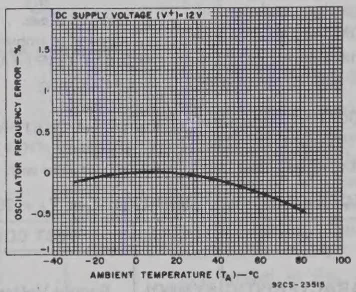


Fig. 9 — Oscillator free running frequency error vs. ambient temperature.

CA810, CA810A Types

Preliminary Data

7-Watt Audio Power Amplifier With Thermal Shut-Down

Features:

- **Power output – 7 W with 4Ω load**
- **Supply voltage range – 4 to 20 V**
- **Peak output current – 2.5 A (max.)**
- **Very low harmonic and cross-over distortion**
- **Load dump voltage surge protection (CA810AQ and CA810AQM)**

The RCA-CA810Q, CA810AQ, CA810QM and CA810AQM are monolithic audio amplifiers intended for class B operation. They are specifically designed for mobile equipment operating from 12-V battery supplies. They operate over a wide range of supply voltages (4 to 20 V) with very low harmonic and crossover distortion. The maximum repetitive peak output current is 2.5 A, and an integral thermal limiting circuit shuts the device down in case of output overload or excessive package temperature.

The CA810Q, CA810AQ, CA810QM, and CA810AQM are supplied in modified 16-lead quad-in-line plastic packages ("Q" suffix) with integral wing-tab heat sinks. The tabs on the CA810Q and CA810AQ are bent down for p.c. board insertion, and on the CA810QM and CA810AQM they are flat and pierced for easy attachment to an external heat sink.

The CA810Q and CA810QM are electrically equivalent to types TBA810S and TBA810AS, respectively. It should be noted that pin-numbering conventions for these devices may differ from manufacturer to manufacturer, however the devices are pin compatible and interchangeability is not affected.

The CA810AQ and CA810AQM are electrically the same as the CA810Q and CA810QM, respectively, except for the inclusion of a load dump (overvoltage) voltage surge protection circuit. This feature makes the CA810AQ and CA810AQM ideally suitable for automotive applications.

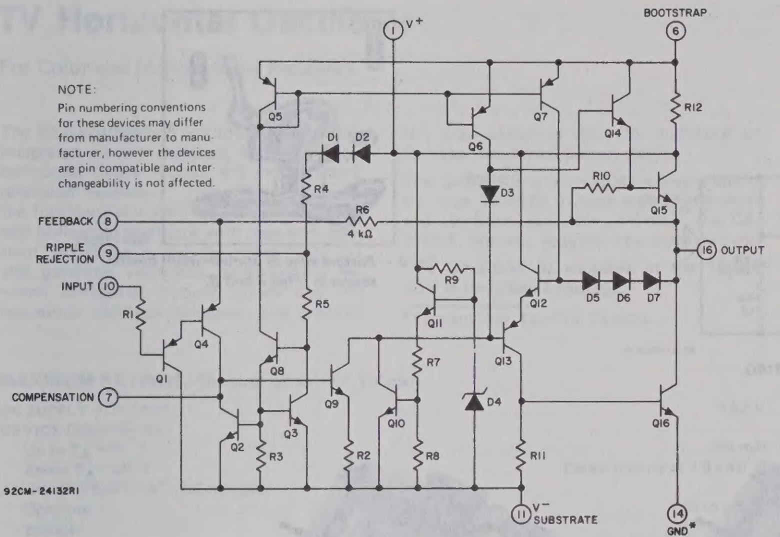
MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA810Q CA810AQ	CA810QM CA810AQM	
PEAK SUPPLY VOLTAGE (50 ms) (CA810AQ, CA810AQM)			40 V
OPERATING SUPPLY VOLTAGE			20 V
OUTPUT PEAK CURRENT:			
REPETITIVE			2.5 A
NON-REPETITIVE			3.5 A
POWER DISSIPATION, P_D			
At $T_A = 70^\circ C$			1 W
At $T_{tab} = 100^\circ C$			5 W
THERMAL RESISTANCE, JUNCTION			
Junction to tab	12	10	°C/W
Junction to ambient	70*	80	°C/W
AMBIENT-TEMPERATURE RANGE:			
OPERATING			−40°C to (Refer to Fig.7 for typical high-temperature limit)
STORAGE			−40 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max.			260°C

*Value obtained with tabs soldered to printed-circuit board.

ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Supply Voltage (V^+) = 14.4 V Unless Otherwise Specified	LIMITS CA810Q,CA810AQ CA810QM,CA810AQM MIN.	 TYP.	 MAX.	UNITS
Supply Voltage	V^+		4	–	20	V
Input Voltage	V_I		–	–	220	mV
Input Sensitivity	e_I	$P_O = 6W$, $R_L = 4\Omega$, $R1 = 56\Omega$, f = 1 kHz	–	80	–	mV
Quiescent Output Voltage	V_O		6.4	7.2	8	V
Quiescent Current Drain	I_O		–	12	20	mA
Input Noise Voltage	e_N	$R_g = 0$, BW (−3 dB) = 20 to 20,000 Hz	–	2	–	μV
Bias Current	I_{IB}		–	0.4	–	μA
Output Power	P_O	f = 1 kHz, $R_L = 4\Omega$, THD = 10%, $V^+ = 14.4$ V	–	6	–	W
		$V^+ = 6$ V	–	1	–	
Input Resistance	R_I		–	5	–	MΩ
Total Harmonic Distortion	THD	P_O = 50 mW to 3W, R_L 4Ω, f = 1 kHz	–	0.3	–	%
Open-Loop Voltage Gain	A_{OL}	$R_L = 4\Omega$, f = 1 kHz	–	80	–	dB
Closed-Loop Voltage Gain	A	$R_L = 4\Omega$, f = 1 kHz, $R1 = 56\Omega$	34	37	40	dB
Efficiency	η	$P_O = 5W$, $R_L = 4\Omega$; f = 1 kHz	–	70	–	%


NOTE:
Pin numbering conventions for these devices may differ from manufacturer to manufacturer, however the devices are pin compatible and interchangeability is not affected.

*WING TABS ARE TO BE GROUNDED.

Fig. 1 — Schematic diagram of CA810Q, CA810QM.

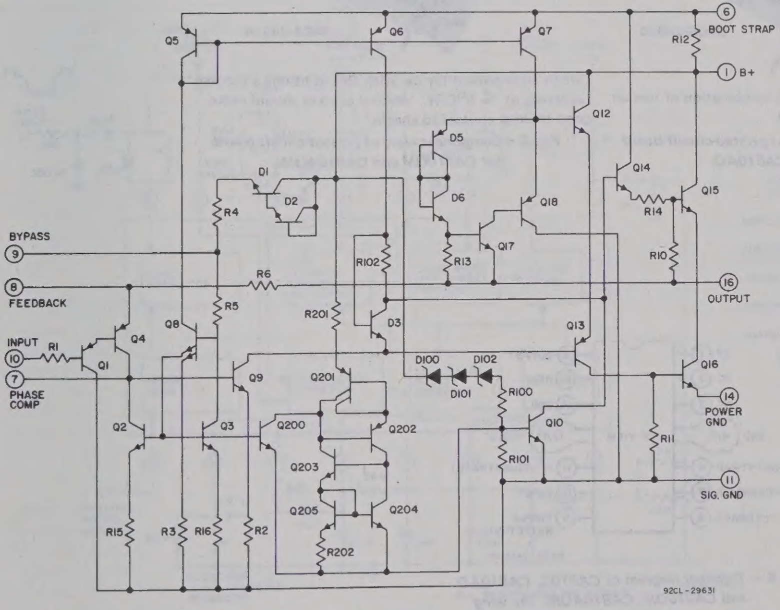


Fig. 3 — Schematic diagram of CA810AQ, CA810AQM.

Thermal Shut-Down

The thermal-limiting network incorporated in the CA810 Series circuits provides protection against damage due to excessive semiconductor temperatures that may result from high ambient temperatures and/or excessive dissipation, e.g., as encountered in sustained overloads. As indicated in Fig.2 the thermal-limiting feature automatically reduces the supply current (and output power) at the higher temperatures.

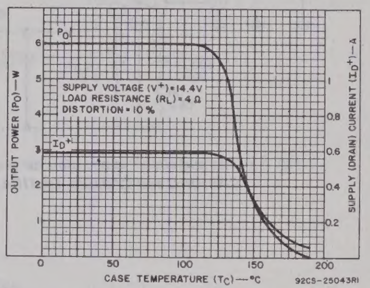


Fig. 2 — Typical output power and drain current as a function of case temperature for all types.

Load-Dump Voltage-Surge Protection

The maximum operating supply voltage of the CA810AQ and CA810AQM is 20 V, and internal protection is provided for peaks of up to 40 V, as shown in Fig. 4. Supply-voltage peaks of more than 40 V will require an LC network between the supply and terminal 5. An LC network, such as the one shown in Fig. 8, provides protection against supply-voltage surges of up to 120 V for 2 ms. This type of protection is ON when the supply voltage (pulsed or dc) exceeds 20 V.

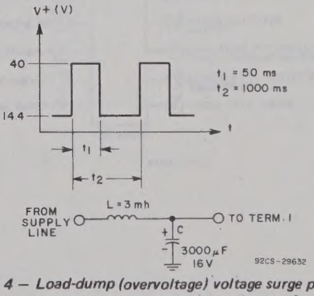


Fig. 4 — Load-dump (overvoltage) voltage surge protection network and timing diagram for CA810AQ and CA810AQM.

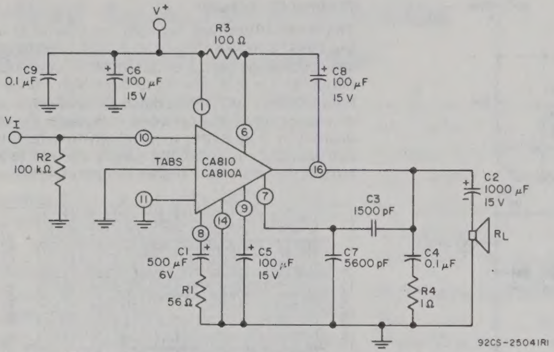


Fig. 5 – Test and circuit application for the CA810Q, CA810AQ and CA810M, CA810AQM.

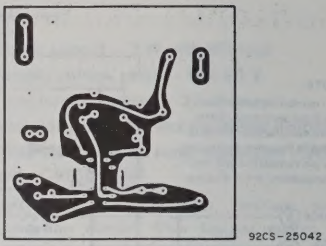
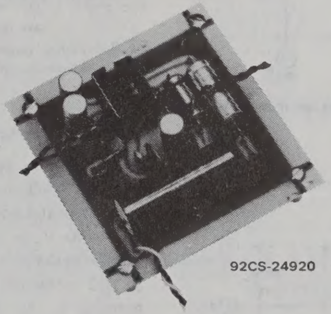
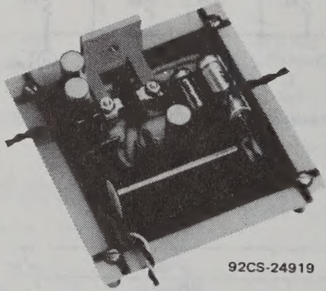


Fig. 6 – Bottom view of printed-circuit boards shown in Figs.7 and 8.



Circuit heat is dissipated by a combination of free air and printed-circuit board foil.

Fig. 7 – Component view of printed-circuit board for CA810Q and CA810AQ.



Circuit arrangement for use with chassis having a thermal resistance of ⩽ 5°C/W. Vertical bracket should make good thermal contact to chassis.

Fig. 8 – Component view of printed-circuit board for CA810QM and CA810AQM.

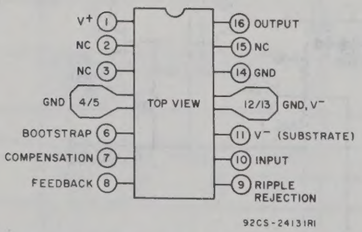


Fig. 9 – Terminal diagram of CA810Q, CA810AQ and CA810QM, CA810AQM. The wing tabs on the CA810Q and CA810AQ are bent down, and on the CA810QM and CA810AQM they are flat and pierced.

TV Horizontal Oscillator

For Color and Monochrome Receivers

The RCA-CA920AE* is a silicon monolithic integrated circuit intended for use in the horizontal stages of color and monochrome television receivers. This device performs the functions of a sync separator, noise gate, and horizontal oscillator with dual-time-constant switching in the fly-wheel loop. It also generates automatic phase control between horizontal flyback pulses and the horizontal oscillator frequency and provides fast edge switching drive for transistor or thyristor horizontal output stages.

The CA920AE is compatible with the industry type TBA920 in both lead arrangement and electrical operation, although the CA920AE features reduced operating current.

The CA920AE is supplied in the 16-lead dual-in-line plastic package.

---

*Formerly Dev. Type No. TA6773.

Features:

- Sync separator
- Noise gate input
- Internal precision timing ramp
- Dual-time-constant phase-locked loop
- Output suitable for transistor or thyristor deflection systems
- Reduced power dissipation

MAXIMUM RATINGS, *Absolute Maximum Values:*

DC SUPPLY VOLTAGE	13.2 V
DEVICE DISSIPATION:	
Up to $T_A = 55^\circ C$	750 mW
Above $T_A = 55^\circ C$	Derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265°C

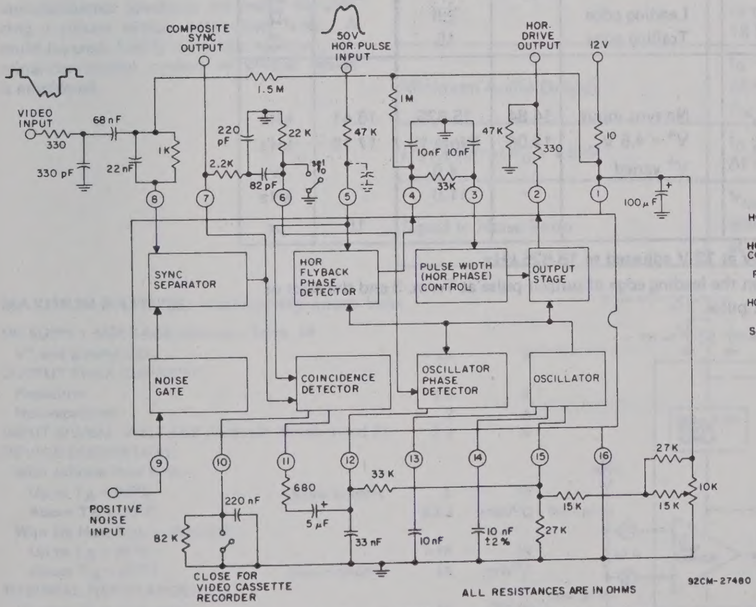
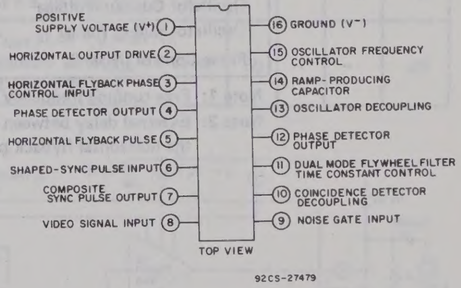


Fig. 1 – Functional block diagram of the CA920AE with typical peripheral circuitry.

TERMINAL ASSIGNMENT


POSITIVE SUPPLY VOLTAGE (V+) 1
HORIZONTAL OUTPUT DRIVE 2
HORIZONTAL FLYBACK PHASE CONTROL INPUT 3
PHASE DETECTOR OUTPUT 4
HORIZONTAL FLYBACK PULSE 5
SHAPED-SYNC PULSE INPUT 6
COMPOSITE SYNC PULSE OUTPUT 7
VIDEO SIGNAL INPUT 8
16 GROUND (V−)
15 OSCILLATOR FREQUENCY CONTROL
14 RAMP-PRODUCING CAPACITOR
13 OSCILLATOR DECOUPLING
12 PHASE DETECTOR OUTPUT
11 DUAL MODE FLYWHEEL FILTER TIME CONSTANT CONTROL
10 COINCIDENCE DETECTOR DECOUPLING
9 NOISE GATE INPUT
TOP VIEW
92CS-27479

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, and Supply Voltage (V^+) = 12 V, Unless otherwise specified. See Fig. 1.

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	Typ.	Max.	UNITS
Supply Current, Term. 1, I^+	Term. 2 open		22		mA
Video Characteristics (Term.8):					
Input Voltage V_8	Peak to peak	1.5	3	6	V
Input Current I_8	Peak			10	mA
Noise Gate Characteristics (Term.9):					
Input Current I_9		0.03		10	mA
Reverse Input Current I_9				−10	mA
Horizontal Flyback Positive Pulse Characteristics (Term.5):					
Input Voltage V_5		1		3	V
Input Current I_5		0.05	1	10	mA
Input Impedance Z_5			0.4		kΩ
Positive Sync Characteristics (Term.7):					
Output Voltage V_7	Peak to peak		10		V
Output Impedance Z_7	Leading edge		50		Ω
Output Impedance Z_7	Trailing edge		100		Ω
Horizontal Output Characteristics (Term.2):					
Output Current I_{2MAX}	Peak			200	mA
Output Current I_{2AV}	Average			20	mA
Output Pulse Width t_W		12		32	µs
Output Impedance Z_2	Leading edge		2.5		Ω
Output Impedance Z_2	Trailing edge		15		Ω
Horizontal Oscillator Characteristics (Term.15):					
Free-Running Frequency f_o	No sync input	14.84	15.625	16.41	kHz
Free-Running Frequency f_o	V^+ = 4.5 V	14.06	(Note 1)	17.19	kHz
Oscillator Cut-out Voltage	V^+ varied		4.0		V
Oscillator Pull-in Range			±1.0		kHz
Phase Control (Note 2)				15	µs

Note 1: Free-running frequency at 12 V adjusted to 15.625 kHz.

Note 2: External delay between the leading edge of output pulse at Term. 3 and the start of the horizontal flyback pulse.

CA1190GQ

TV Sound IF and Audio Output Subsystems

"GQ" Suffix Type – Hermetic Gold-CHIP in Quad-In-Line Plastic Package

The RCA-CA1190GQ combines the sound IF and audio output subsystems on a single monolithic integrated circuit to provide a television sound system. Each device includes a multistage IF amplifier-limiter, an FM detector, and an audio power amplifier that is designed to drive, primarily, an 8-, 16-, or 32-ohm speaker.

The CA1190GQ is electrically and mechanically equivalent to industry type TDA1190Z. The CA1190GQ differs from the TDA1190Z primarily in its provisions for external feedback components and a higher value volume control.

The CA1190GQ is supplied in the hermetic Gold-CHIP (G suffix) 16-lead quad-in-line plastic package with an integral bent-down wing-tab heat sink (Q suffix), intended for printed circuit board mounting.

The transistor chips used in the hermetic Gold-CHIP plastic package are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

Features:

- **Nominal power output: 4 W at V^+=24 V, R_L=16Ω, dist. = 10%; 2 W at V^+=12 V, R_L=8Ω, dist.=10%**
- **Wide power-supply range: 9 to 28 V**
- **Low quiescent current: 25 mA typ.**
- **5-kHz deviation sensitivity: 1 W output typ.**
- **3-dB limiting sensitivity: 50 µV typ.**
- **Excellent AM rejection: 50 dB typ.**
- **Differential peak detector – requires one tuned coil**
- **Electronic volume control with improved taper and single wire control**

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 24 V, DC Volume Control Rx = 0 Ω, R_L = 16 Ω unless otherwise indicated. Refer to Fig. 1.

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Static Characteristics					
Current into Term. 14	P_o = 0	10	25	40	mA
Dynamic Characteristics					
IF Amplifier: Input Limiting Voltage, (At –3 dB point), V_1 (lim)	f_o = 4.5 MHz, f_m = 400 Hz Δf = ± 25 kHz	–	50	100	µV
AM Rejection, AMR	f_o = 4.5 MHz, f_m = 400 Hz, Modulation Index = 0.3, V_{IN} = 1 mV	40	50	–	dB
Deviation Sensitivity	f_o = 4.5 MHz, f_m = 400 Hz Δf = ± 25 kHz, V_I = 1 mV Rx = 0, Deviation necessary to obtain 4 Vrms across 16 Ω (1 W)	–	5	–	kHz
Minimum Audio Output	f_o = 4.5 MHz, f_m = 400 Hz Δf = ± 25 kHz, V_I = 1 mV R_x = 15 kΩ	–	–	10	mVrms
Distortion at P_o = 1.5 W	f_o = 4.5 MHz, f_m = 400 Hz Δf = ± 25 kHz, V_{IN} = 1 mV	–	–	3	%
Signal to Noise Ratio	V_{out} at Δf = 0 with Rx adjusted for V_{out} = 4 Vrms at Δf = ± 25 kHz	50	–	–	dB

MAXIMUM RATINGS, *Absolute-Maximum Valu*

DC SUPPLY VOLTAGE (Between Term. 14 V^+ and ground tabs)	+ 28	V
OUTPUT PEAK CURRENT:		
Repetitive	1.5	A
Non-repetitive	2	A
INPUT SIGNAL VOLTAGE (Between Terms. 1 and 2)	±3	V
DEVICE DISSIPATION:		
With Infinite Heat Sink –		
Up to T_A = 90°C derate linearly	5	W
Above T_A = 90°C	83.3	mW/°C
With No Heat Sink – (free air) –		
Up to T_A = 25°C	1.75	W
Above T_A = 25°C derate linearly	14	mW/°C
THERMAL RESISTANCE:		
Junction to ground tabs	12	°C/W
AMBIENT TEMPERATURE RANGE:		
Operating	–40 to +85	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At a distance 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

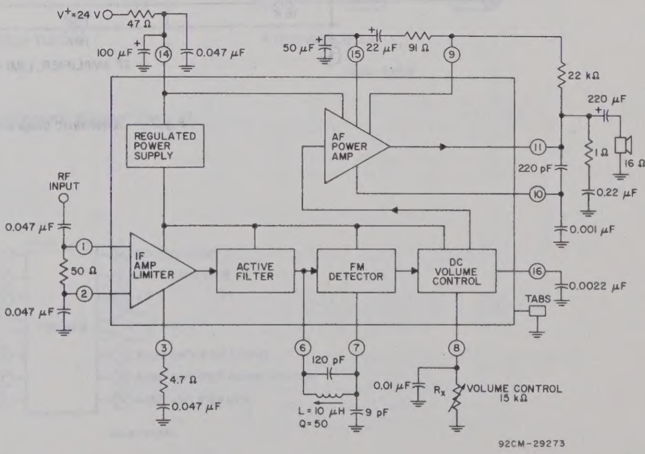


Fig.1 – Block diagram of the CA1190GQ in a typical application.

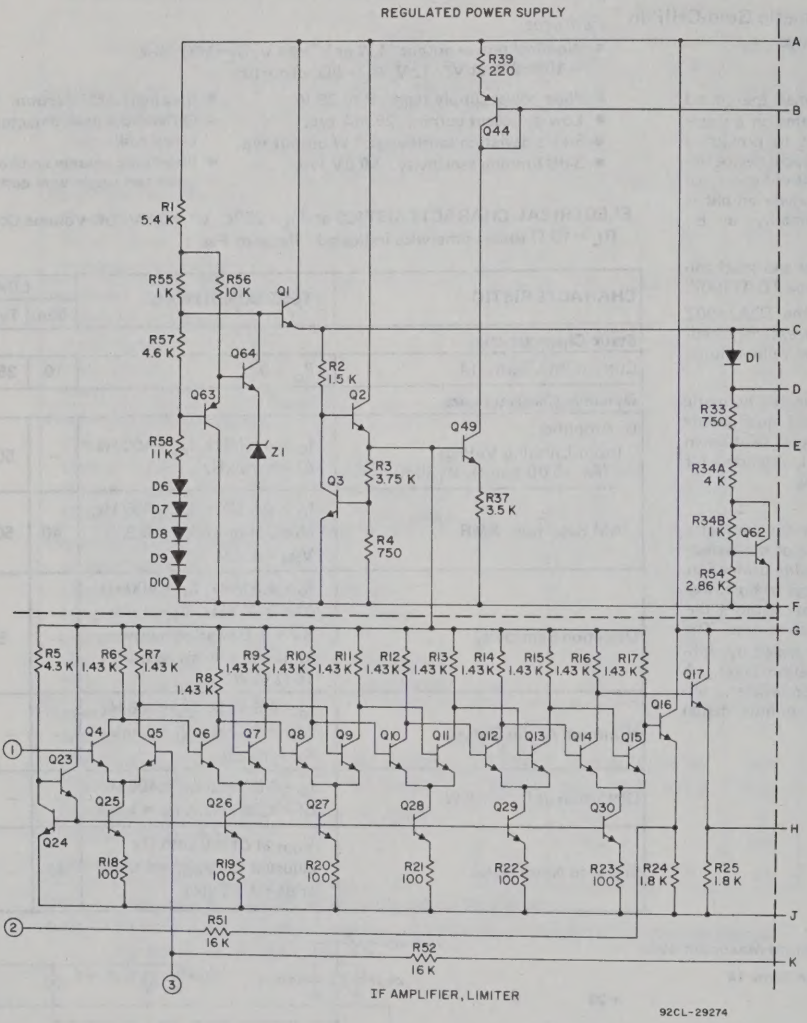


Fig.2 — Schematic diagram.

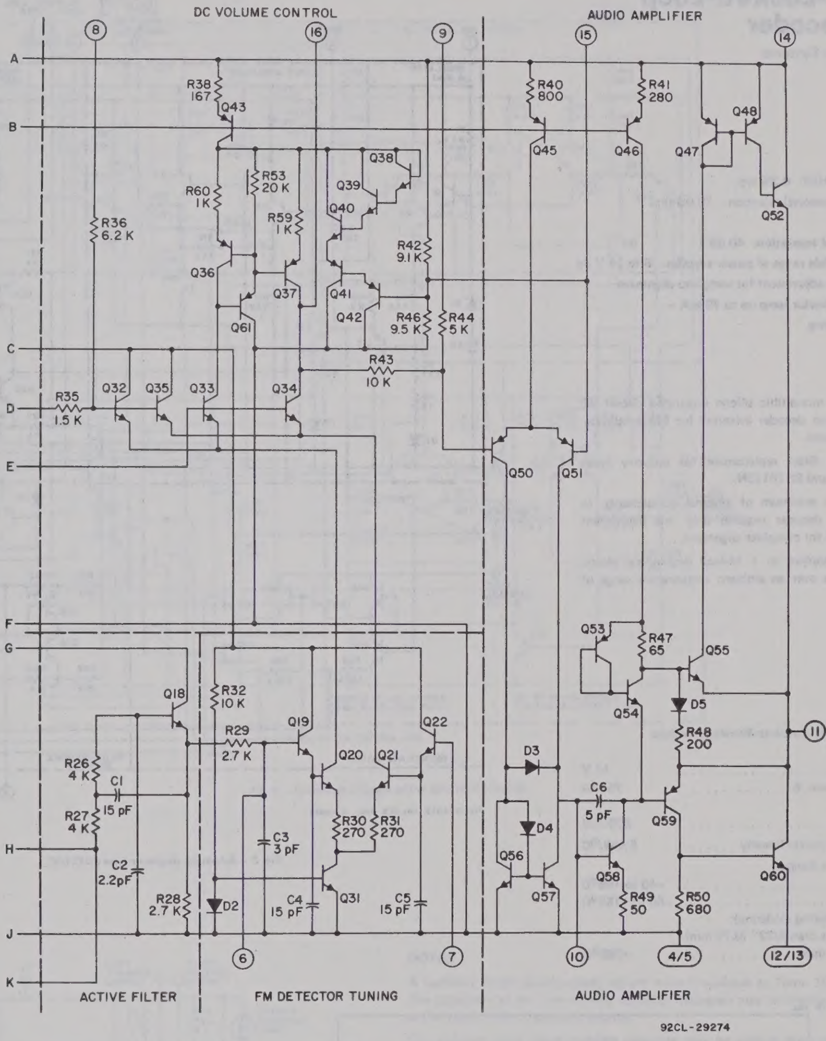


Fig.2 — Schematic diagram (cont'd).

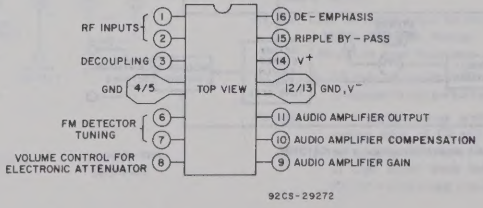


Fig.3 — Terminal diagram.

CA1310E

RC Phase-Locked-Loop Stereo Decoder

For FM Multiplex Systems

Features:

- Low distortion (THD): 0.3% typ.
- Excellent SCA (storecast) rejection: 75 dB typ.
- RC oscillator
- High audio channel separation: 40 dB
- Operates from a wide range of power supplies: 8 to 14 V dc
- Requires only one adjustment for complete alignment
- Drives a stereo indicator lamp up to 75 mA – surge current limiting

RCA-CA1310E is a monolithic silicon integrated circuit RC phase-lock-loop stereo decoder intended for FM solid-state stereo multiplex systems.

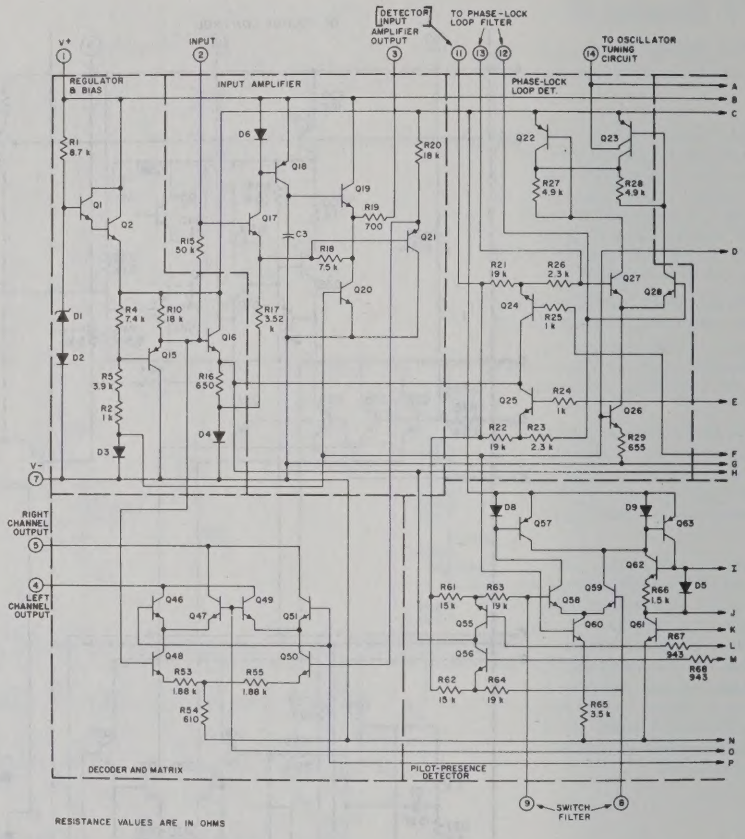
The CA1310E is a direct replacement for industry types MC1310P, LM1310, and SN76115N.

This decoder uses a minimum of external components. In addition the stereo decoder requires only one adjustment (oscillator frequency) for complete alignment.

The CA1310E is supplied in a 14-lead dual-in-line plastic package and operates over an ambient temperature range of –40 to +85°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC Supply Voltage	14 V
Current (Lamp) at Term. 6	75 mA
Device Dissipation:	
Up to $T_A = 25^oC$	625 mW
Above $T_A = 25^oC$ derate linearly	5 mW/°C
Ambient Temperature Range:	
Operating	–40 to +85°C
Storage	–65 to +150°C
Lead Temperature (During soldering):	
At distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C



RESISTANCE VALUES ARE IN OHMS

Fig. 2 – Schematic diagram of the CA1310E.

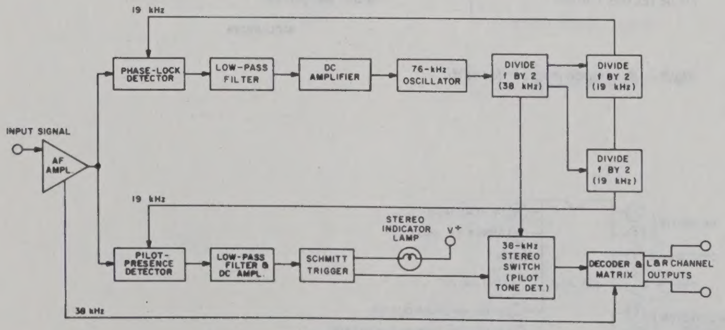


Fig. 1 – Functional block diagram system using the CA1310E.

92CS-23500

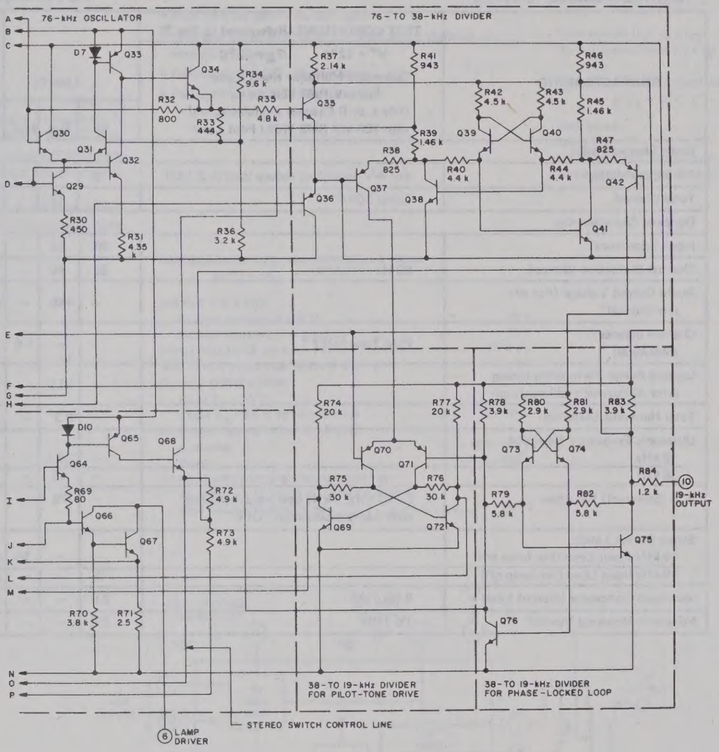
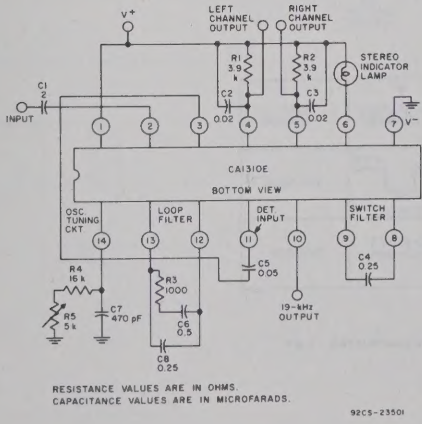


Fig. 2 – Schematic diagram of the CA1310E (Cont'd).



NOTES

A buffered 3-volt positive-going square wave is available at Term. 10. The alignment of the free-running oscillator frequency may be checked at this point with a frequency counter.

C1: A lower value input coupling capacitor may be used in place of the 2-μF value if reduced separation at low frequencies is acceptable.

C4: The time constant for the stereo switch level detector circuit is calculated by C4 x 53,000 ohms ±30% with a maximum dc voltage drop across C4 of 0.25 volt (Term. 8 positive) and a pilot level voltage of 100 mV RMS. Signal voltage across C4 is negligible.

C5: The recommended 0.05-μF capacitor provides a 1.75° phase lead at 19 kHz.

R1, R2: Load resistance values are related to supply voltage as follows:

Minimum Supply Voltage	8	10	12	V
Maximum Load Resistance	2.7	4.3	6.2	kΩ

R3, C6, C8: C8 may be omitted, R3 = 100 ohms and C6 = 0.25 μF, if relaxed circuit performance is acceptable.

R4, R5, C7: If a capture range greater than ±3% typ. is required, reduce value of C7 and increase values of R4, R5 proportionally. However, beat-note distortion is increased at high signal levels because of oscillator-phase jitter. R4, C7 = ±1% in test circuit and ±5% in typical application.

Fig. 3 – Test circuit for measurement of dynamic characteristics.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig. 3)	LIMITS			UNITS
	$V^+ = 12$ V $T_A = 25^{\circ}$C Composite Multiplex Input Signal = 560 mV RMS (2.8 V p-p) Only L or R Channel modulated; and with 100-mV RMS (10%) Pilot Level	Min.	Typ.	Max.	
Static Characteristics					
DC Supply Voltage	For 8-V operation, reduce load to 2.7 kΩ	8	–	14	V
Total Current	Lamp "OFF"	–	13	–	mA
Dynamic Characteristics					
Input Impedance		20	50	–	kΩ
Channel Separation (Stereo)	50 Hz – 15 kHz	30	40	–	dB
Audio Output Voltage (For any one channel)		–	485	–	mV RMS
Channel Balance (Monaural)	Pilot Tone "OFF"	–	–	1.5	dB
Capture Range (Permissible tuning error of internal oscillator)		–	±3.5	–	%
Total Harmonic Distortion		–	0.3	–	%
Ultrasonic Frequency Rejection:					
19 kHz		–	34.4	–	dB
38 kHz		–	45	–	dB
SCA (Storecast) Rejection	f = 67 kHz, 9-kHz beat note measured with 1-kHz modulation "OFF"	–	75	–	dB
Stereo Switch Level:					
19-kHz Input Level (For lamp on)		–	–	20	mV RMS
19-kHz Input Level (For lamp off)		5	–	–	mV RMS
Maximum Composite (Stereo) Input	0.5% THD	2.8	–	–	V p-p
Maximum Monaural Input	1% THD	2.8	–	–	V p-p

CA1352E

TV Video IF Amplifier

With AGC and Keyer Circuit

The RCA-CA1352E is a monolithic integrated circuit designed for use as an if amplifier in monochrome or color TV receivers. It features a high-gain gated AGC system with a 68-dB range (typ.). A delayed forward AGC output is adjustable by means of a potentiometer. Either positive- or negative-going sync may be used for this system.

The CA1352E is supplied in the 14-lead dual-in-line plastic package, and is directly interchangeable with the industry type 1352 in similar packages.

Features

- **High 45-MHz gain — 53 dB (typ.)**
- **High-gain gated AGC system — with either positive- or negative-going sync.**
- **Adjustable rf AGC delay to tuner**
- **AGC gain reduction — 68 dB (typ.)**

MAXIMUM RATINGS, ***Absolute-Maximum Values***
At T_A = 25

SUPPLY VOLTAGE:

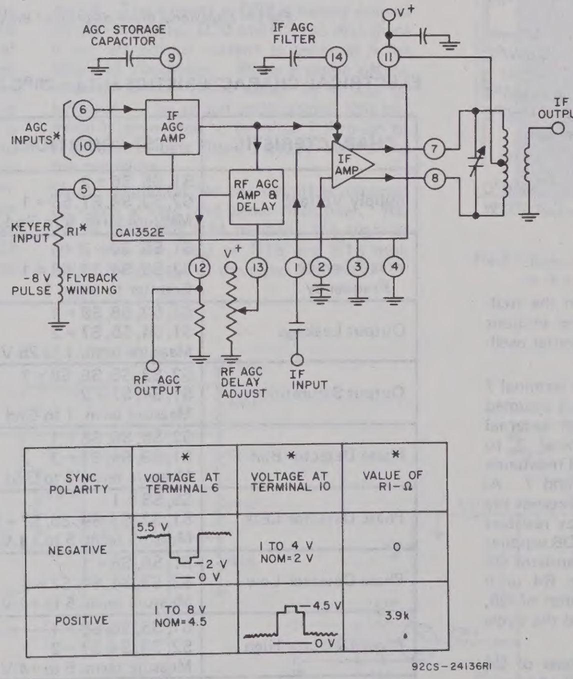
Between terminals 4 and 11	18 V
Between terminals 7 or 8 and 4	18 V
INPUT VOLTAGE (terminal 1 or 2)	10 V p-p
AGC INPUT VOLTAGE (terminal 6 or 10)	6 V
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C derate linearly at	7.9 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

TYPICAL STATIC CHARACTERISTICS
at T_A = 25°C, V^+ = 12 V

Total Current ($I_7 + I_8 + I_{11}$)	27 mA
Output Stage Current ($I_7 + I_8$)	5.7 mA

TYPICAL DYNAMIC CHARACTERISTICS
at T_A = 25°C, V^+ = 12 V

AGC Range	68 dB
Power Gain	53 dB
Minimum rf AGC Range (term. 12)	0.2 V
Maximum rf AGC Range (term. 12)	7 V



SYNC POLARITY	* VOLTAGE AT TERMINAL 6	* VOLTAGE AT TERMINAL 10	* VALUE OF RI-Ω
NEGATIVE	5.5 V 2 V 0 V	I TO 4 V NOM=2 V	0
POSITIVE	I TO 8 V NOM=4.5	4.5 V 0 V	3.9k

Fig. 1 – CA1352E block diagram and typical AGC test set-up.

CA1391E, CA1394E

TV Horizontal Processors

CA1391E — Positive Horizontal Sawtooth Input
CA1394E — Negative Horizontal Sawtooth Input

Features:

- Internal shunt regulator
- Linear balanced phase detector
- Preset hold control capability
- ±300-Hz pull-in (typ.)
- Low thermal frequency drift
- Small static phase error
- Variable output duty cycle
- Adjustable dc loop gain

The RCA-CA1391E and CA1394E are monolithic integrated circuits designed for use in the low-level horizontal section of monochrome or color television receivers. Functions include a phase detector, an oscillator, a regulator, and a pre-driver.

The CA1391E and CA1394E are electrically equivalent and pin compatible with industry types 1391 and 1394 in similar packages.

These types are supplied in an 8-lead dual-in-line plastic (Mini-DIP) package, and operate over an ambient temperature range of 0 to +85°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC SUPPLY CURRENT	40 mA
DC OUTPUT VOLTAGE	40 V
DC OUTPUT CURRENT	30 mA
SYNC INPUT VOLTAGE	5 V_{p-p}
SAWTOOTH INPUT VOLTAGE	5 V_{p-p}
DEVICE DISSIPATION:	
Up to $T_A = 25^oC$	625 mW
Above $T_A = 25^oC$ derate linearly	5 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+260°C
THERMAL RESISTANCE	200°C/W

CIRCUIT OPERATION

(See schematic diagram, Fig.2)

The CA1391 and CA1394 contain the oscillator, phase detector, and predriver sections necessary for the television horizontal oscillator and AFC loop.

The oscillator is an RC type with terminal 7 used to control the timing. If it is assumed that Q7 is initially off, then an external capacitor connected from terminal 7 to ground charges through an external resistance connected between terminals 6 and 7. As soon as the voltage at terminal 7 exceeds the potential set at the base of Q8 by resistors R11 and R12, Q7 turns on, and Q6 supplies base current to Q5 and Q10. Transistor Q5 discharges the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time, Q7 turns off, and the cycle repeats.

The sawtooth generated at the base of Q4 appears across R3 and turn off Q3 whenever the sawtooth voltage rises to a value that exceeds the bias set at terminal 8. By adjusting the potential at terminal 8, the duty cycle at the pre-drive output (terminal 1) may be changed.

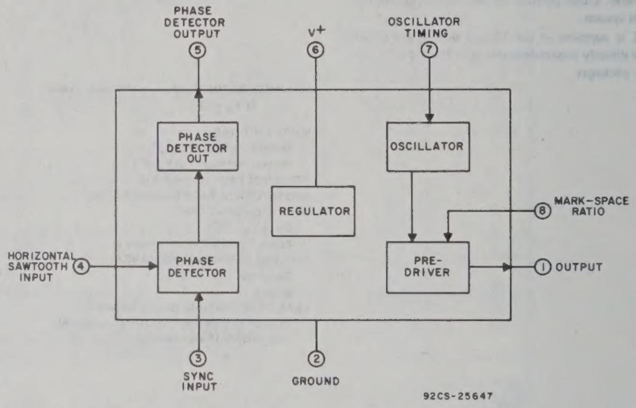


Fig.1 — Functional block diagram of the CA1391E, CA1394E.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$ (See Fig.3)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage	S1, S5, S6 = 2 S2, S3, S4, S7, S8 = 1 Measure term. 6 to Gnd	8	–	9	V
Free-Running Frequency	S1, S5, S6 = 2 S2, S3, S4, S7, S8 = 1 Counter to term. 1	14734	–	16734	Hz
Output Leakage	S2, S3, S6, S8 = 1 S1, S4, S5, S7 = 2 Measure term. 1 to 25 V	–	10	–	mV
Output Saturation	S2, S3, S5, S6, S8 = 1 S1, S4, S7 = 2 Measure term. 1 to Gnd	–	60	–	mV
Phase Detector Bias	S2, S5, S6, S8 = 1 S1, S3, S4, S7 = 2 Measure term. 3 to Gnd	–	1.9	–	V
Phase Detector Leak	S5, S8 = 1 S1, S2, S3, S4, S6, S7 = 2 Measure term. 5 to +4 V	−2	–	+2	mV
Phase Detector Low	S1, S5, S8 = 1 S2, S3, S4, S6, S7 = 2 Measure term. 5 to +4 V	−0.55*	–	–	V
Phase Detector High	S1, S5, S6, S8 = 1 S2, S3, S4, S7 = 2 Measure term. 5 to +4 V	+0.55*	–	–	V
Phase Detector Balance	$V_{DET2} + V_{DET3}$	−100	–	+100	mV
Sync Diode	S1, S2, S3, S4, S6, S7 = 1 S5, S8 = 2	0.3	–	1.2	V
Static Phase Error	See Fig.4	–	0.5	–	μs
Oscillator Pull-in Range		–	±300	–	Hz
Oscillator Hold-in Range		–	±900	–	Hz

* Polarity reversed in the CA1391.

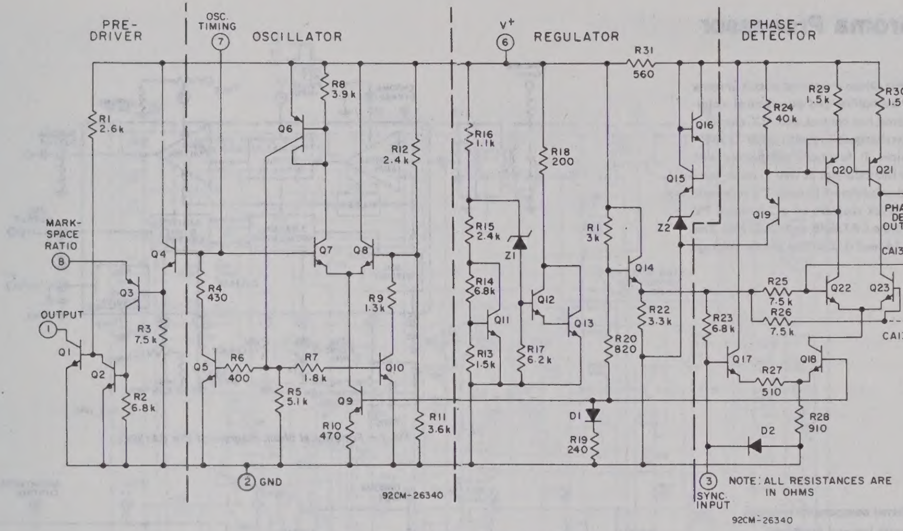


Fig.2 – Schematic diagram of CA1391E, CA1394E.

The phase detector is isolated from the remainder of the circuit by R31, Z2, Q15 and Q16. The phase detector consists of the comparator Q22 and Q23, and the gated current source Q18. Negative-going sync pulses at terminal 3 turn off Q17, and the current division between Q22 and Q23 is then determined by the phase relationship of the sync and the sawtooth waveform at terminal 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents flow in the collectors of Q22 and Q23 during each half of the sync pulse period. The current in Q22 is turned around by current mirror Q20 and Q21 so that there is no net output current at terminal 5 for balanced conditons. When a phase offset occurs, current flows either in or out of terminal 5. In circuit applications, this terminal is connected to terminal 7 through an external low-pass filter, thereby controlling the oscillator.

Shunt regulation for the circuit is obtained by using a V_{BE} and zener multiplier. Resistors R13 and R14 multiply the V_{BE} of Q11, and the ratio of R15 and R16 multiplies the voltage of the zener diode Z1.

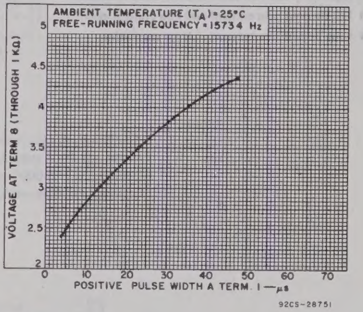


Fig.3 – Duty cycle at the pre-drive output (term.1) as it is affected by the input at term. 8.

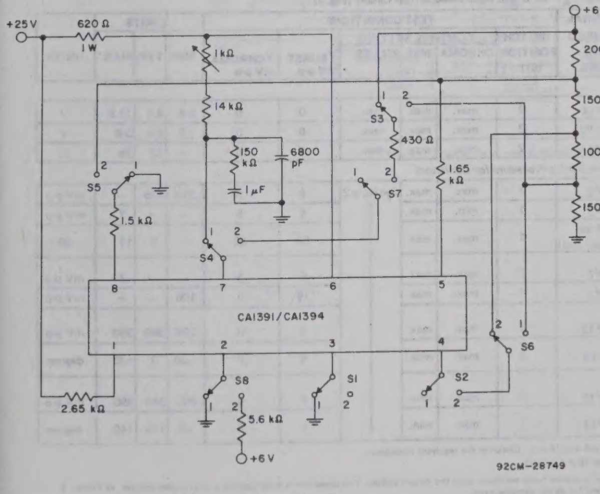


Fig.4 – DC test circuit.

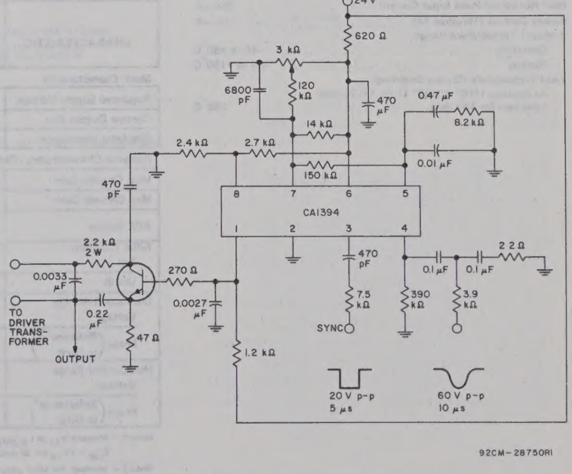


Fig.5 – Typical circuit application.

CA1398E

Television Chroma Processor

RCA-CA1398E is a monolithic silicon integrated-circuit chroma processor containing chroma-amplifier and gain-control, color-killer, color subcarrier oscillator, hue control, and ACC circuitry. It has been designed for interchangeability with other "1398"-type chroma-processor devices. It functions compatibly with the RCA-CA3125E Chroma Demodulator as well as other commercially available chroma demodulators in color-TV receivers. Fig. 2 shows a functional block diagram of a 2-package TV chroma system incorporating the CA1398E and CA3125E. The CA1398E is supplied in a 14-lead dual-in-line plastic package.

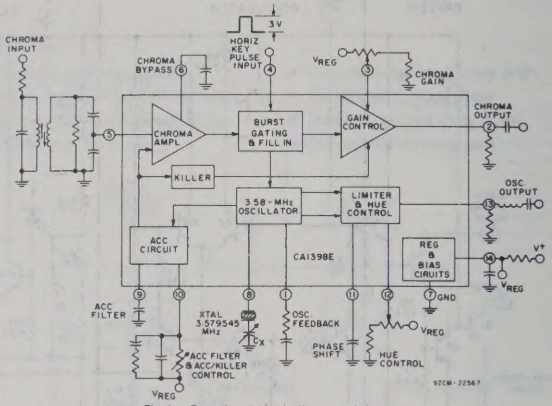


Fig. 1 – Functional block diagram of the CA1398E.

Features

- **Minimum number of external components required**
- **Injection-lock oscillator with internal feedback**
- **DC chroma gain control and hue control circuits**
- **Low-impedance internal voltage regulation**

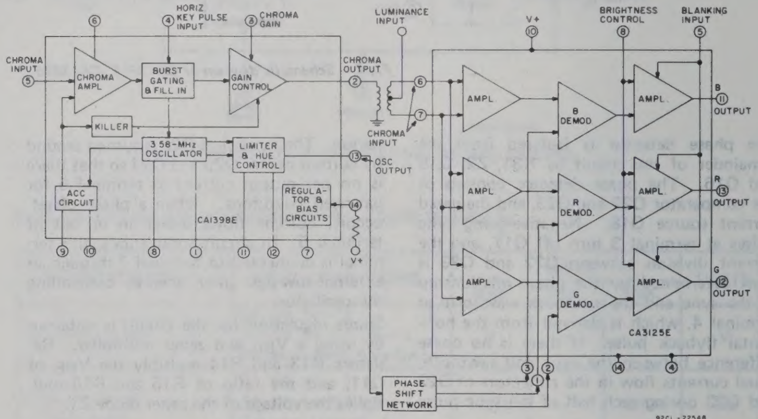


Fig. 2 – TV chroma system functional block diagram.

Maximum Ratings, ***Absolute-Maximum Values at $T_A = 25^\circ C$***

Peak Horizontal-Pulse Input Current	250 µA
Supply Current (Terminal 14)	35 mA
Ambient Temperature Range:	
Operating	–40 to +85°C
Storage	–65 to +150°C
Lead Temperature (During Soldering): At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$ and Referenced to Test Circuit (Fig. 4)

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS						LIMITS			UNITS
		SWITCH POSITION (S1)	CONTROL SETTING			V_{BURST} mV p-p	V_{CHROMA} mV p-p	MIN.	TYP.	MAX.	
			CHROMA	HUE	KILLER						
Static Characteristics											
Regulated Supply Voltage	V_{14}	2	max.	max.	max.	0	0	8.9	9.5	11.5	V
Chroma Output Bias	V_{14} to V_2	2	max.	max.	max.	6	0	1.2	2.4	3.6	V
Regulator Impedance	See Note 1	2	max.	max.	max.	0	0	–	12	25	Ω
Dynamic Characteristics (Refer to Test Set-Up Procedure for Oscillator)											
Max. Chroma Gain	V_2	1	max.	max.	See Note 2	6	5	310	425	–	mV p-p
Min. Chroma Gain	V_2	1	min.	max.		6	5	–	–	7	mV p-p
ACC Action	V_2 (dB up from gain test)	1	max.	max.		50	50	2	7	11	dB
Killer Function: Kill	V_2	2	max.	max.		0	5	–	–	7	mV p-p
Unkill	V_2	1	max.	max.		15	5	100	–	–	mV p-p
Oscillator Lock-Up: Voltage	V_{13}	1	max.	max.		6	0	250	340	390	mV p-p
Phase (Referenced to burst)	ϕ_{13}	1	max.	max.		6	0	–20	0	+20	degrees
Hue Control Range: Voltage	V_{13}	1	max.	min.		6	0	250	340	390	mV p-p
Phase (Referenced to burst)	ϕ_{13}	1	max.	min.		6	0	95	110	140	degrees

Note 1 – Measure V_{14} at I_{SUPPLY} = 38 mA and 18 mA. Calculate the regulator impedance:
$Z_{reg.} = [V_{14}\text{ (at 38 mA)} - V_{14}\text{ (at 18 mA)}]/0.02$

Note 2 – Increase the killer potentiometer resistance from minimum until the circuit unkills. This condition is evidenced by a shift in bias voltage at Term. 2 Maintain this potentiometer setting for all the dynamic tests.

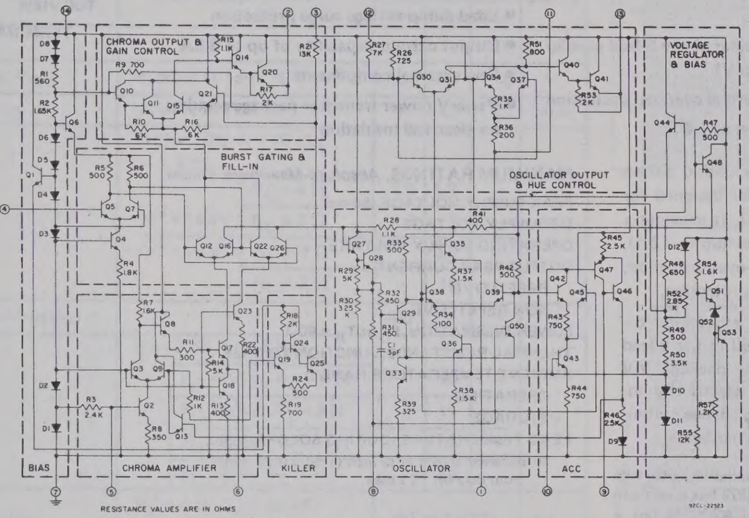


Fig. 3 – Schematic diagram of the CA1398E.

TEST SET-UP PROCEDURE FOR OSCILLATOR

Remove the horizontal keying and chroma inputs and adjust C_X to obtain a free-running oscillator frequency of 3.579545 MHz ±10 Hz. Under the same Test Conditions described in the Electrical Characteristics Chart for Oscillator Lock-Up, vary L1 (approx. 20 μH) and/or C1 (approx. 1000 pF) to obtain the initial conditions for amplitude and phase oscillator lock-up.

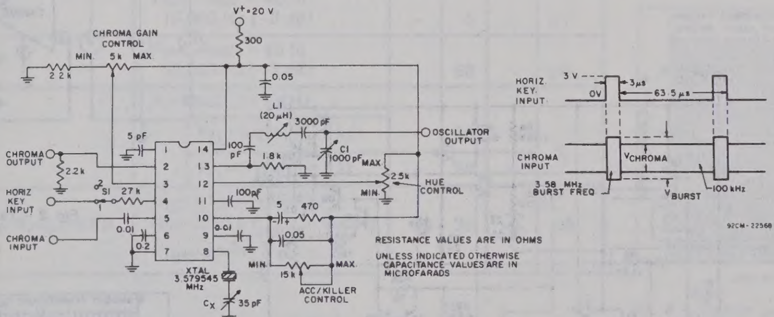


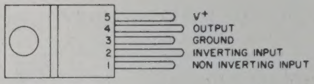
Fig. 4 – Typical static and dynamic characteristics test circuit for the CA1398E.

CA2002, CA2002M

Preliminary Data

8-Watt Audio Power Amplifier

For Automobile Radios



TOP VIEW

TERMINAL ASSIGNMENT

Features:

- **Hermetic Gold-CHIP encapsulated in a 5-lead plastic TO-220-style package (Versa-V)**
- **Output short-circuit and thermal overload protection**
- **Drives load impedance as low as 1.6 Ω**
- **Load dump voltage surge protection**
- **Output current capability of up to 3.5A**
- **Few external components**
- **Versa-V power transistor package-requires no electrical insulation**

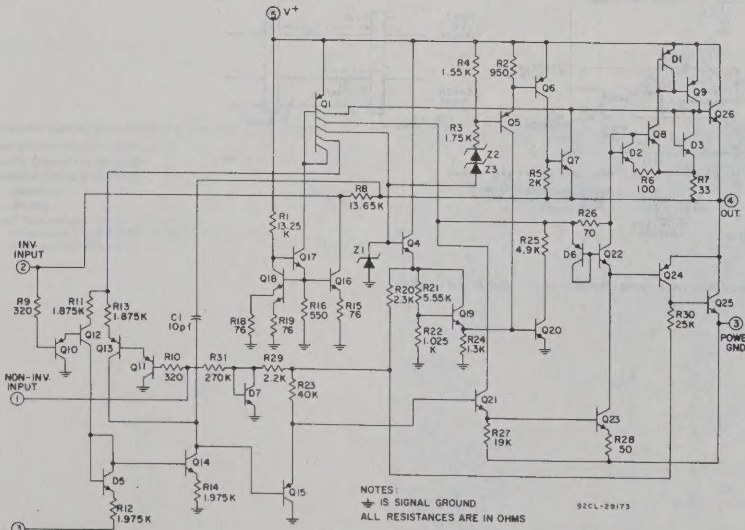
The RCA-CA2002 is a monolithic silicon class B audio power amplifier designed for driving loads as low as 1.6 Ω. It provides a high output current capability (up to 3.5A), very low harmonic and cross-over distortion, and load-dump voltage-surge protection.

The CA2002 is supplied in a hermetic trimetal Gold-CHIP encapsulated in the 5-lead plastic TO-220-style Versa-V package. All leads (except term. 3) are electrically insulated from the mounting flange, eliminating the need for insulating hardware.

The VERSA-V package is available with two lead configurations. The CA2002 has a vertical-mount lead form, and the CA2002M has a horizontal-mount lead form.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

PEAK SUPPLY VOLTAGE (50 ms)	40 V
DC SUPPLY VOLTAGE	28 V
OPERATING SUPPLY VOLTAGE	18 V
OUTPUT PEAK CURRENT:	
REPETITIVE	3.5 A
NON-REPETITIVE	4.5 A
POWER DISSIPATION, P_D at $T_A = 90^\circ C$	15 W
THERMAL RESISTANCE, JUNCTION TO CASE	4 °C/W
AMBIENT-TEMPERATURE RANGE:	
OPERATING	See Figure 16
STORAGE	−40 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 12 s max.	260°C



NOTES:
⏚ IS SIGNAL GROUND
ALL RESISTANCES ARE IN OHMS

Fig. 1 – Schematic diagram.

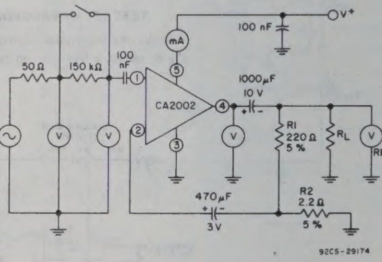


Fig. 2 – Test circuit.

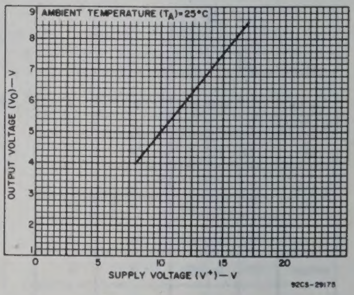


Fig. 3 – Typical quiescent output voltage as a function of supply voltage.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 14.4$ V
Unless otherwise specified (See Figure 2)

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Supply Voltage, V^+		8	–	18	V
Quiescent Output Voltage, V_O	Measure at Term. 4	6.4	7.2	8	V
Quiescent Drain Current, I_D	Measure at Term. 5	–	45	80	mA
Output Power, P_O	THD = 10%, A = 40 dB, f = 1 KHz				W
	$V^+ = 14.4$V, $R_L = 4\ \Omega$	4.8	5.2	–	
	$V^+ = 14.4$V, $R_L = 2\ \Omega$	7	8	–	
	$V^+ = 16$ V, $R_L = 4\ \Omega$	–	6.5	–	
	$V^+ = 16$ V, $R_L = 2\ \Omega$	–	10	–	
Input Saturation Voltage, $V_{I(RMS)}$		400	–	–	mV
Input Sensitivity, e_I	A = 40 dB, f = 1 KHz				mV
	$P_O = 0.5$ W, $R_L = 4\ \Omega$	–	15	–	
	$P_O = 0.5$ W, $R_L = 2\ \Omega$	–	11	–	
	$P_O = 5.2$ W, $R_L = 4\ \Omega$	–	55	–	
	$P_O = 8$ W, $R_L = 2\ \Omega$	–	50	–	
Frequency Response (–3 dB)	$R_L = 4\ \Omega$, $C_X = 39$ nF, $R_X = 39\ \Omega$ (See Figs.15,20)	40 to 15000			Hz
Input Resistance, R_I (Term. 1)	f = 1 KHz	70	150	–	KΩ
Open-Loop Voltage Gain, A_{OL}	$R_L = 4\ \Omega$, f = 1 KHz	–	80	–	dB
Closed-Loop Voltage Gain, A	$R_L = 4\Omega$, f = 1 KHz	39.5	40	40.5	dB
Input Noise Voltage, e_N	Freq. Resp. = 40 to 15,000 Hz (–3 dB)	–	4	–	µV
Input Noise Current, i_N	Freq. Resp. = 40 to 15,000 Hz (–3 dB)	–	60	–	pA
Efficiency, η	A = 40 dB, f = 1 KHz				%
	$P_O = 5.2$ W, $R_L = 4\ \Omega$	–	68	–	
	$P_O = 8$ W, $R_L = 2\ \Omega$	–	58	–	
Power Supply Rejection Ratio, PSRR	$R_L = 4\ \Omega$, A = 40 dB, Rg = 10 KΩ, $f_{ripple} = 100$ Hz, $V_{ripple} = 0.5$ V	30	35	–	dB

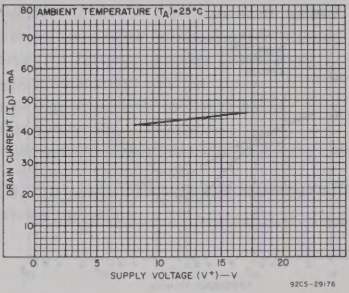


Fig. 4 – Typical quiescent drain current as a function of supply voltage.

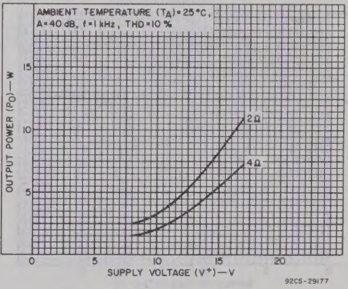


Fig. 5 – Typical output power as a function of supply voltage.

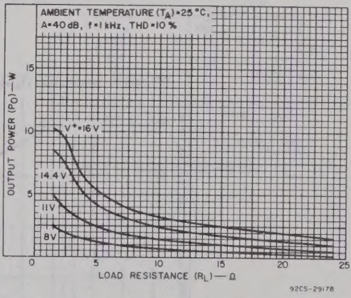


Fig. 6 – Typical output power as a function of load resistance.

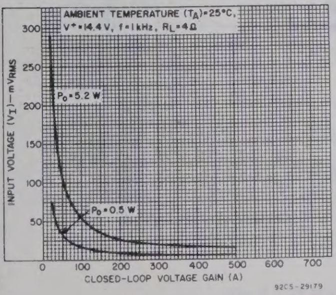


Fig. 7 – Typical input voltage as a function of closed-loop voltage gain.

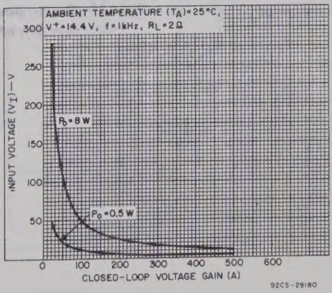


Fig. 8 – Typical input voltage as a function of closed-loop voltage gain.

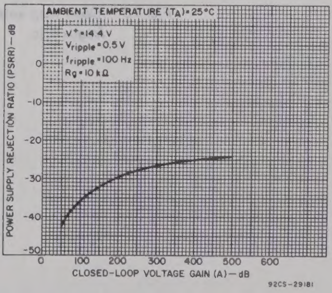


Fig. 9 – Typical power supply rejection ratio as a function of closed-loop voltage gain.

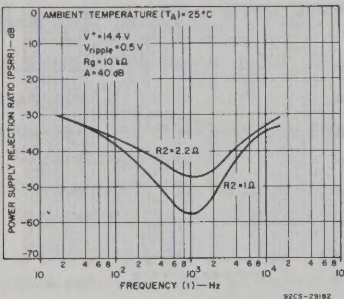


Fig. 10 — Typical power supply rejection ratio as a function of frequency.

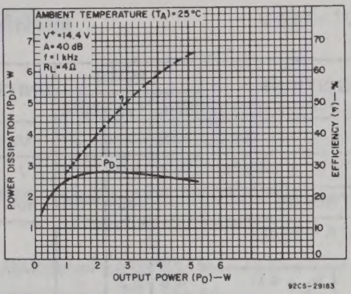


Fig. 11 — Typical power dissipation and efficiency as a function of output power.

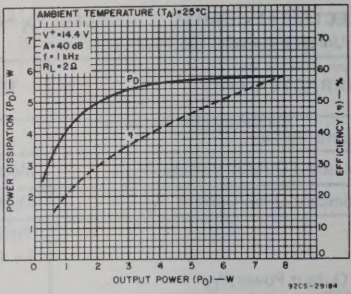


Fig. 12 — Typical power dissipation and efficiency as a function of output power.

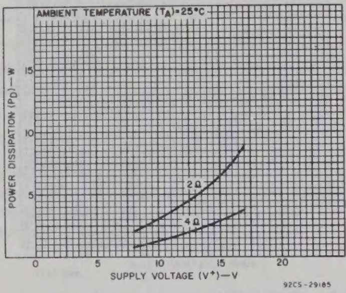


Fig. 13 — Maximum power dissipation as a function of supply voltage (sine-wave operation).

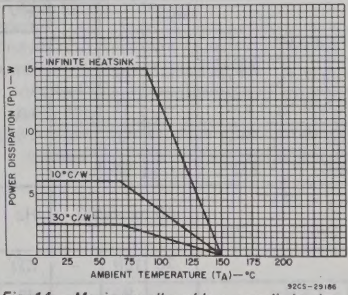


Fig. 14 — Maximum allowable power dissipation as a function of ambient temperature.

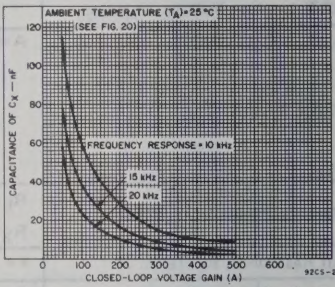


Fig. 15 — Typical values of capacitor C_X (see test circuit, figure 20) for different values of frequency response.

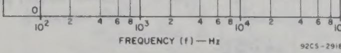


Fig. 16 — Open-loop voltage gain as a function of frequency.

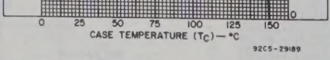


Fig. 17 — Output power and drain current as a function of case temperature.

CA2004, CA2004M

12-Watt Audio Power Amplifier

The RCA-CA2004 is a monolithic silicon class B audio power amplifier designed for driving loads as low as 3.2 Ω. It provides a high output current capability (up to 3.5 A), and very low harmonic and cross-over distortion.

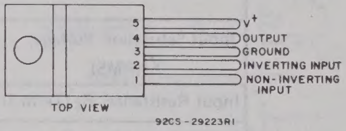
The CA2004 is supplied in a hermetic tri-metal Gold-CHIP encapsulated in the 5-lead plastic TO-220-style VERSA-V package. All leads (except term. 3) are electrically insulated from the mounting flange, eliminating the need for insulating hardware. The VERSA-V package is available with two lead configurations. The CA2004 has a vertical-mount lead form, and the CA2004M has a horizontal-mount lead form.

Features:

- Hermetic Gold-CHIP encapsulated in a 5-lead plastic TO-220-style package (VERSA-V)
- Thermal overload protection
- Drives load impedance as low as 3.2 Ω
- Deflection amplifier capability
- Output current capability of up to 3.5 A
- Few external components
- VERSA-V power transistor package-requires no electrical insulation

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	28 V
OPERATING SUPPLY VOLTAGE	26 V
OUTPUT PEAK CURRENT:	
REPETITIVE	3.5 A
NON-REPETITIVE	4.5 A
POWER DISSIPATION, P_D at $T_A = 90^\circ C$	15 W
THERMAL RESISTANCE, JUNCTION TO CASE	$4^\circ C/W$
AMBIENT-TERMPERATURE RANGE:	
OPERATING	0 to +125°C
STORAGE	−40 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 12 s max.	260°C



TERMINAL ASSIGNMENT

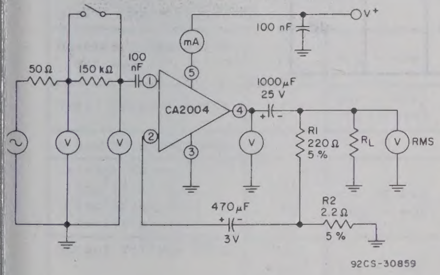


Fig. 1 – Test circuit.

Thermal Shut-Down

Thermal shut-down occurs if the output overloads (temporary or permanent), the ambient temperature is excessive, or the junction temperature is excessive. None of these conditions results in device damage. They merely cause a temporary automatic reduction of output power and drain current.

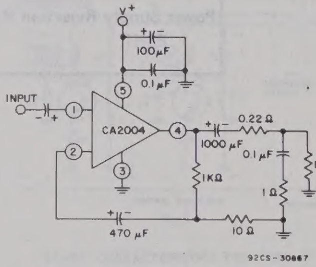


Fig. 2 – Typical application.

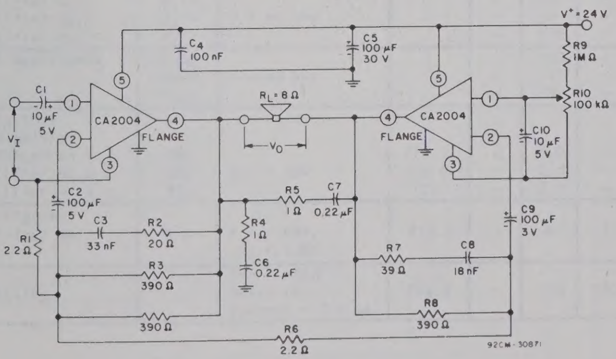


Fig. 3 – 25 W circuit-bridge application.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 24$ V
Unless otherwise specified (See Figure 1)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage, V^+		8	–	26	V
Quiescent Output Voltage, V_O	Measure at Term. 4	11	12	13	V
Quiescent Drain Current, I_D	Measure at Term. 5	–	40	100	mA
Output Power, P_O	THD = 10%, A = 40 dB, f = 1 KHz $R_L = 4\ \Omega$	10	12	–	W
	$R_L = 8\ \Omega$	–	8	–	
Input Saturation Voltage, $V_{I(RMS)}$		400	–	–	mV
Input Resistance, R_I (Term.1)	f = 1 KHz	70	150	–	KΩ
Open-Loop Voltage Gain, A_{OL}	$R_L = 8\Omega$, f = 1 KHz	–	80	–	dB
Closed-Loop Voltage Gain, A	$R_L = 8\Omega$, f = 1 KHz	39.5	40	40.5	dB
Input Noise Voltage, e_N	Freq. Resp. = 40 to 15,000 Hz (–3 dB)	–	4	–	μV
Power Supply Rejection Ratio, PSRR	$R_L = 4\ \Omega$, A = 40 dB, $R_g = 10\ K\Omega$, $f_{ripple} = 100$ Hz, $V_{ripple} = 0.5$ V	30	35	–	dB

CA3035, CA3035V1

Ultra-High-Gain Wide-Band Amplifier Array

- Three Individual General-Purpose Amplifiers
- Ideal for service in Remote-Control Amplifiers — — e.g., TV Receivers
- Available in two electrically identical versions: CA3035 with straight leads; CA3035V1 with formed leads

HIGHLIGHTS

- Three separate amplifiers — gain and bandwidth for each amplifier can be adjusted with suitable external circuitry
- Amplifiers operable independently or in cascade
- Exceptionally high cascade voltage gain — 129 dB typ. at 40 kHz
- Low noise performance
- Wide-band response
- All amplifiers single-ended — only one power supply required
- Wide operating temperature range — -55°C to +125°C
- Built-in temperature compensation
- Hermetically sealed, all-welded 10-lead TO-5-style metal package with straight or formed leads

ABSOLUTE-MAXIMUM RATINGS:

Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Device Dissipation	300 mW
Input Voltage	1 V p-p
Supply Voltage	+15V
Lead Temperature (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUITS AND CHARACTERISTICS CURVES	LIMITS CA3035, CA3035V1			UNITS
				Min.	Typ.	Max.	
STATIC CHARACTERISTICS							
Quiescent Operating Voltage	V_3 V_5 V_7	V_{CC} = +9V	Fig.3	– – –	2 1.9 4.9	– – –	V V V
Total Current Drain	I_d	V_{CC} = +9V, R_{L3} = 5KΩ	Fig.3	3.5	5	7.5	mA
DYNAMIC CHARACTERISTICS							
Voltage Gain: Amplifier No.1 Amplifier No.2 Amplifier No.3	A_1 A_2 A_3	f = 40 kHz, V_{CC} = +9V		40 40 38	44 46 42	– – –	dB dB dB
Output Voltage Swing	V_{out} V_{1out} V_{2out} V_{3out}	R_{L1} = 10KΩ R_{L2} = 10KΩ R_{L3} = 5KΩ Sinusoidal Output, V_{CC} = +9V		– – –	2 2.6 8	– – –	Vp-p Vp-p Vp-p
Input Resistance: Amplifier No.1 Amplifier No.2 Amplifier No.3	R_{1in} R_{2in} R_{3in}	f = 40 kHz		– – –	50K 2K 670	– – –	Ω Ω Ω
Output Resistance	R_{1out} R_{2out} R_{3out}	f = 40 kHz		– – –	270 170 100K	– – –	Ω Ω Ω
Bandwidth at -3dB point: Amplifier No.1 Amplifier No.2 Amplifier No.3	BW_1 BW_2 BW_3	V_{CC} = +9V	Fig.5 Fig.6 Fig.7	– – –	500 2.5 2.5	– – –	kHz MHz MHz
Noise Figure Amplifier No.1	NF_1	f = 1 kHz, R_S = 1 KΩ	Fig.4	–	6	7	dB
Sensitivity		V_{CC} = +13 V Relay (K_1) Current = 7.5 mA	Fig.2	–	100	150	µV

SCHEMATIC DIAGRAM FOR CA3035 AND CA3035V1

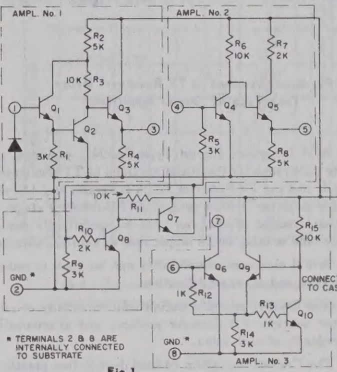
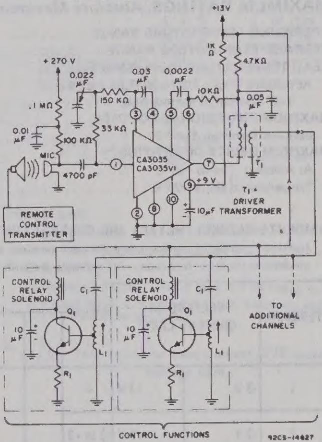


Fig.1

92CS-14626R1

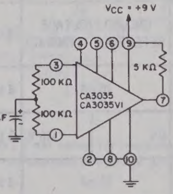
TYPICAL REMOTE CONTROL SYSTEM



92CS-14627

Fig.2

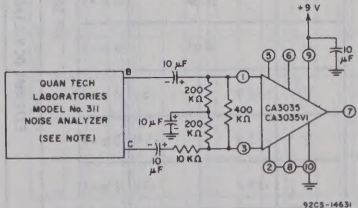
STATIC CHARACTERISTICS TEST CIRCUIT



92CS-14625

Fig.3

NOISE FIGURE TEST CIRCUIT



+9 V
10 µF
QUAN TECH LABORATORIES MODEL No. 311 NOISE ANALYZER (SEE NOTE)
B
C
10 µF
200 KΩ
400 KΩ
10 µF
200 KΩ
10 KΩ
CA3035 CA3035V1

92CS-14631

NOTE: SET ALL INTERNAL POWER SUPPLIES ON QUAN TECH NOISE ANALYZER TO ZERO VOLTS.

Fig.4

CA3041

Wideband Amplifier, FM Detector, AF Preamplifier/Driver

For Sound Sections of TV Receivers Using
Tube-Type AF Output Amplifiers

FEATURES

- high-sensitivity – input limiting voltage (knee) = 150 μV typ. at 4.5 MHz
- large audio drive voltage capability
- excellent AM rejection – 58 dB typ. at 4.5 MHz
- inherent high stability – internally shielded
- internal Zener-diode-regulated voltage supply
- low harmonic radiation
- wide frequency capability – <100 kHz to > 20 MHz
- low harmonic distortion

RCA Integrated Circuit Type CA3041 provides, in a single monolithic silicon chip, a major subsystem for the sound sections of TV receivers. As shown in the Schematic Diagram (Fig.1) and the TV Receiver Block Diagrams (Fig. 12) the CA3041 contains a multistage wideband if-amplifier/limiter section, an FM-detector stage, a Zener-diode-regulated power-supply section, and an af-amplifier section specifically designed to drive directly a 6AQ5 beam power tube or other audio output tube of similar characteristics.

In FM receivers, the CA3041 can be used to provide if amplification and limiting, FM detection, and af preamplification.

The CA3041 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The CA3041 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitably punched printed-circuit boards.

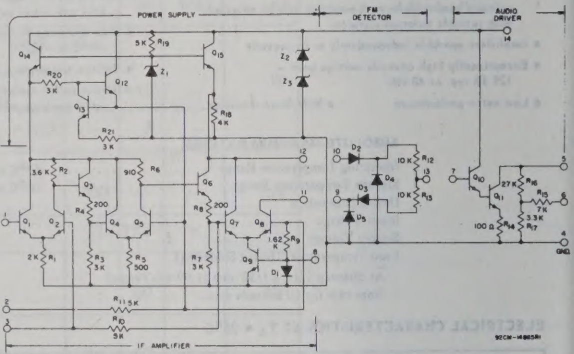


Fig.1 - Schematic diagram.

MAXIMUM RATINGS, *Absolute Maximum Values:*

OPERATING-TEMPERATURE RANGE .... –40° to +85°C
STORAGE-TEMPERATURE RANGE .... –65° to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. .... +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 3 .... ±3 V
MAXIMUM DEVICE DISSIPATION:
At Ambient Temperatures up to +25°C .... 950 mW
At Ambient Temperatures above +25°C .... Derate at 10.8 mW/°C

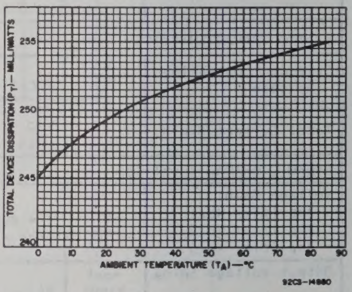


Fig.2 - Typical dissipation characteristic for CA3041.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS AT $T_A = 25°C$

Indicated voltage or current limits for each terminal may be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 4).

TERMINAL	VOLTAGE OR CURRENT LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS													
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	-3 V	+3 V	–	AT SAME DC VOLTAGE AS TERMINAL 1	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	GROUND (VOLTAGE REFERENCE TERMINAL)	CONNECTED TO +140 V THROUGH 47 kΩ RESISTOR*	CONNECTED TO TERMINAL 7 THROUGH 100 kΩ RESISTOR*	AF-INPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 9)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 10)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 11)	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AT TERMINAL 12 (EXCEPT TERMINAL 13)	CONNECTED TO +140 V DC THROUGH 6.2-kΩ RESISTOR*
2	-3 V	+3 V	-3 to +3													
3	-3 V	+3 V	-3 to +3													
4	GROUND (VOLTAGE REFERENCE TERMINAL)		-3 to +3													
5	20 mA		-3 to +3													
6	0 V	+10 V	-3 to +3													
7	10 mA		-3 to +3													
8	10 mA		-3 to +3													
9	10 mA		-3 to +3													
10	10 mA		-3 to +3													
11	+2.5 V	+5 V	-3 to +3													
12	+2.5 V	+5 V	-3 to +3													
13	+2.5 V	+5 V	-3 to +3													
14	50 mA		-3 to +3													

* Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Device Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3041 to be exceeded may be used.

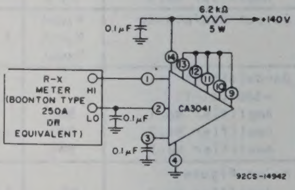
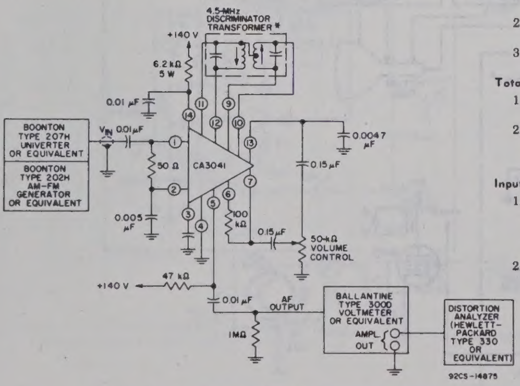


Fig.3 - Test setup for measurement of input-impedance components.

ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3041 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS			LIMITS				TYPICAL CHARACTERISTICS CURVES
		SETUP AND PROCEDURE	SPECIAL CONDITIONS		TYPE CA3041				
		Fig.			Min.	Typ.	Max.	Units	Fig.
Total Device Dissipation	P_T	11	T_A = 0°C		220	245	270	mW	2
			+25°C		225	250	275	mW	
			+85°C		230	255	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	–			10.5	11.2	12.3	V	–
Quiescent Operating Current (into Terminal 11)	I_{11}	11			0.25	0.63	1	mA	–
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	11	V_{CC} = +9 V applied directly to Terminal 14		7	11	16	mA	–
Input-Impedance Components: Parallel Input Resistance	R_i	3	f = 4.5 MHz		–	11	–	kΩ	–
Parallel Input Capacitance	C_i	3			–	5	–	pF	–
Output-Impedance Components: Parallel Output Resistance	R_o	–			–	100	–	kΩ	–
Parallel Output Capacitance	C_o	–			–	4	–	pF	–
Input Limiting Voltage (Knee)	$V_{i(lim)}$	7			–	150	200	μV (rms)	4
Amplitude-Modulation Rejection	AMR	10			45	58	–	dB	9
IF-Amplifier Voltage Gain	$A_{(IF)}$	5			–	67	–	dB	4
Recovered AF Voltage: 1. At FM-Detector Output	$V_o(af)$	–		R_L = 50 kΩ, Δf = ±25 kHz THD = 0.7% (typ.)	–	250	–	mV (rms)	–
2. At AF-Driver Output in Test Setup		–		THD < 5%	8	9	–	V (rms)	–
Total Harmonic Distortion	THD	7		$V_{o(af)}$ = 8 $V_{(rms)}$	–	1.5	5	%	–
Discriminator Output Resistance	$R_{o(dis)}$	–	f = 1 kHz		–	10	–	kΩ	–
AF-Amplifier Input Resistance	$R_{i(af)}$	–			–	100	–	kΩ	–
AF-Amplifier Output Resistance	$R_o(af)$	–			–	30	–	kΩ	–
AF-Driver Voltage Gain	A_{af}	6			–	41	–	dB	8


4.5-MHz DISCRIMINATOR TRANSFORMER *
+140 V
6.2 kΩ 5 W
0.01 μF
BOONTON TYPE 207H UNIVERTER OR EQUIVALENT
BOONTON TYPE 202H AM-FM GENERATOR OR EQUIVALENT
V_{IN}
0.01 μF
50 Ω
CA3041
0.0047 μF
0.15 μF
0.005 μF
100 kΩ
0.15 μF
50-kΩ VOLUME CONTROL
47 kΩ
+140 V
0.01 μF
AF OUTPUT
1 MΩ
BALLANTINE TYPE 3000 VOLTMETER OR EQUIVALENT
AMPL. OUT
DISTORTION ANALYZER (HEWLETT-PACKARD TYPE 330 OR EQUIVALENT)
92CS-14875

PROCEDURES:

Recovered AF Voltage:

1. Set Input Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1 kHz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output.
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 300 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (300 mV - 3 dB = 210 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).

* TRW Electronics, Des Plaines, Illinois, Part No. E023874, or equivalent.

Fig.7 - Test setup for measurement of input limiting voltage (Knee), recovered AF voltage, and total harmonic distortion.

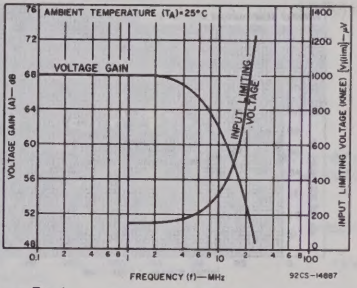
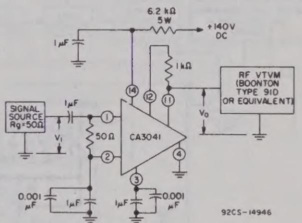


Fig.4 - Typical IF-amplifier voltage gain and input-limiting voltage (knee) characteristics.



PROCEDURE:

A - Voltage Gain:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

Fig.5 - Test setup for measurement of IF-amplifier voltage gain.

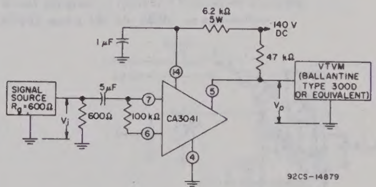


Fig.6 - Test setup for measurement of AF-amplifier voltage gain.

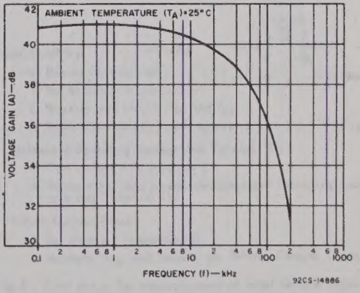


Fig.8 - Typical AF-driver voltage-gain characteristic

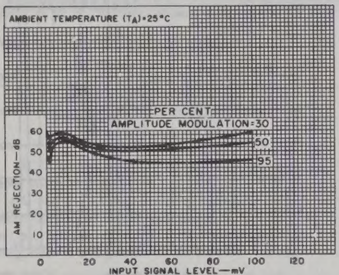
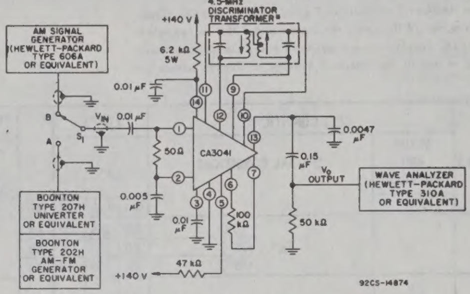


Fig.9 - Typical AM rejection characteristics for CA3041.


4.5-MHz DISCRIMINATOR TRANSFORMER*
+140 V
AM SIGNAL GENERATOR (HEWLETT-PACKARD TYPE 606A OR EQUIVALENT)
6.2 kΩ 5W
0.01 µF
B
A
V_{IN}
0.01 µF
S_1
50Ω
CA3041
0.0047 µF
0.15 µF
V_o OUTPUT
WAVE ANALYZER (HEWLETT-PACKARD TYPE 310A OR EQUIVALENT)
50 kΩ
BOONTON TYPE 207H UNIVERTER OR EQUIVALENT
BOONTON TYPE 202H AM-FM GENERATOR OR EQUIVALENT
0.005 µF
0.01 µF
100 kΩ
47 kΩ
+140 V
92CS-14874

PROCEDURES:

1. Set FM Signal Generator as follows:

   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms

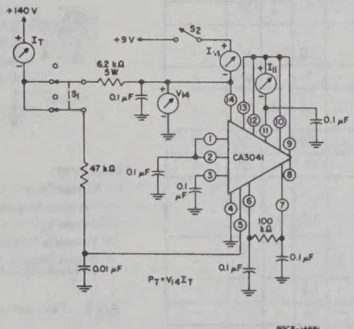
2. Set AM Signal Generator as follows:

   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Per cent modulation = 30
   Output level for V_{in} = 10 mV rms

3. With S_1 in Position A measure AF Output Voltage and record as $V_{o(FM)}$.
4. With S_1 in Position B measure AF Output Voltage and record as $V_{o(AM)}$.
5. Determine AM Rejection from $AMR = V_{o(FM)}/V_{o(AM)}$

* TRW Electronics, Des Plaines, Illinois. Part No. E023874, or equivalent.

Fig.10 - Test setup for measurement of AM rejection.



PROCEDURES:

Total Device Dissipation:

1. Close S_1, open S_2.
2. Measure and record V_{14} and I_T.
3. Determine Total Device Dissipation from $P_T = V_{14} I_T$.

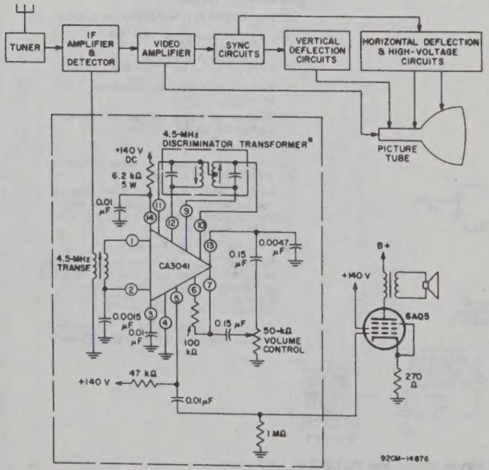
Quiescent Operating Current into Terminal 11:

1. Close S_1, open S_2.
2. Measure I_{11} and record as Quiescent Operating Current into Terminal 11.

9-Volt Current Drain:

1. Open S_1, close S_2.
2. Measure I_{14} and record as 9-Volt Current Drain.

Fig.11 - Test setup for total dissipation, quiescent operating current into terminal No.11, and 9-volt current drain.



* TRW Electronics, Des Plaines, Illinois. Part No. E023874, or equivalent.

Fig.12 - Block diagram of typical TV receiver using CA3041.

Wideband Amplifier, FM Detector, AF Preamplifier/Driver

For Sound Sections of TV Receivers Using Transistor-Type AF Output Amplifiers

FEATURES

- high sensitivity — input limiting voltage (knee) = 150 μV typ. at 4.5 MHz
- 6-mA audio drive capability
- excellent AM rejection — 58 dB typ. at 4.5 MHz
- inherent high stability — internally shielded
- internally Zener-diode-regulated voltage supply
- low harmonic radiation
- wide frequency capability — <100 kHz to >20 MHz
- low harmonic distortion

RCA Integrated Circuit Type CA3042 provides, in a single monolithic silicon chip, a major sub-system for the sound sections of TV receivers. As shown in the Schematic Diagram (Fig.1) and the TV Receiver Block Diagrams (Figs.2A and 2B) the CA3042 contains a multistage wide-band if-amplifier section, an FM-detector stage, a Zener-diode-regulated power-supply section, and an af-amplifier section specifically designed to drive directly an n-p-n audio output transistor or a high-gain audio output pentode tube.

In FM receivers, the CA3042 can be used to provide if amplification and limiting, FM detection, and af preamplification.

The CA3042 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The CA3042 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitably punched printed-circuit boards.

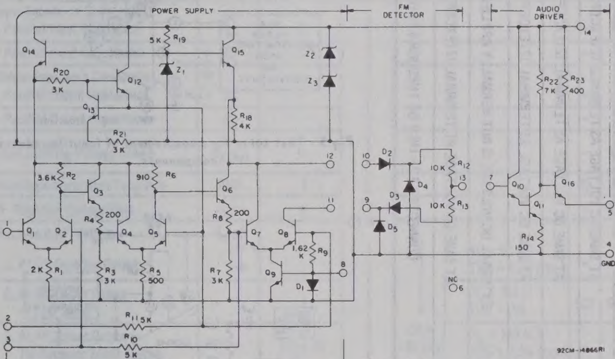


Fig.1 - Schematic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

OPERATING-TEMPERATURE RANGE .... −40° to +85°C
STORAGE-TEMPERATURE RANGE .... −65° to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. .... +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 3 .... ±3 V
MAXIMUM DEVICE DISSIPATION:
At Ambient Temperatures up to +25°C .... 950 mW
At Ambient Temperatures above +25°C .... Derate at 10.8 mW/°C

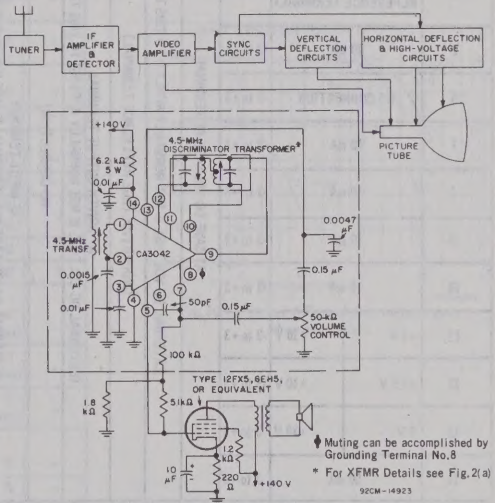

TUNER
IF AMPLIFIER & DETECTOR
VIDEO AMPLIFIER
SYNC CIRCUITS
VERTICAL DEFLECTION CIRCUITS
HORIZONTAL DEFLECTION & HIGH-VOLTAGE CIRCUITS
PICTURE TUBE
+140 V
6.2 kΩ 5 W
0.01 µF
4.5-MHz DISCRIMINATOR TRANSFORMER*
4.5-MHz TRANSF
CA3042
0.0015 µF
0.01 µF
0.0047 µF
0.15 µF
50pF
0.15 µF
50-kΩ VOLUME CONTROL
100 kΩ
TYPE 12FX5, 6EH5, OR EQUIVALENT
51 kΩ
1.8 kΩ
1.2 kΩ
10 µF
220 Ω
+140 V
♦ Muting can be accomplished by Grounding Terminal No.8
* For XFMR Details see Fig.2(a)
92CM-14923

Fig.2(b) - Block diagram of typical TV receiver utilizing the CA3042 and a 12FX5, 6EH5, or equivalent.

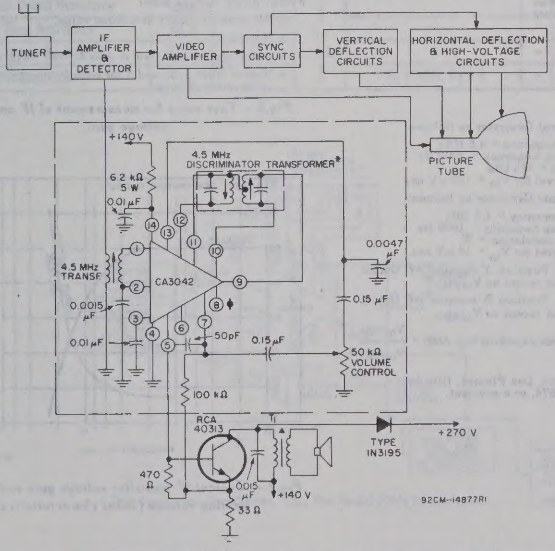
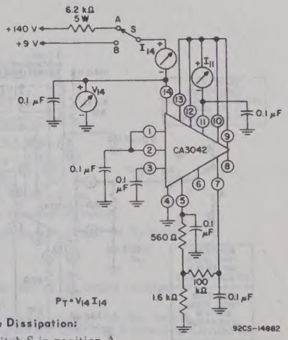


Fig. 2(a) - Block diagram of typical TV receiver utilizing transistor RCA-40313.



PROCEDURES:

Total Device Dissipation:

1. Set switch S in position A
2. Measure and record V_{14} and I_{14}.
3. Determine Total Device Dissipation from $P_T = V_{14}I_{14}$

Quiescent Operating Current into Terminal 11:

1. Turn switch S to position B
2. Measure I_{11} and record as Quiescent Operating Current into Terminal 11.

9-Volt Current Drain:

1. Set switch S in position B
2. Measure I_{14} and record as 9-Volt Current Drain.

Fig.3 - Test setup for measurement of total device dissipation, quiescent current into terminal No.11, and 9-volt current drain.

CA3042

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS AT T_A = 25°C

Indicated voltage or current limits for each terminal may be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 4).

TERMINAL	VOLTAGE OR CURRENT LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS													
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	-3 V	+3 V	–	AT SAME DC VOLTAGE AS TERMINAL 1	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	GROUND (VOLTAGE REFERENCE TERMINAL)	AF-DRIVER OUTPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	NO CONNECTION	AF-INPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	MUTING TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL EXCEPT THAT TERMINAL MAY BE GROUNDED TO OBTAIN MUTING ACTION)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 9)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 10)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 11)	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AT TERMINAL 12 (EXCEPT TERMINAL 13)	CONNECTED TO +140 V DC THROUGH 6.2-kΩ RESISTOR*
2	-3 V	+3 V	-3 to +3													
3	-3 V	+3 V	-3 to +3													
4	GROUND (VOLTAGE REFERENCE TERMINAL)		-3 to +3													
5	20 mA		-3 to +3													
6	NO CONNECTION		-3 to +3													
7	10 mA		-3 to +3													
8	10 mA		-3 to +3													
9	10 mA		-3 to +3													
10	10 mA		-3 to +3													
11	+2 V	+10 V	-3 to +3													
12	+2.5 V	+10 V	-3 to +3													
13	0 V	+10 V	-3 to +3													
14	50 mA		-3 to +3													

* Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Device Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3042 to be exceeded may be used.

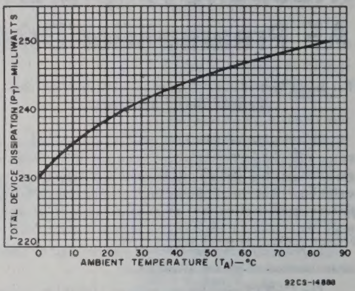


Fig.4 - Typical dissipation characteristic.

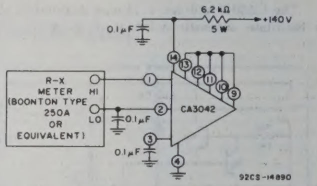
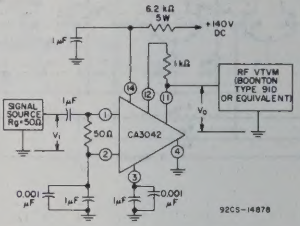


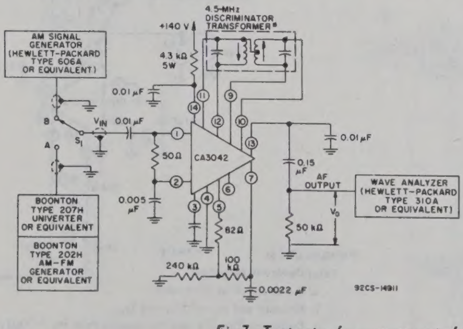
Fig.5 - Test setup for measurement of input-impedance components.



PROCEDURE Voltage Gain:

1. Set input frequency at desired value, v_i = 100 µV rms.
2. Record v_o.
3. Calculate Voltage Gain A from A = 20 $\log_{10} v_o/v_i$.
4. Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

Fig.6 - Test setup for measurement of IF amplifier voltage gain.



AM SIGNAL GENERATOR (HEWLETT-PACKARD TYPE 606A OR EQUIVALENT)
+140 V
4.5-MHz DISCRIMINATOR TRANSFORMER*
4.3 kΩ 5W
0.01 µF
B
A
V_{IN}
0.01 µF
S_1
50Ω
CA3042
0.005 µF
0.01 µF
0.15 µF
AF OUTPUT
V_o
50 kΩ
WAVE ANALYZER (HEWLETT-PACKARD TYPE 310A OR EQUIVALENT)
BOONTON TYPE 207H UNIVERTER OR EQUIVALENT
BOONTON TYPE 202H AM-FM GENERATOR OR EQUIVALENT
62Ω
100 kΩ
240 kΩ
0.0022 µF
92CS-14911

PROCEDURES:

1. Set FM Signal Generator as follows:
   Output Frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Deviation = ±25 kHz
   Output level for V_{in} = 100 mV rms
2. Set AM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Per cent modulation = 30
   Output level for V_{in} = 10 mV rms
3. With S_1 in Position A measure AF Output Voltage and record as $V_{o(FM)}$.
4. With S_1 in Position B measure AF Output Voltage and record as $V_{o(AM)}$.
5. Determine AM Rejection from AMR = $\frac{V_{o(FM)}}{V_{o(AM)}}$

* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.7 - Test setup for measurement of AM rejection.

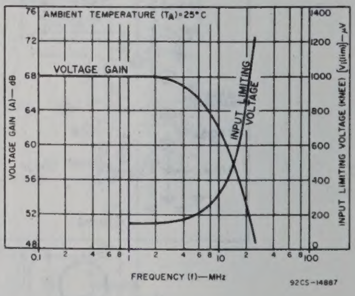


Fig.8 - Typical IF amplifier voltage gain and input limiting voltage (knee) characteristics.

ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3042 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS				LIMITS				TYPICAL CHARACTERISTICS CURVES
		SETUP AND PROCEDURE	SPECIAL CONDITIONS			TYPE CA3042				
		Fig.				Min.	Typ.	Max.	Units	Fig.
Total Device Dissipation	P_T	3	T_A = 0°C			200	230	260	mW	4
			T_A = +25°C			210	240	270	mW	
			T_A = +85°C			220	250	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	–				10.5	11.2	12.3	V	–
Quiescent Operating Current (into Terminal 11)	I_{11}	3				0.25	0.63	1	mA	–
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	3	V_{CC} = +9 V applied directly to Terminal 14			8	12	18	mA	–
Input-Impedance Components: Parallel Input Resistance	R_I	5	f = 4.5 MHz			–	11	–	kΩ	–
Parallel Input Capacitance	C_I	5				–	5	–	pF	–
Output-Impedance Components: Parallel Output Resistance	R_0	–				–	100	–	kΩ	–
Parallel Output Capacitance	C_0	–				–	4	–	pF	–
Input Limiting Voltage (Knee)	$V_{i(lim)}$	11				–	150	200	μV (rms)	8
Amplitude-Modulation Rejection	AMR	7				45	58	–	dB	–
IF-Amplifier Voltage Gain	$A_{(IF)}$	6				–	67	–	dB	8
Recovered AF Voltage: 1. At FM-Detector Output	$V_0(af)$	11		Δf = ±25 kHz	R_L = 50 kΩ THD = 0.7% (typ.)	–	250	–	mV (rms)	–
2. At AF-Driver Output in Test Setup		11			R_L = 322 Ω THD < 5%	500	800	–	mV (rms)	–
3. At AF-Driver Output in TV-Receiver Sound System		2A or 2B			R_L = 150 kΩ THD = 1.5% (typ.)	–	3	–	V (rms)	–
Total Harmonic Distortion: 1. In Test Setup	THD	11			$V_0(af)$ = 500 mV (rms)	–	1.5	5	%	–
2. In TV Receiver Sound System		2A or 2B			$V_{0(af)}$ = 1.3 V (rms)	–	1	–	%	–
FM-Detector Output Resistance	$R_{o(det)}$	–	f = 1 kHz			–	10	–	kΩ	–
AF-Driver Input Resistance	$R_{I(af)}$	–				–	100	–	kΩ	–
AF-Driver Output Resistance	$R_0(af)$	–				–	250	–	Ω	–
AF-Driver Voltage Gain	A_{af}	9			R_S = 50 Ω, C_1 = 0	–	30	–	dB	10

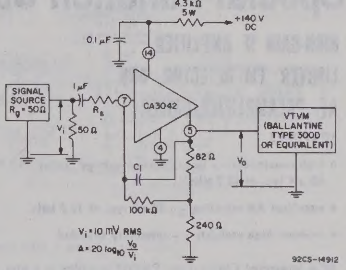


Fig.9 - Test setup for measurement of AF amplifier voltage gain.

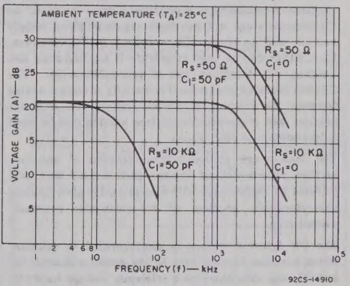
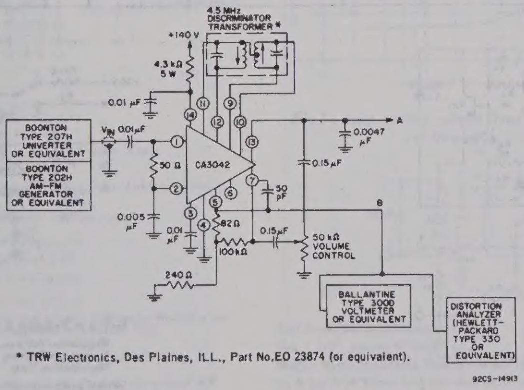


Fig.10 - Typical AF amplifier voltage gain characteristics.



* TRW Electronics, Des Plaines, ILL., Part No.EO 23874 (or equivalent).

Fig.11 - Test setup for measurement of input limiting voltage (knee), recovered AF voltage, and total harmonic distortion.

PROCEDURES:

Recovered AF Voltage:

1. Set Input Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1 kHz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 500 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (500mV - 3 dB = 350 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).

CA3043
Special-Function Subsystem

HIGH-GAIN IF AMPLIFIER, LIMITER, FM DETECTOR, AND AF PREAMPLIFIER/DRIVER

FEATURES

- high sensitivity - - input limiting voltage (knee) 50 µV typ. at 10.7 MHz
- excellent AM rejection - - 58 dB typ. at 10.7 MHz
- inherent high stability - - internally shielded

RCA Integrated Circuit Type CA3043 provides in a single monolithic silicon chip, a major sub-system for the IF sections of Communications and high-fidelity FM receivers. As shown in the Schematic Diagram (Fig.2) and the FM Receiver Block Diagram (Fig.1), the CA3043 contains a multistage if-amplifier/limiter section, an FM-detector stage, a Zener-diode regulated power-supply section, and an af-amplifier section. In FM receivers, the CA3043 can be used to provide if amplification and limiting, FM detection, and af preamplification. The CA3043 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The four stage emitter-follower-coupled if amplifier section provides 80-dB voltage gain at 10.7 MHz, and features an output stage with exceptionally good limiting characteristics because of its transistor constant-current sink.

The FM detector section is distinguished by circuitry which provides forward bias to the detector diodes, D2 and D3, and also provides a reference voltage for AFC.

The audio amplifier provides a low-impedance drive for subsequent audio amplifiers.

The power supply section provides zener-regulated, decoupled voltages for the IF amplifier, detector, and audio amplifier sections.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C

DISSIPATION:
At T_A = 25°C to T_A = 85°C . . . . .450 mW
Above T_A = 85°C . . . . . Derate linearly 5 mW/°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 min)
from case for 10 seconds max . . . . . . + 265°C

TEMPERATURE RANGE:
Operating . . . . -55°C to + 125°C
Storage . . . . -65°C to + 150°C

For FM IF Amplifier Applications in Communications Receivers and High-Fidelity FM Receivers up to 20 MHz

- internal Zener-diode regulated voltage supply
- low harmonic radiation
- wide frequency capability - - <100 kHz to >20 MHz
- low harmonic distortion
- hermetic 12-lead TO-5 style package

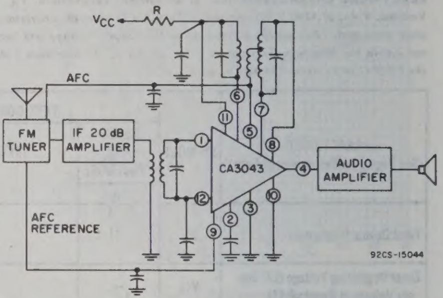


Fig.1 - Typical application of the CA3043 as a high-gain limiter, amplifier-detector in an FM receiver.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUIT AND PROCEDURE	LIMITS TYPE CA3043			UNITS
			Fig.	Min.	Typ.	Max.	
STATIC CHARACTERISTICS							
Current Drain at 6V into Pin No.11	I_{11}	V_{CC} = +6V	3	10	16	20	mA
Regulator Voltage Pin No.11	V_{11}	V_{CC} = +30V, R_S = 750 Ω	3	6.9	7.4	8	V
Total Device Dissipation	P_T		3	200	225	260	mW
Quiescent Operating Current into Pin No.6	I_6		3	-	0.65	-	mA
DYNAMIC CHARACTERISTICS at V_{CC} = +30V, R_S = 750 Ω, f = 10.7 MHz							
Voltage Gain	A_V		4	72	80	-	dB
Input Limiting Voltage (knee)	$v_i(lim)$	$v_o(af)$ at -3 dB point	6	-	50	-	µV (RMS)
Limiting Current from Pin No.6	$I_6(lim)$		4	-	0.42	-	mA (RMS)
Recovered AF Voltage	$v_o(af)$	v_i = 1 mV (RMS). f (modulating) = 1 kHz Deviation = ± 75 kHz	6	75	110	150	mV (RMS)
Amplitude-Modulation Rejection	AMR	v_i = 10 mV f (modulating) = 1 kHz % modulation = 50%	8	-	58	-	dB
Total Harmonic Distortion	THD	v_i = 1 mV (RMS)	6	-	0.3	-	%
Input Impedance Components:							
Parallel Input Resistance	R_I		-	-	7	-	kΩ
Parallel Input Capacitance	C_I		-	-	5	-	pF

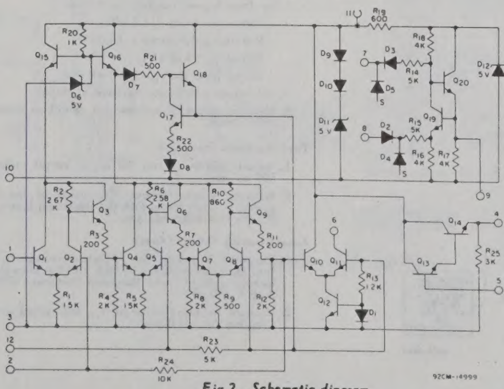


Fig.2 - Schematic diagram.

Notes:

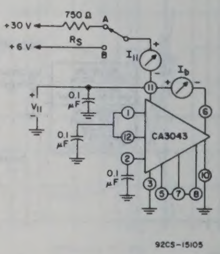
S = Substrate

Terminal No.3 wire-connected to the case.

Terminal No.10 connected to the case through the substrate

Terminals No.3 and 10 which are connected to the substrate should be connected to the most negative point in the circuit.

Diodes D_4 and D_5, act as capacitors and are used to balance the detector substrate capacitances.



Switch in Position A for:
Regulator-Voltage, Quiescent-Operating-Current, and Device Dissipation Test

Switch in Position B for Current into Pin No.11

Fig.3 - Regulator voltage, device dissipation, quiescent operating current, and current at 6 volts into Pin No. 11.

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range between horizontal terminal 5 and vertical terminal 3 is +6 to 0 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		+4 -4	0 -5	*	*	*	*	*	*	0 -5	*	Note(1)
2			0 -3	*	*	*	*	*	*	0 -3	*	*
3				+6 0	+6 0	+15 +2	+6 0	+6 0	+6 0	0	Note(2)	+3 0
4					+2 -4	*	*	*	*	0 -6	*	*
5						*	*	*	*	0 -6	+6 0	*
6							*	*	*	-2 -15	*	*
7								Note(1)	*	0 -6	*	*
8									*	0 -6	*	*
9										0 -6	*	*
10											Note(2) 0	+3 0
11												*
12												

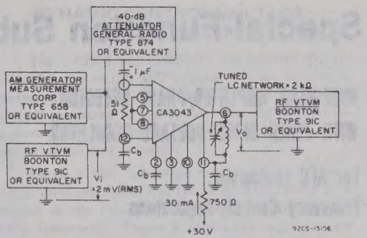
MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	-
2	-	-
3	0.1	40
4	-	20
5	-	-
6	-	-
7	-	-
8	-	-
9	-	20
10	0.1	40
11	40	0.1
12	-	-

Note 1: These terminals should be connected through a dc resistance to any terminal which does not exceed 100 ohms.

Note 2: Pin 11 may be connected to any positive voltage source through a suitable resistor provided its current rating is not exceeded.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.



40-dB ATTENUATOR GENERAL RADIO TYPE 874 OR EQUIVALENT
1 μF
AM GENERATOR MEASUREMENT CORP TYPE 658 OR EQUIVALENT
RF VTVM BOONTON TYPE 91C OR EQUIVALENT
51 Ω
CA3043
TUNED LC NETWORK = 2 kΩ
RF VTVM BOONTON TYPE 91C OR EQUIVALENT
Vo
Vi =2 mV(RMS)
Cb
30 mA
750 Ω
+30 V
92CS-15106

$$\text{Voltage Gain} = 20 \log_{10} 100 \frac{v_o}{v_i}$$

C_b - Bypass Capacitor, 0.1 μF electrolytic in parallel with 0.01 μF

$$I_6(\text{lim}) = \frac{v_o}{2K\Omega}, \quad v_i = 100\ \text{mV(RMS)}$$

* Output circuit should be completely shielded from the input circuit at the socket.

Fig.4 - Voltage gain test circuit.

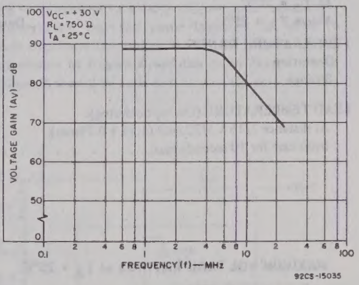
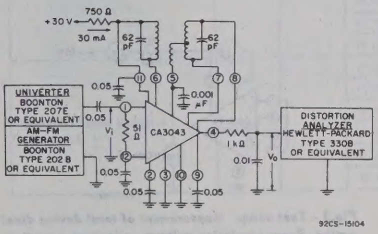


Fig.5 - Voltage gain vs frequency.



750 Ω
+30 V
30 mA
62 pF
62 pF
0.001 μF
UNIVERTER BOONTON TYPE 207E OR EQUIVALENT
AM-FM GENERATOR BOONTON TYPE 202 B OR EQUIVALENT
0.05
51 Ω
Vi
CA3043
1 kΩ
DISTORTION ANALYZER HEWLETT-PACKARD TYPE 330B OR EQUIVALENT
0.01
Vo
92CS-15104

PROCEDURE:

1. Recovered Audio Voltage $v_{o(af)}$ –

   Set input frequency to 10.7 MHz,

   v_i = 1 mV(RMS), modulating frequency = 1 kHz

   Deviation = ±75 kHz

   Record v_o as measured on the Distortion Analyzer meter scale.

   This is the recovered Audio Voltage $v_{o(af)}$

2. 3 dB Limiting Sensitivity $v_{i(lim)}$ –

   Reduce v_i until $v_{o(af)}$ drops 3 dB.

   Record this value of v_i as $v_{i(lim)}$

3. Total Harmonic Distortion THD –

   Reset v_i to 1 mV(RMS) and operate Distortion Analyzer per manufacturer's instructions to measure THD.

* See Fig.9 for details on Discriminator Transformer.

Fig.6 - Input limiting voltage (knee), recovered AF voltage, and total harmonic distortion test circuit.

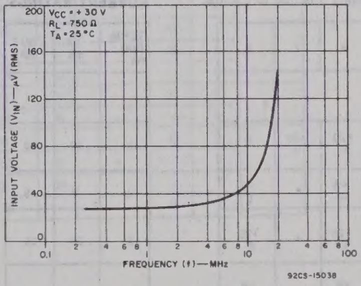
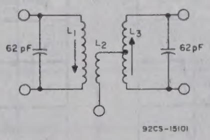


Fig.7 - Input limiting voltage (knee) at -3 dB point vs frequency.



Coil Form, Outside Diameter = 7/32"

Can = 1/2" square X 1-1/8" long

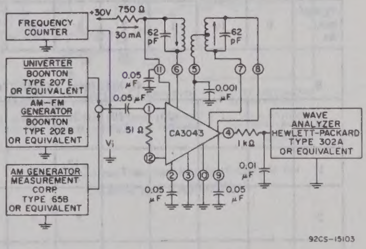
Slugs - Radio Industries Type MP34/MP100 Material

L_1 & L_3 = 20 Turns 5-44 litz wire universal wound

L_2 = 10 Turns 5-44 litz wire wound bifilar with L_1

L_1 & L_3 coupling adjusted to 520 kHz peak to peak separation on S curve when operated in circuit shown in Fig.6.

Fig.9 - 10.7-MHz discriminator transformer for CA3043.



FREQUENCY COUNTER
+30V
750 Ω
30 mA
62 pF
62 pF
UNIVERTER BOONTON TYPE 207E OR EQUIVALENT
AM-FM GENERATOR BOONTON TYPE 202 B OR EQUIVALENT
AM GENERATOR MEASUREMENT CORP TYPE 658 OR EQUIVALENT
0.05 μF
0.001 μF
51 Ω
Vi
CA3043
1 kΩ
WAVE ANALYZER HEWLETT-PACKARD TYPE 302A OR EQUIVALENT
0.01 μF
0.05 μF
92CS-15103

PROCEDURE:

A. Connect FM Generator to CA3043 input.

   Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz

   Deviation = ±75 kHz.

   Tune Wave Analyzer to peak reading at 1 kHz and record recovered Audio Voltage $v_{o(af)FM}$.

B. Disconnect FM Generator and Connect AM Generator to CA3043 input.

   Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz, percent modulation = 50%.

   Tune Wave Analyzer to peak reading and record recovered audio voltage $v_{o(af)AM}$

   $$\text{Amplitude Modulation Rejection Ratio} = 20 \log_{10} \frac{v_{o(af)FM}}{v_{o(af)AM}}$$

Fig.8 - Amplitude modulation rejection test circuit.

CA3044, CA3044V1

Special-Function Subsystem

WIDE-BAND AMPLIFIER/PHASE DETECTOR WITH ZENER DIODE VOLTAGE REGULATOR

For AFC (Automatic Frequency Control) Applications

The RCA CA3044 and CA3044V1 represent a second generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications.

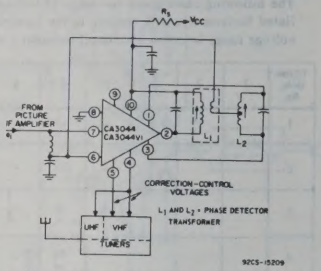
The CA3044V1 is electrically identical to the CA3044 but is supplied with formed leads for easier PC board design and construction.

FEATURES

- Primarily intended for AFC (automatic frequency control) Applications
- Internal Zener Diode Voltage Regulator
- Differential Input Amplifier/Limiter
- Full-Wave Diode Bridge Detector
- Differential Output Voltage Amplifier
- Available in Two Electrically Identical Versions of the 10-lead TO-5 style package,

  CA3044 With Straight Leads;

  CA3044V1 With Formed Leads
- Wide Operating Temperature Range; -55 to +125°C



R5
Vcc
FROM PICTURE IF AMPLIFIER
e1
9
10
8
7
6
1
2
3
5
4
CA3044
CA3044V1
L1
L2
CORRECTION-CONTROL VOLTAGES
L1 AND L2 - PHASE DETECTOR TRANSFORMER
UHF
VHF
TUNERS
92CS-15209

Fig.1 - Block diagram of Typical Automatic Fine Tuning (AFT) Application using CA3044 or CA3044V1 in Color-TV Receiver.

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION:

At $T_A = 25^oC$ . . . . 830 mW

Above $T_A = 25^oC$. . . . . Derate linearly 5.6 mW/°C

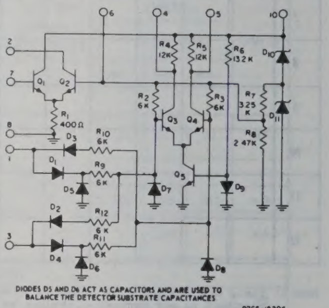
TEMPERATURE RANGE:

Operating . . . . -55°C to +125°C

Storage . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . + 265C



DIODES D5 AND D6 ACT AS CAPACITORS AND ARE USED TO BALANCE THE DETECTOR SUBSTRATE CAPACITANCES

92CS-15204

Fig.2 - Schematic diagram CA3044, CA3044V1

MAXIMUM VOLTAGE RATINGS at $T_A = 25^oC$

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 6 is +20 to 0 volts.

TERMINAL No.	9	10	1	2	3	4	5	6	7	8
9	NO INTERNAL CONNECTION									-
10			+20 0	+20 -10	+20 0	+20 0	+20 0	+20 0	+20 0	▲
1				*	+12 -12	*	*	+6 -6	*	+6 0
2					*	*	*	+20 0	*	+20 0
3						*	*	+6 -6	*	+6 0
4							*	*	*	+12 0
5								*	*	+12 0
6									+5 -5	+5 0
7										+8 -5
8										REF. SUBSTRATE

▲ Terminal No. 10 may be connected to any positive voltage source through a suitable dropping resistor—provided the dissipation rating is not exceeded.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9	-	-
10	50	50
1	5	5
2	20	20
3	5	5
4	5	5
5	5	5
6	5	5
7	5	5
8	50	50

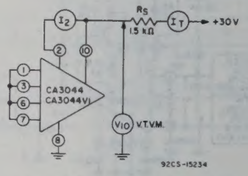


Fig.3 - Test setup: Measurement of total device dissipation, Zener regulating voltage, quiescent operating current (terminal 2).

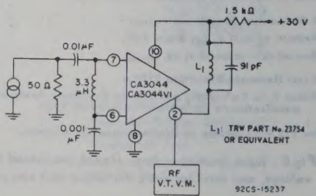


Fig.4 - Input limiting sensitivity test circuit.

CA3044, CA3044V1

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

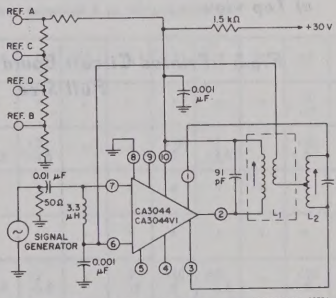
CHARACTERISTICS	SYMBOLS	TEST CIRCUITS	TEST CONDITIONS	LIMITS CA3044 and CA3044V1			UNITS	CHARAC-TERISTIC CURVES
		FIG.		MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS								
Device Dissipation	P_T	3	V_{CC} = 30 V R_S = 1.5 kΩ T_A = -55°C	90	120	150	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V R_S = 1.5 kΩ T_A = 25°C	110	140	170	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V R_S = 1.5 kΩ T_A = +125°C	130	160	190	mW	-
9-Volt Current Drain	I_T	3	V_{10} = 9 V	2.5	4	5.5	mA	-
Zener Regulating Voltage - DC Supply Voltage at Terminal 10	V_{10}	3	V_{CC} = 30 V R_S = 1.5 kΩ	10.5	11.2	11.9	V	-
Quiescent Operating Current into Terminal 2	I_2	3		1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4	V_4	-		5.0	6.5	8.0	V	-
Quiescent Operating Voltage at Terminal 5	V_5	-		5.0	6.5	8.0	V	-
Output Offset Voltage between Terminals 4 and 5	V_{4-5}	-		-1.5	0	1.5	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER)								
Input Limiting Voltage (Knee)	V_i Limiting	4	f=45.75 MHz	-	75	-	mV	-
Input Admittance	y_{11}	-	f = 45.75 MHz V_{CC} = 30 V R_S = 1.5 kΩ	-	0.5+j1.1	-	mmho	-
Reverse Transfer Admittance	y_{12}	-		-	3.8+j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-		-	-11.7 +10.1	-	mmho	-
Output Admittance	y_{22}	-		-	0.077+j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC								
Correction-Control Voltage at Terminal 4	V corr. (4)	5	V_{CC} = +30 V V_{in} = 200 mV RMS f_o = MHz as indicated	% of V_{10}		% of V_{10}		
			45.750 - 0.025	85	-	-	V	6,7
			45.750 + 0.025	-	-	33	V	
			45.750 - 0.900	75	-	-	V	7
			45.750 + 0.900	-	-	43	V	
			45.750 - 1.500	-	-	85	V	
			45.750 + 1.500	33	-	-	V	
Correction-Control Voltage at Terminal 5	V corr. (5)	5	45.750 - 0.025	-	-	33	V	6,7
			45.750 + 0.025	85	-	-	V	
			45.750 - 0.900	-	-	43	V	7
			45.750 + 0.900	75	-	-	V	
			45.750 - 1.500	33	-	-	V	
			45.750 + 1.500	-	-	85	V	

DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

The CA3044 and CA3044VI are specifically intended for use in the AFT system of color television receivers. Each device is tested so that the control voltages generated by the circuit meet the critical requirements of the system. Figure 5 is the schematic diagram of the test circuit.

Figure 6 and 7 show the control voltages generated at terminals 4 and 5 of the Integrated Circuit as a function of the frequency deviation from the nominal center frequency. Figure 6 shows the region within 25 KHz of the center frequency while Figure 7 covers the entire bandwidth of the system. The horizontal reference lines on the figures are generated by a voltage divider connected between the power supply voltage on Terminal 10 and ground. The dynamic control voltages are compared with these references according to the Output vs Frequency Deviation Table. For example: when the frequency deviation is -25 KHz the control voltage at Terminal 4 is greater than the reference A voltage; the control voltage at Terminal 5 is less than the reference B voltage.

The shape of the correction voltage characteristics is dependent to a large degree upon transformer characteristics and the parts layout. In order to closely duplicate the curves shown, the printed circuit board shown in Figure 8 and the parts layout shown in Figure 9 should be followed as closely as possible.



L_1 IS ALIGNED FOR SYMMETRICAL BANDWIDTH ON EITHER SIDE OF 45.750 MHz.

L_2 IS ALIGNED FOR ZERO DIFFERENTIAL OUTPUT BETWEEN TERMINALS 4 AND 5 AT f_o = 45.750 MHz.

L_1: TRW PART No. 23754 OR EQUIVALENT.

L_2: TRW PART No. 23755 OR EQUIVALENT.

92CS-15235

Fig.5 - Correction voltage test circuit for CA3044 and CA3044VI.

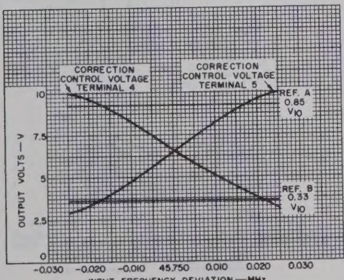


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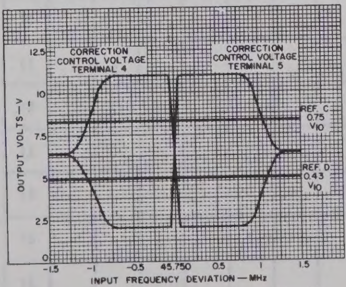
Fig.6 - Typical narrow-band dynamic control voltage characteristics.



92CS-15239

Fig.7 - Typical wide-band dynamic control voltage characteristics.

DEFINITIONS OF TERMS

Input Limiting Voltage (Knee) $[v_i(\text{lim})]$

The input signal voltage which will cause the output signal to decrease 3 dB from its maximum level.

Total Device Dissipation (P_T)

The total power drain of the device with no signal applied and no external load current.

Quiescent Operating Voltage

The dc voltage at the output terminal, with respect to ground, with no signal applied.

Quiescent Operating Current

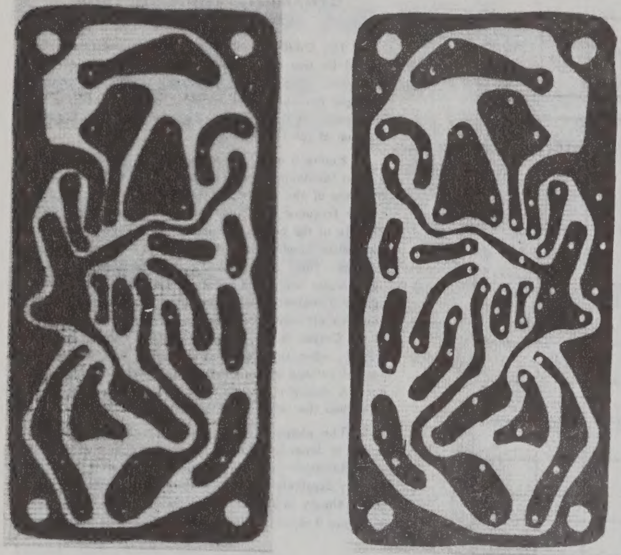
The average (dc) value of the current in either output, terminal, with no signal applied.

Output Offset Voltage

The dc voltage between output terminals with no signal applied.

Control Voltage

The dc voltage at either output terminal with respect to ground with an RF signal of specified frequency applied.



a) Top view b) Bottom view

Fig.8 - Printed Circuit Board for Test Circuit -- Full Size

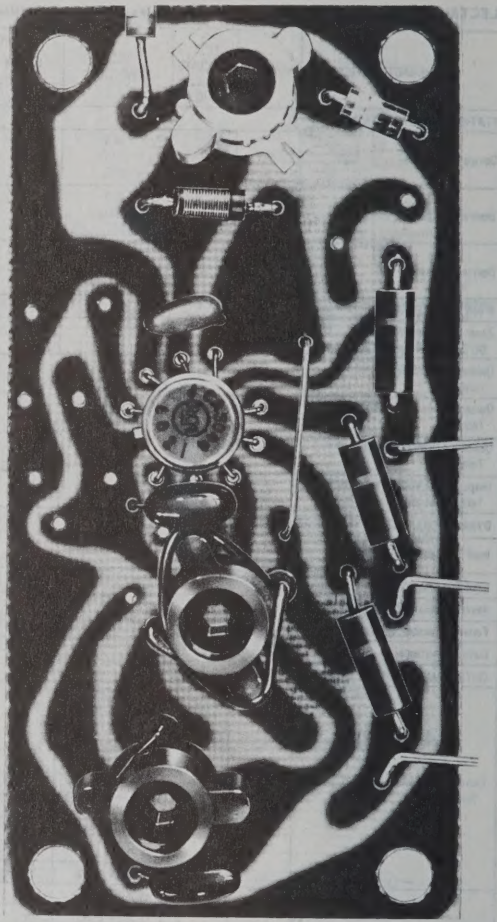


Fig.9 - Top view of wired test board.

Four Independent AC Amplifiers

Special-Function Sub-System for Stereo Preamplifiers, Magnetic Pickups, Tape Heads, etc.

FEATURES

- **Four AC amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Operates from single-ended supply**

EACH AMPLIFIER

High voltage gain	**53 dB min.**
High input resistance	**90 kΩ typ.**
Undistorted output voltage	**2 V rms min.**
Output Impedance	**1 kΩ typ.**
Open-loop bandwidth	**300 kHz typ.**

The RCA-CA3052 is a silicon monolithic integrated circuit designed specifically for stereo preamplifier service. The circuit consists of four independent ac amplifiers which can operate from a single-ended supply.

The CA3052 can operate as an equalizer amplifier in tape recorders, magnetic cartridge phonograph applications, and tone control amplifiers. It can provide all of the amplification necessary for a full-function stereo preamplifier.

The CA3052 is supplied in a 16-lead dual-in-line plastic package.

RCA-CA3052 is schematically identical with the CA3048 Amplifier Array (File No. 377). Each amplifier of the CA3048 is tightly specified for equivalent output noise under a variety of test methods. The CA3052 is specified using RIAA test methods for equivalent input noise using one test method for amplifiers 1 and 4, and an appropriately different method for amplifiers 2 and 3.

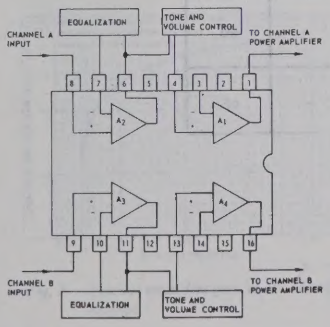


Fig. 1 – Block diagram of stereo preamplifier using CA3052.

APPLICATIONS

- **Full-function stereo preamplifiers**
- **Tape recorder and playback preamplifiers**
- **Tone Generators**

ABSOLUTE-MAXIMUM RATING at T_A = 25°C:

POWER SUPPLY VOLTAGE	+16 V
AC INPUT VOLTAGE	0.5 V rms
DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	Derate linearly at 7.7 mW/°C
TEMPERATURE RANGE:	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	+265°C

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	+2 -3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at T_A = 25° C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS CA3052 MIN.	TYP.	MAX.	UNITS
STATIC						
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12 V	9.5	13.5	17.5	mA
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12 V	6.1	6.9	8.1	V
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12 V	1.7	2.0	2.3	V
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12 V	2.2	2.5	2.8	V
DYNAMIC each amplifier with no AC feedback unless otherwise noted—terminals 3, 7, 10, & 14 bypassed to ground						
Open-Loop Gain	A_{OL}	V_{CC} = +12 V E_{IN} = 2 mV f = 10 kHz	53	58	–	dB
Open-Loop Output Voltage Swing	V_O(rms)	V_{CC} = +12 V f = 1 kHz THD = 5%	2.0	2.4	–	V
Open-Loop -3 dB Bandwidth	BW	V_{CC} = +12 V E_{IN} = 2 mV	–	300	–	kHz
Open-Loop Total Harmonic Distortion	THD	V_{CC} = +12 V, f = 1 kHz E_{OUT} = 2 V rms	–	0.65	–	%
Input Resistance	R_I	V_{CC} = +12 V, f = 1 kHz	–	90	–	kΩ
Input Capacitance	C_I	V_{CC} = +12 V, f = 1 MHz	–	9	–	pF
Output Resistance	R_O	V_{CC} = +12 V, f = 1 kHz	–	1	–	kΩ
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12 V f = 1 MHz	–	<0.1	–	pF
Equivalent Input Noise Voltage (Amplifiers 1 & 4), "C" Filter at Output*	E_{N1}‡	V_{CC} = +10 V R_S = 5 kΩ A = 45 dB	–	1.7	6.4	μV
Equivalent Input Noise Voltage (Amplifiers 2 & 3) RIAA Compensated*	E_{N2}‡	V_{CC} = +10 V R_S = 5 kΩ A = 64 dB (1 kHz)	–	4	15.0	μV
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12 V f = 1 kHz 0 dB = 0.78 V	–	<-45	–	dB
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12 V f = 1 MHz	–	< 0.02	–	pF

*Per IHF Standard Methods of Measurement for Audio Amplifiers IHF–A–201, 1966

‡ ac feedback included in test circuit

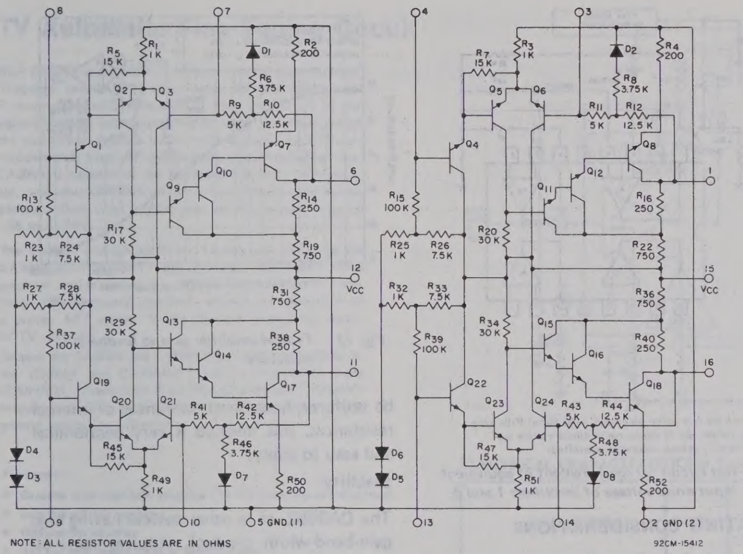


Fig. 2 — Schematic diagram for CA3052.

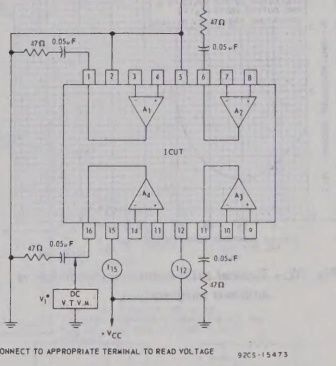
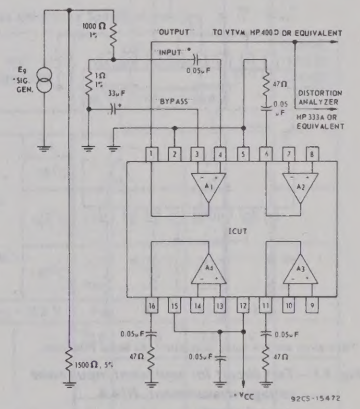


Fig. 3 — Test circuit for measurement of collector supply voltage and currents.


TO VTVM, HP400D OR EQUIVALENT
DISTORTION ANALYZER HP 333A OR EQUIVALENT
92CS-15472

* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make $E_S = 2mV$.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig. 6 — Test circuit for measurement of distortion, open-loop gain, and bandwidth characteristics.

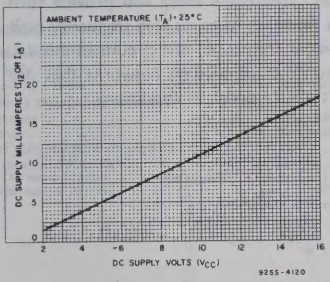


Fig. 4 — Typical DC supply current vs supply voltage.

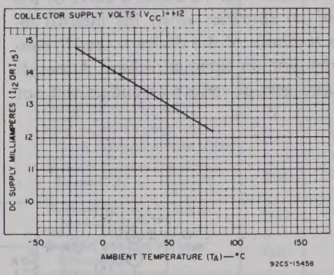


Fig. 5 — Typical DC supply current vs ambient temperature.

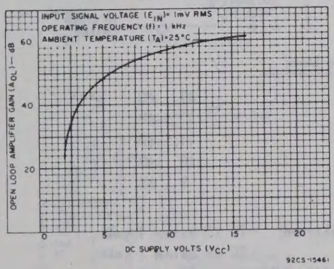


Fig. 7 — Typical amplifier gain vs DC supply voltage.

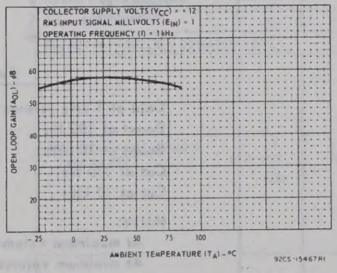


Fig. 8 — Typical open-loop gain vs ambient temperature.

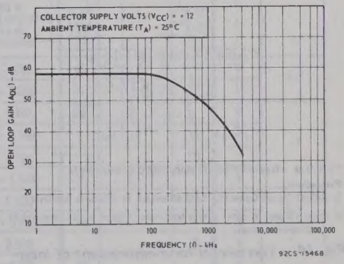


Fig. 9 — Typical open-loop gain vs frequency.

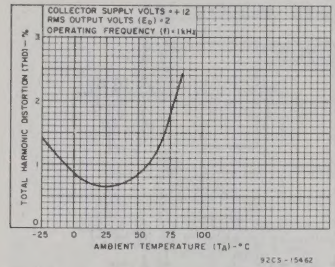
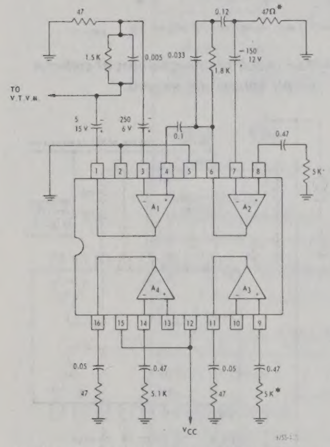
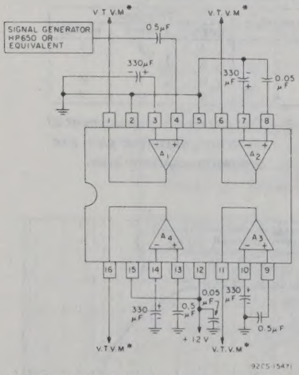


Fig. 10 – Typical total harmonic distortion vs ambient temperature.



*Resistors are low noise precision (1%) Metal Film type.

Fig. 13 – Test circuit for equivalent input noise voltage measurement, RIAA compensated.

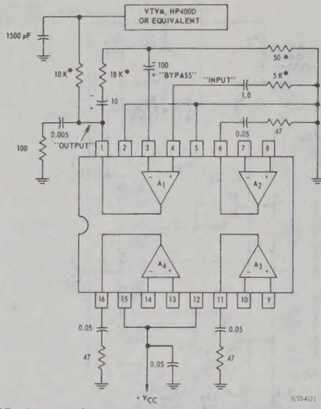


*V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig. 14 – Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.



*Resistors are low noise precision, (1%) Metal Film type. Resistor values are in ohms; capacitance values are in microfarads, unless otherwise specified.

Fig. 11 – Test circuit for measurement of equivalent input noise voltage of amplifiers 1 and 4.

OPERATING CONSIDERATIONS

Economical Gain Control

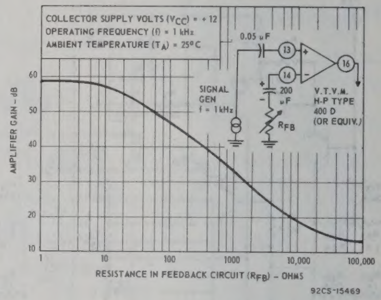


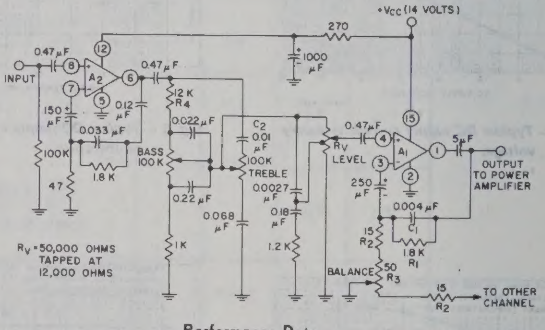
Fig. 12– Typical amplifier gain vs feedback resistance.

The CA3052 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig. 15 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3052, as in other devices having high gain-band-width product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3052 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.



Performance Data

Gain at 1-kHz reference	47 dB
Boost at 100 Hz	11.5 dB
Boost at 10 kHz	11.5 dB
Cut at 100 Hz	10 dB
Cut at 10 kHz	9 dB
Noise:	
At maximum volume (input shorted)	> 70 dB below 1 volt
At minimum volume	> 80 dB below 1 volt
Total harmonic distortion (at 1-kHz reference and an output of 1 volt)	< 0.3 per cent

92CM-29305

Fig. 15 – Schematic of one channel of a complete stereo preamplifier.

CA3064, CA3064E

TV Automatic Fine Tuning Circuit

RCA-CA3064 and CA3064E represent the third generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications. They provide all of the signal-processing components needed (with the exception of the tuned-phase-detector transformer) to derive the AFT correction signals from the output of the video-if amplifier. The CA3064 is supplied in the 10-formed-lead TO-5 style package, and the CA3064E in the 14-lead dual-in-line plastic package. Both types operate over the temperature range of −55 to +125°C.

The CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1 but embody a higher-gain input amplifier which provides a 20-dB improvement in sensitivity. The increased sensitivity extends the application of a proven AFT system to the low-level if-amplifier stages in TV receivers.

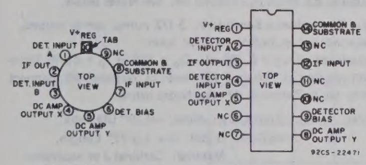
Because the CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1, refer to Application Note ICAN-5831, "Application of the RCA CA3044 and CA3044V1 Integrated Circuits in Automatic Fine-Tuning Systems" for general application information.

Features:

- **Cascode type high-gain amplifier (18 mV input for rated output)**
- **Internal voltage regulator**
- **Differential detector**
- **For use with either color or monochrome**
- **Differential amplifier**
- **Bipolar outputs**
- **Wide operating-temperature range; −55 to +125°C**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DEVICE DISSIPATION:
Up to T_A = 25°C . . . . 700 mW
Above T_A = 25°C . . . . derate linearly 5.6 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating . . . . −55 to +125°C
Storage . . . . −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32"
(1.59 mm ± 0.79 mm)
from case for 10 s max.. . . . . 265°C



(a) CA3064 *(b) CA3064E*

Fig.2 – Terminal assignment diagrams.

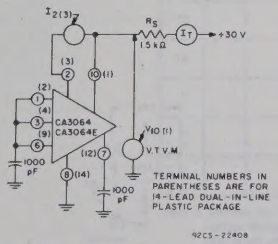


Fig. 3 – Test setup: Measurement of total device dissipation, zener regulating voltage, quiescent operating current at terminal 2 (3).

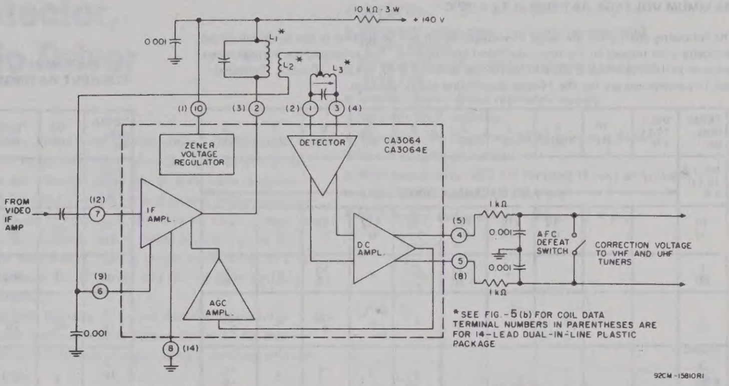


Fig.1 – Block diagram of typical operating circuit utilizing the CA3064 and CA3064E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS	TEST CONDITIONS		LIMITS CA3064, CA3064E			UNITS	CHARAC-TERISTIC CURVES
		FIG.			MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS									
Device Dissipation	P_D	3	V^+ = 30V R_S = 1.5kΩ	T_A −25°C	-	135	150	mW	-
				+25°C	130	140	150		-
				+85°C	-	145	150		-
Current Drain at 10.5 Volts	I_T	3	$V_{10(1)}$ = 10.5 V		4	6.5	9.5	mA	-
Zener Regulated Voltage – DC Supply Voltage at terminal 10(1)*	$V_{10(1)}$	3	↑ V^+ = 30 V R_S = 1.5 kΩ ↓		10.9	11.8	12.8	V	-
Quiescent Operating Current into Terminal 2(3)	$I_{2(3)}$	3			1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4(5)	$V_{4(5)}$	-			5	6.9	8	V	-
Quiescent Operating Voltage at Terminal 5(8)	$V_{5(8)}$	-			5	6.9	8	V	-
Output Offset Voltage between Terminals 4 and 5(5 and 8)	V_{4-5} (5-8)	-			-1	0	1	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER IN TO-5 STYLE PACKAGE)									
Input Voltage Sensitivity	V_I sensitivity	5	V^+ = +30 V V_I = 18 mV		Correction Voltage Output as shown in table below.				
Input Admittance	y_{11}	-	f = 45.75 MHz V^+ = 30 V R_S = 1.5 kΩ		-	0.41 + j1.0	-	mmho	-
Reverse Transfer Admittance	y_{12}	-			-	0 + j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-			-	24.5 - j29	-	mmho	-
Output Admittance	y_{22}	-			-	0.04 + j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC									
Correction-Control Voltage at Terminal 4(5)	V corr. 4(5)	5	V^+ = +30 V V_I = 18 mV RMS f_0 = MHz as indicated		% of V_{10} (1)		% of V_{10} (1)		
			45.750 - 0.030		85	-	-	V	6,7
			45.750 + 0.030		-	-	25	V	
			45.750 - 0.900		80	-	-	V	7
			45.750 + 0.900		-	-	35	V	
			45.750 - 1.500			-	80	V	
			45.750 + 1.500		35	-		V	
Correction-Control Voltage at Terminal 5(8)	V corr. 5(8)	5	45.750 - 0.030		-	-	25	V	6,7
			45.750 + 0.030		85	-	-	V	
			45.750 - 0.900		-	-	35	V	7
			45.750 + 0.900		80	-	-	V	
			45.750 - 1.500		35	-	-	V	
			45.750 + 1.500		-	-	80	V	

* Terminal numbers in parentheses are for 14-lead dual-in-line plastic package.

CA3064, CA3064E

MAXIMUM VOLTAGE RATINGS at $T_A = 25^oC$

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 (3) and horizontal terminal 6 (9) is +20 to 0 volts. Terminal nos. in parentheses are for the 14-lead dual-in-line plastic package.

TERMINAL No.	9(6,7, 10,11, 13)	10 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (8)	6 (9)	7 (12)	8 (14)
9(6,7,♠ 10,11, 13)	← NO INTERNAL CONNECTION →									
10 (1)			+12 0	+10 -10	+12 0	+12 0	+12 0	+10 0	+20 0	▲
1 (2)				*	+10 -10	*	*	+5 -5	*	+5 -6
2 (3)					*	*	*	+20 0	*	+20 0
3 (4)						*	*	+5 -6	*	+5 -6
4 (5)							*	*	*	+12 0
5 (8)								*	*	+12 0
6 (9)									+5 -2	+2 0
7 (12)										+2 -10
8 (14)										REF.SUBSTRATE & CASE■

MAXIMUM CURRENT RATINGS

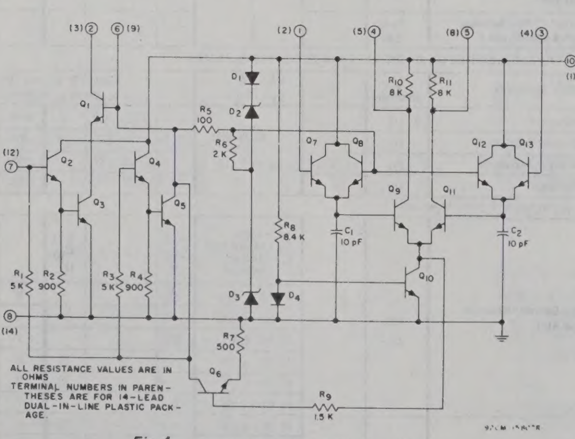
TERMINAL No.	I_{IN} mA	I_{OUT} mA
9(6,7, 10,11, 13)	-	-
10 (1)	50	50
1 (2)	1	0.1
2 (3)	20	20
3 (4)	1	0.1
4 (5)	5	5
5 (8)	5	5
6 (9)	5	5
7 (12)	1	1
8 (14)	50	50

▲ Terminal number 10 (1) may be connected to any positive voltage source greater than the internal zener regulating voltage through a suitable dropping resistor – provided the dissipation rating is not exceeded.

■ This terminal should be connected to the most negative potential of the complete circuit.

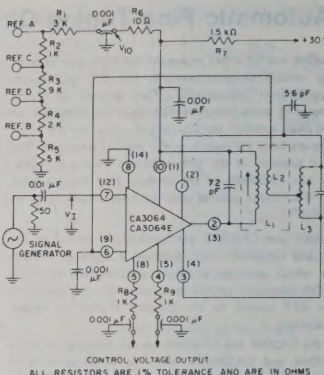
* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

♠ It is recommended that unused terminals 6,7,10,11, and 13 on the 14-lead dual-in-line-plastic package and terminal 9 on the TO-5 package be grounded to act as shields.



(3) ② ⑥ (9)
(2) ① (5) ④ (8) ⑤ (4) ③
⑩ (1)
(12) ⑦
⑧ (14)
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13
D1 D2 D3 D4
R5 100
R6 2 K
R10 8 K
R11 8 K
R8 8.4 K
C1 10 pF
C2 10 pF
R1 5 K R2 900
R3 5 K R4 900
R7 500
R9 1.5 K
ALL RESISTANCE VALUES ARE IN OHMS
TERMINAL NUMBERS IN PARENTHESES ARE FOR 14-LEAD DUAL-IN-LINE PLASTIC PACKAGE.

Fig.4 — Schematic diagram for CA3064 and CA3064E.



L_1 IS ALIGNED FOR SYMMETRICAL BANDWIDTH ON EITHER SIDE OF 45.750 MHz
L_2 TERTIARY WINDING WOUND ON L_1 COIL FORM
L_3 IS ALIGNED FOR ZERO DIFFERENTIAL OUTPUT BETWEEN TERMINALS 4 AND 5 AT f_o = 45.750 MHz
* FOR COIL CONSTRUCTION DATA, SEE FIG.4(b).

REFERENCE VOLTAGE PERCENTAGES	
Ref. A	85% of $V_{10(1)}$
Ref. B	25% of $V_{10(1)}$
Ref. C	80% of $V_{10(1)}$
Ref. D	35% of $V_{10(1)}$

Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

Fig.5 (a) – Correction voltage test circuit for CA3064 and CA3064E.

COIL DATA FOR DISCRIMINATOR WINDINGS

L_1 – Discriminator Primary: 3-1/6 turns; #20 Enamel-covered wire – close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz. Start winding at terminal #6; finish at Terminal #1. See Notes below.

L_2 – Tertiary Windings: 2-1/6 turns; #20 Enamel-covered wire – close wound over bottom end of L_1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 – Discriminator Secondary: 3-1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of L_3 = 0.180 μH; Q_o = 150 at f_o = 45.75 MHz. Start winding at Terminal #2; finish at Terminal #5; connect center tap to Terminal #7. See Notes below.

Notes:
1. Coil Forms; Cylindrical; –0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   : Material: Carbinal J or equivalent
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.

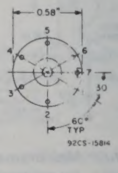


Fig.5 (b) Coil form base terminal diagram.

IF Amplifier-Limiter, FM Detector, Electronic Attenuator, Audio Driver

For Television Sound-System Applications

The RCA CA3065 Television Sound System is a monolithic integrated circuit which combines a multistage IF amplifier limiter, an FM detector, an electronic attenuator, a zener diode regulated power supply, and an audio amplifier-driver that is designed to directly drive an npn power transistor or high-transconductance tube. Because the circuit is so inclusive, a minimum number of external components is required. A block diagram of the integrated circuit television sound system is shown in Fig. 1.

The CA3065 with its advanced circuit design provides a high-performance multistage subsystem for the sound system of a television receiver. A particular feature of the CA3065 is the electronic attenuator which performs the conventional volume control function. Volume control is accomplished when the bias levels in the attenuator are changed by means of a variable resistor connected between Terminal 6 and ground (attenuation in excess of 60 dB is attained). Because no audio signal is present in this control, hum or noise pickup can be bypassed. In most cases, only a single unshielded wire is required between the IF board and the variable resistor (volume control).

The CA3065 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device into suitably punched printed-circuit boards.

FEATURES:

- Electronic attenuator - replaces conventional volume control
- Differential peak detector - requires one single tuned coil
- Internal Zener diode regulated supply
- Inherent high stability
- Excellent AM rejection - 50 dB typ. at 4.5 MHz
- Low harmonic distortion
- High sensitivity - 200 μV limiting (knee) at 4.5 MHz
- Audio drive capability - 6 mA p-p
- Undistorted audio output voltage - 7 V p-p

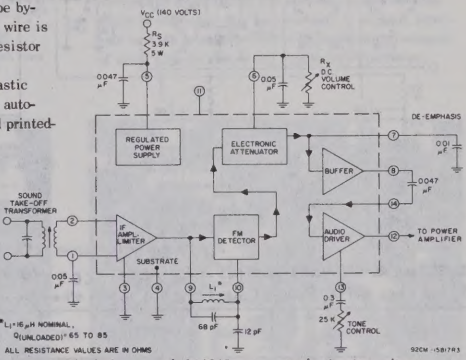


Fig. 1 - Block diagram of CA3065 in a typical circuit application.

MAXIMUM RATINGS, ***Absolute Maximum Values,*** **at T_A = 25° C**

Input Signal Voltage (between Terminals 1 and 2)	±3	V
Power Supply Current (Terminal 5)	50	mA
Power Dissipation:		
Up to T_A = 25°C	850	mW
Above T_A = 25°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	- 40 to + 85	°C
Storage	- 65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C

MAXIMUM VOLTAGE RATINGS at T_A = 25° C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 9 with respect to terminal 3 is 0 to +4 volts.

TERMINAL No.	4	5	6	7	8	9	10	11	12	13	14	1	2	3
4		SUBSTRATE CONNECTION – ALWAYS CONNECT TO TERMINAL 3												
5			+13 0	+13 0	+13 0	*	*	INTERNAL CONNECTION DO NOT USE	+13 0	+13 0	*	*	*	NOTE 1
6				*	*	*	*		*	*	*	*	*	+13 −5
7					+1 −4	*	*		*	*	*	*	*	+13 0
8						*	*		*	*	*	*	*	*
9							*		*	*	*	*	*	+4 0
10									*	*	*	*	*	+4 −5
11									INTERNAL CONNECTION DO NOT USE					
12										+4 −1	*	*	*	*
13											*	*	*	*
14												*	*	+3 −5
1													+5 −5	+5 −5
2														+4 −5
3														

Note 1: Terminal No. 5 may be connected to any positive voltage through a suitable resistor provided that the current and dissipation ratings of the CA3065 are not exceeded.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if specified limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
4	SUBSTRATE: CONNECT TO TERMINAL 3	
5	50	1
6	1	1
7	1	1
8	0.5	6
9	1	1
10	1	0.1
11	INT. CONN. DO NOT USE	
12	0.5	6
13	1	2
14	1	0.1
1	1	0.1
2	1	0.1
3	0.1	50

CA3065

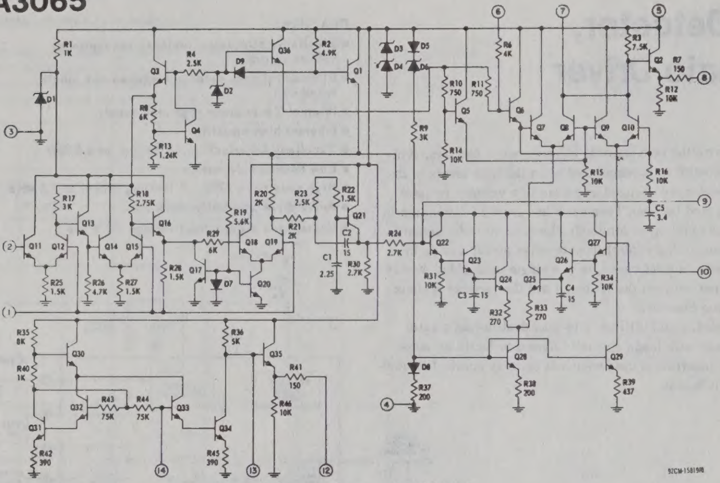


Fig. 2 - Schematic diagram of CA3065

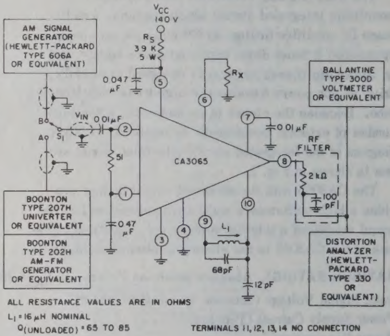
The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

ELECTRICAL CHARACTERISTICS *at T_A = 25° C, V_{CC} = +140 V applied to Terminal 5 through R_S = 3.9 kΩ, and DC Volume Control (R_x) = 0 unless otherwise indicated.*

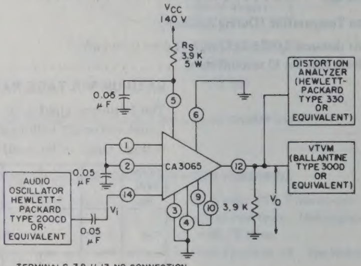
CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics						
Zener Regulating Voltage Terminal No. 5	V_5		10.3	11.2	12.2	V
Current into Terminal 5	I_5	Connect Terminal 5 to +9 V	10	16	24	mA
Total Device Dissipation	P_T		343	370	400	mW
Terminal Voltages: 1	V_1		–	2	–	V
6	V_6		–	4.8	–	V
7	V_7		–	6.1	–	V
9	V_9		–	3.7	–	V
12	V_{12}		4	5.1	5.8	V
Dynamic Characteristics						
IF AMPLIFIER Input Limiting Voltage (at −3 dB point)	$V_{i(lim)}$	f_0 = 4.5 MHz, f_m = 400 Hz, Deviation = ±25 kHz,	–	200	400	µV
AM Rejection	AMR	Amplitude Modulation = 30% f = 4.5 MHz	40	50	–	dB
Transconductance Magnitude	$\lvert G_m \rvert$(IF)	f = 4.5 MHz IF Input Terminals: 2, 1	–	500	–	mmho
Phase Angle	∠(IF)	IF Output Terminals: 9, 3	–	46	–	degrees
Feedback Capacitance	C_{fb}	f = 1 MHz; Terminals 2 and 9	–	· 0.02	–	pF
Input Impedance Components: Parallel Input Resistance	R_i(IF)	Measured between Terminal Nos. 1 and 2	–	17	–	kΩ
Parallel Input Capacitance	C_i(IF)	f = 4.5 MHz	–	4	–	pF
Output Impedance Components: Parallel Output Resistance	R_0(IF)	Measured between Terminal No. 9 and gnd	–	3.25	–	kΩ
Parallel Output Capacitance	C_0(IF)	f = 4.5 MHz	–	7.5	–	pF
DETECTOR Recovered AF Voltage	V_0(af)	f = 4.5 MHz; V_i = 100 mV Δf = ±25 kHz	0.5	0.75	–	V(rms)
Total Harmonic Distortion	THD	fm = 400 Hz	–	0.9	2	%
Output Resistance: Terminal 7	R_0		–	7.5	–	kΩ
Terminal 8			–	· 300	–	Ω
ATTENUATOR Max. Attenuation	–	See Fig. 7 R_X = ∞	60	80	–	dB
Max. "Play-through" Voltage*	–	R_X = ∞	–	0.075	1	mV
AUDIO AMPLIFIER Voltage Gain	A(af)	V_i = 0.1 V(rms), f = 400 Hz	17.5	20	–	dB
Total Harmonic Distortion	THD	V_O = 2 V(rms), f = 400 Hz	–	1.5	–	%
Undistorted Output Voltage	–	THD = 5%, f = 400 Hz	2	2.5	–	V(rms)
Input Resistance	R_i(af)	f = 400 Hz	–	70	–	kΩ
Output Resistance	R_0(af)	f = 400 Hz	–	270	–	Ω

*"Playthrough" voltage is the unwanted signal, measured at Terminal 8, when the volume control is set for minimum output.


AM SIGNAL GENERATOR (HEWLETT-PACKARD TYPE 606A OR EQUIVALENT)
V_{CC} 140 V
R_S 3.9 K 5 W
0.047 µF
5
R_X
6
BALLANTINE TYPE 300D VOLTMETER OR EQUIVALENT
B
A
S_1
V_{IN}
0.01 µF
2
7
0.01 µF
RF FILTER
51
CA3065
8
2 kΩ
100 pF
1
10
BOONTON TYPE 207H UNIVERTER OR EQUIVALENT
0.47 µF
9
L_1
3
4
DISTORTION ANALYZER (HEWLETT-PACKARD TYPE 330 OR EQUIVALENT)
BOONTON TYPE 202H AM-FM GENERATOR OR EQUIVALENT
68pF
12 pF
92CM-15815

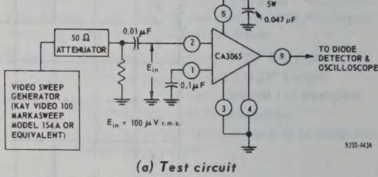
ALL RESISTANCE VALUES ARE IN OHMS
L_1 = 16 µH NOMINAL
$Q_{(UNLOADED)}$ = 65 TO 85
TERMINALS 11, 12, 13, 14 NO CONNECTION

Fig. 3 - Input limiting voltage, AM rejection, recovered audio, total harmonic distortion, maximum attenuation, maximum "play-through" test circuit.

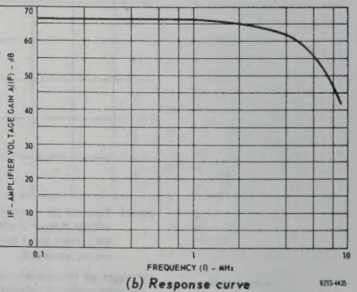

V_{CC} 140 V
R_S 3.9 K 5 W
0.05 µF
5
6
DISTORTION ANALYZER (HEWLETT-PACKARD TYPE 330 OR EQUIVALENT)
1
2
CA3065
12
VTVM (BALLANTINE TYPE 300D OR EQUIVALENT)
0.05 µF
AUDIO OSCILLATOR HEWLETT-PACKARD TYPE 200CD OR EQUIVALENT
14
V_i
9
10
3.9 K
V_O
3
4
0.05 µF
92CS-15816

TERMINALS 7,8,11,13 NO CONNECTION
ALL RESISTANCE VALUES ARE IN OHMS

Fig. 4 - Audio voltage gain (undistorted output) test circuit.

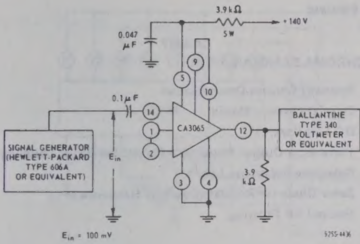

3.9 kΩ
5W
+140 V
5
0.047 µF
50 Ω ATTENUATOR
0.01 µF
2
CA3065
9
TO DIODE DETECTOR & OSCILLOSCOPE
E_{in}
1
0.1 µF
VIDEO SWEEP GENERATOR (KAY VIDEO 100 MARKASWEEP MODEL 154A OR EQUIVALENT)
3
4
E_{in} = 100 µV r.m.s.
92SS-4434

(a) Test circuit

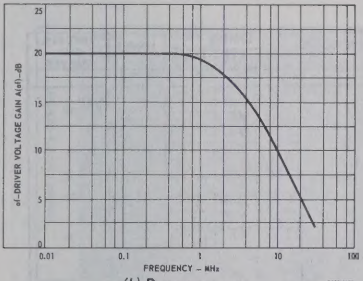


(b) Response curve

Fig. 5 - Frequency response of IF-amplifier section of CA3065


3.9 kΩ
5 W
+140 V
0.047 μF
0.1 μF
5
9
10
14
1
2
3
4
12
CA3065
SIGNAL GENERATOR (HEWLETT-PACKARD TYPE 606A OR EQUIVALENT)
E_{in}
BALLANTINE TYPE 340 VOLTMETER OR EQUIVALENT
3.9 kΩ
E_{in} = 100 mV
92SS-4436

(a) Test circuit



(b) Response curve

Fig. 6 - Frequency response of af-amplifier section of CA3065

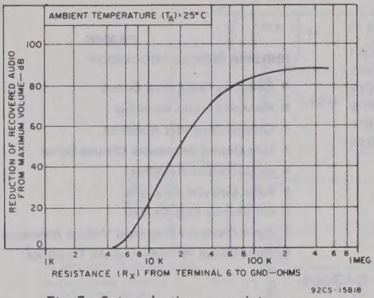


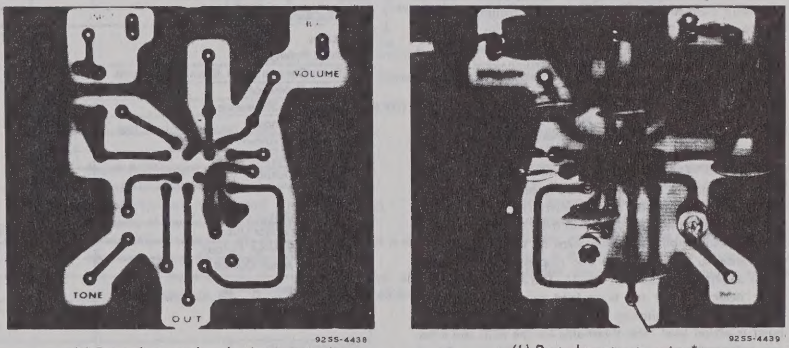
Fig. 7 - Gain reduction vs. resistance (terminal 6 to gnd)

OPERATING CONSIDERATIONS

The CA3065 may be used to drive a video output transistor or a high-transconductance output tube.

As in all TV receivers, precaution should be taken to prevent destruction of the CA3065 in the event of cascade arcs originating in the picture tube or in the output tube. In the case of arcing in the output tube a resistor of 150k in series with terminal No. 12 and the grid of the tube is usually sufficient protection.

To prevent damage from picture tube arcs, a careful analysis of board layout and coupling modes (electrostatic or magnetic) may be necessary to suggest alternate layouts or appropriate locations for the placement of spark gaps to absorb the high energy discharge.



*(a) Printed circuit board – bottom view**

*(b) Parts layout – top view**

Fig. 8 - Recommended parts layout for TV receiver sound strip using CA3065.

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* A 200 mil square grid was used in the layout of passive components on the printed circuit board. The Quad-in-line formed leads conform to a standard grid spacing of 100 mil centers.

CA3066, CA3067

Television Chroma System

The RCA CA3066 and CA3067 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3066 provides subcarrier regeneration and total chroma signal processing prior to demodulation; the CA3067 performs the demodulation and tint control functions. Each device utilizes a 16-lead quad-in-line plastic package.

CA3066 CHROMA SIGNAL PROCESSOR

The CA3066 contains substantially all the color processing circuitry exclusive of the tint control and demodulating circuits. The chroma amplifier sections of the CA3066 consist of the chroma and bandpass amplifiers. The chroma amplifier receives the chroma input signal at terminal No. 1. This amplifier is gain controlled by the automatic chroma control (ACC) detector-amplifier. The chroma signal is internally coupled from the output of the chroma amplifier to the input of the chroma bandpass amplifier and burst separator amplifier. The horizontal keying pulse (+8V) is used to gate the burst portion of the chroma signal from the input of the bandpass amplifier to the input of the burst separator amplifier. The bandpass amplifier is gain controlled by the dc chroma gain control and can also be controlled by the killer detector-amplifier. The bandpass amplifier output is internally coupled to the chroma output amplifier stage of the CA3066. The coils of the chroma amplifier and the bandpass amplifier are stagger-tuned to provide a combined typical bandpass of 3.08 to 4.08 MHz. The burst separator amplifier injects the burst signal into the 3.58 MHz oscillator. The oscillator amplitude is dependent on the terminal No. 9 impedance to ground and is also responsive to the burst signal amplitude at terminal No. 11. The ACC detector and killer detector sense the burst level or absence of burst, respectively, by monitoring the oscillators response to the burst injection level. The thresholds for the ACC and killer are independently adjusted by resistors R2 and R1 at terminals No. 9 and No. 4, respectively. The chroma output is at terminal No. 14 and the oscillator output is at terminal No. 8. Terminal No. 6 is a zener diode for use as a regulated voltage reference at 11.9 volts. When the zener reference element is not used, the power supply voltage should be maintained at 11.2 ± 0.5 volts.

System Features

CA3066
CHROMA SIGNAL PROCESSOR

- **Complete Color Sync Circuit**
- **Blanked Chroma Amplifier**
- **Chroma Band-Pass Amplifier**
- **Low Output Impedance Chroma Driver**
- **ACC Detector-Amplifier**
- **Killer Detector-Amplifier**
- **DC Chroma Gain Control**
- **Zener Diode for Regulated Voltage Reference**
- **Short-Circuit Protection on All Terminals**

CA3067
CHROMA DEMODULATOR

- **Balanced Chroma Demodulators**
- **Color Difference Matrix**
- **DC Tint Control**
- **Three Low Output Impedance Drivers for Direct Coupling**
- **Reference Subcarrier Limiter**
- **Zener Diode for Regulated Voltage Reference**
- **Internal RF Filtering**

CA3066

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$ and $V^+ = 11.2$ V

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	TEST FIG. AND CURVES
			MIN.	TYP.	MAX.		
Static Characteristics							
Voltages:							
ACC Reference	V_2		–	0.5	–	V	2
Burst-Chroma Ampl. Bias Current Term.	V_3		–	2.9	–		
Killer Reference	V_4		–	1.0	–		
Zener Reg. Reference	V_6		10.6	11.9	12.6		
Oscillator Input	V_7		–	1.4	–		
Oscillator Output	V_8		–	2.35	–		
Balance (ACC Control)	V_9		–	1.65	–		
Chroma Output	V_{14}		–	4.6	–		
Currents:							
Total Supply	I_5		14	24	33	mA	
Burst Separator Output	I_{11}	S_1 Closed	–	6.5	–		
Band-Pass Ampl. Output	I_{13}		–	4.8	–		
Chroma Ampl. Output	I_{16}		–	1.27	–		
Dynamic Characteristics							
Oscillator Output	v_8	$v_1 = 0\ v_{p\text{-}p}$ $v_1 = 1.25\ v_{p\text{-}p}$	0.8 –	1.2 2.5	– 3.5	$v_{p\text{-}p}$	4
Chroma Output:							
100%	v_{14}	$v_1 = 1.25\ v_{p\text{-}p}$	0.5	1.0	–	$v_{p\text{-}p}$	3, 4
Killed		$v_1 = 0.025\ v_{p\text{-}p}$	–	–	12		
ACC Detector Output	v_2	$v_1 = 1.25\ v_{p\text{-}p}$	–	0.9	–	V	4
Small-Signal Input Resistance (Term. No.1)	r_i		–	50	–	kΩ	–
Small-Signal Input Capacitance (Term. No.1)	c_i		–	2.4	–	pF	
Small-Signal Output Impedance (Term. No.14)	r_o		–	250	–	Ω	

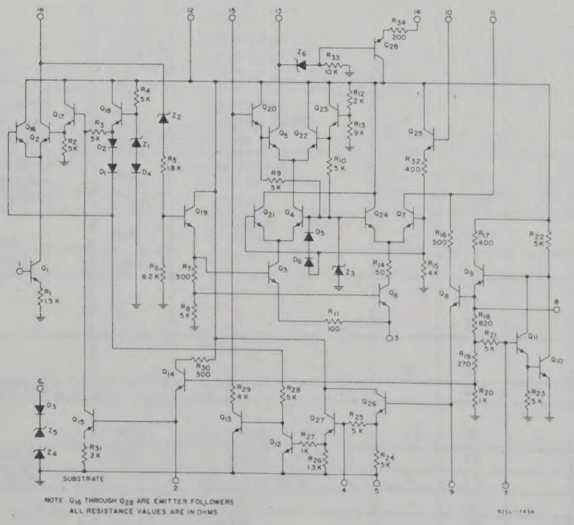


Fig. 1 - CA3066 schematic diagram.

CA3066

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

Supply Voltages and Currents (see charts below)
Device Dissipation:
Up to $T_A = 70^oC$ . . . . 600 mW
Above $T_A = 70^oC$ . . . . derate linearly 7.7 mW/^oC
Ambient Temperature Range:
Operating . . . . −40 to +85 ^oC
Storage . . . . −65 to +150 ^oC
Lead Temperature (During soldering for 10s max. at not less than 1/32″ from package) . . . +265 ^oC

Voltage with respect to Terminal No. 5.

Terminal No.	$V_{min.}$ (volts)	$V_{max.}$ (volts)
6	See Note N1	
7	–	–
8	–	–
9	–	–
10	−5.0	N2
11	0.0	18.0
12	0.0	12.0
13	0.0	15.0
14	–	–
15	0.0	N2
16	0.0	15.0
1	−5.0	5.0
2	–	–
3	–	–
4	–	–

Current

Terminal No.	I_I mA	I_o mA
6	20	0.1
7	5	0.1
8	1	2
9	0.1	2
10	1	0.1
11	10	1
12	50	1
13	10	1
14	0.1	6
15	3	1
16	6	1
1	1	0.1
2	0.1	2
3	0.1	20
4	1	1

N1 Terminal No. 6 is connected to a zener reference element, that, if used, should be biased by a positive voltage through a resistor that limits the current to a value which is less than the maximum current rating of terminal No. 6.

N2 The upper voltage limit cannot exceed the power supply input voltage at terminal 12.

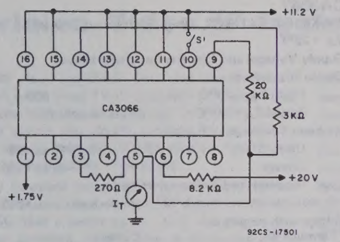


Fig. 2 - Static characteristics test circuit for CA3066.

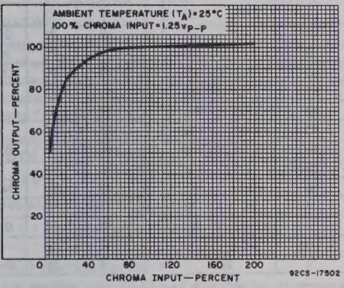


Fig. 3 - Typical ACC characteristic of chroma output vs chroma input for CA3066.

CA3067 CHROMA DEMODULATOR

The CA3067 contains the separate functional systems of a dc tint control and a demodulator. The phase shift of the tint amplifier system is accomplished by functional control of the fixed phase signal from the CA3066 oscillator output. This regenerated reference subcarrier is applied to terminal No. 3 and driven differentially into phase shift circuits. The tint adjustment controls the vector addition of phase shifted signals after which a limiting amplifier removes any remaining amplitude modulation. The output of the tint amplifier at terminal No. 1 is phase separated for the required reference subcarrier phase at terminal No. 6 and No. 12 (terminal No. 12 lags terminal No. 6 by approximately 76°). These terminals are inputs to the demodulator drive amplifiers. The demodulators consist of two sets of balanced detectors which receive their reference subcarrier from the demodulator drive amplifiers. The chroma signal input from the CA3066 is applied to terminal No. 14. The chroma signal differentially drives the demodulators. The demodulation components are matrixed and dc-shifted in voltage to give R–Y, G–Y, and B–Y color difference components with close dc balance and proper amplitude ratios. The output amplifiers of the CA3067 are specially designed to meet the low-impedance driving source requirements of the high-level color output amplifiers. A special feature of the CA3067 is R–C filtering of high frequency demodulation components. Terminal No. 4 is a zener diode for use as a regulated voltage reference at 11.9V. When the zener reference element is not used, the power supply should be maintained at +11.2 ±0.5 volts.

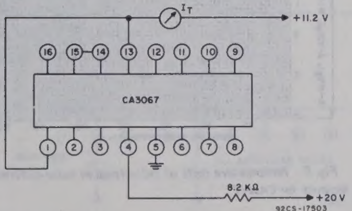
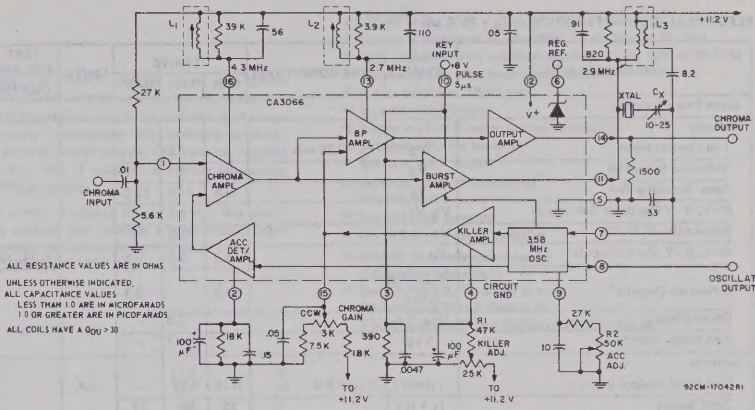


Fig. 5 - Static characteristics test circuit for CA3067.



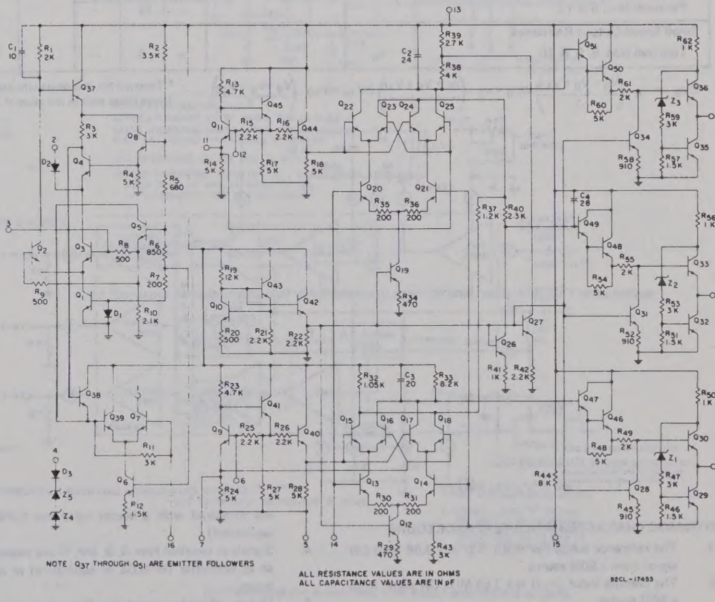
ALL RESISTANCE VALUES ARE IN OHMS
UNLESS OTHERWISE INDICATED,
ALL CAPACITANCE VALUES
LESS THAN 1.0 ARE IN MICROFARADS
1.0 OR GREATER ARE IN PICOFARADS
ALL COILS HAVE A $Q_{OU} > 30$

Fig. 4 - Dynamic characteristics test circuit for CA3066.

DYNAMIC CHARACTERISTICS TEST PROCEDURE

Steps 1, 2, and 3 are performed with no Chroma input ($v_1 = 0$)

1. Adjust ACC potentiometer for $V_2 = +0.65V$.
2. Adjust Killer potentiometer for $V_4 = +1.2V$.
3. Adjust capacitor C_x (crystal trimmer) so that frequency of oscillator is 3.579545 MHz.
4. Unless otherwise noted, the chroma gain control is at maximum gain (fully clockwise).
5. The chroma input test signal is a 52.5 μs "line" at subcarrier frequency, and 10 cycles of burst at 46.5% of the "line" amplitude. The chroma input (v_1) is in peak-to-peak volts of "line" amplitude.
6. The chroma output (v_{14}) is the same as the chroma input (v_1) except that the burst is removed and keying overshoot occurs in the retrace period. The chroma output is in peak-to-peak volts of "line" amplitude.
7. The oscillator output (v_8) is the CW output at terminal No. 8 and is in peak-to-peak volts. Some modulation of oscillation dampening between burst injection is visible.



NOTE Q_{37} THROUGH Q_{51} ARE EMITTER FOLLOWERS

ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN pF

Fig. 6 - CA3067 schematic diagram.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$ and $V^+ = 11.2$ V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST FIG. AND CURVES
Static Characteristics							
Voltages:							
Tint Control Input	V_2	$I_2 = 0.25$ mA	–	3.5	–	V	9
Reference Subcarrier	V_3		–	2.1	–		
Zener Regulator Ref.	V_4		10.6	11.9	12·6		
B–Y, R–Y Oscillator Ref. Inputs	V_6, V_{12}		–	5.7	–		
Balance (B–Y, R–Y)	V_7, V_{11}		–	5.0	–		
B–Y, G–Y, R–Y Outputs	$V_{8, 9, 10}$		4.2	5.0	5.8		9, 11, 12
Difference Outputs*	$\Delta V_8, \Delta V_9, \Delta V_{10}$		–0.3	–	0.3		9
Chroma Inputs	V_{14}, V_{15}		–	3.0	–		
Tint Ampl. Balance	V_{16}		–	4.7	–		
Currents:							
Tint Ampl. Output (min.)	I_1(min.)	$V_{16} = 8$ V	0.16	0.37	–	mA	
Total Supply	$I_1 + I_{13}$		15	24	33		
Dynamic Characteristics							
Tint Amplifier Output							10
Sensitivity	V_1	$V_3 = 7$ mV (RMS)	160	250	–	mV (RMS)	
Limiting Knee		$V_3 = 35$mV (RMS)	–	300	–		
Limiting		$V_3 = 350$mV (RMS)	–	–	380		
Tint Ampl. Phase Ref.▲	ϕ_6	$V_3 = 70$mV (RMS)	185	220	235	deg.	
Tint Ampl. Phase Shift‡	$\Delta\phi_6$	$V_3 = 70$mV (RMS)	90	105	–	deg.	
Demodulated Chroma Output:							
R–Y	V_{10}	$V_3 = 70$mV (RMS) $V_{14} = 35$mV (RMS)	150	250	–	V(RMS)	
Ratio of G–Y to R–Y	V_9/V_{10}		0.28	0.36	0.44		
Ratio of B–Y to R–Y	V_8/V_{10}		1.0	1.2	1.4		
Color Difference Output BW at 3.3 dB	$BW_{Diff.}$		450	550	–	kHz	
Color Difference Outputs (max. input signals):							
R–Y	v_{10}	$V_3 = 70$mV (RMS) $V_{14} = 212$mV (RMS)	–	3.0	–	$v_{p\text{-}p}$	
G–Y	v_9		–	1.1	–		
B–Y	v_8		–	3.6	–		
Small Signal Input Resistance							
Terminal No. 3	r_i		–	550	–	Ω	
Terminal Nos. 6 & 12			–	22	–		
Small Signal Output Resistance							
Terminal Nos. 8, 9, & 10	r_o		–	5	–		

$$^*\Delta V_8 = V_8 - \left(\frac{V_8 + V_9 + V_{10}}{3}\right), \Delta V_9 = V_9 - \left(\frac{V_8 + V_9 + V_{10}}{3}\right), \Delta V_{10} = V_{10} - \left(\frac{V_8 + V_9 + V_{10}}{3}\right)$$

▲ Terminal No. 3 is phase reference

‡ read phase shift as tint control is varied

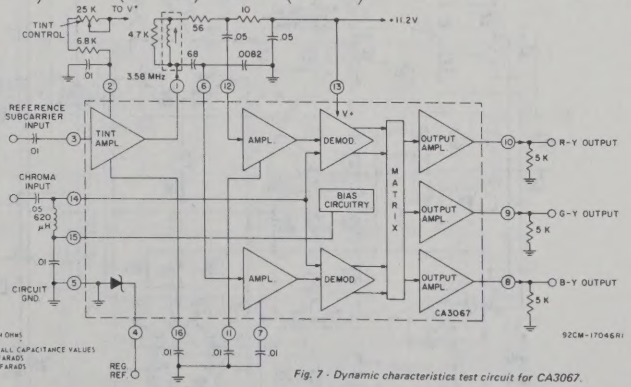


Fig. 7 - Dynamic characteristics test circuit for CA3067.

DYNAMIC CHARACTERISTICS TEST PROCEDURE

1. The reference subcarrier input (v_3) is a 3.58 MHz CW signal from a 50Ω source.
2. The chroma input (v_{14}) is a 3.53 MHz CW signal from a 50Ω source.
3. Phase and amplitude at terminal Nos. 1, 3, 6 and 12 are measured with a vector voltmeter (HP8405A or equivalent).
4. Signals at terminal Nos. 8, 9, and 10 are measured with an ac voltmeter (HP400E or equivalent) or an oscilloscope.
5. Unless otherwise noted the Tint control is at maximum resistance.

CA3067

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

Supply Voltages and Currents (see charts below)

Device Dissipation:

Up to $T_A = 70^oC$ . . . . 600 mW

Above $T_A = 70^oC$ . . . . derate linearly 7.7 mW/^oC

Ambient Temperature Range:

Operating . . . . –40 to +85 ^oC

Storage . . . . –65 to +150 ^oC

Lead Temperature (During soldering for 10s max. at not less than 1/32" from package) . . . +265 ^oC

Voltage with respect to Terminal No. 5

Terminal No.	$V_{min.}$ (volts)	$V_{max.}$ (volts)
6	0	N2
7	0	N2
8	0	N2
9	0	N2
10	0	N2
11	0	N2
12	0	N2
13	0	12
14	–3	N2
15	0	N2
16	N3	N3
1	0	15
2	0	N2
3	0	5
4	N1	

Current

Terminal No.	I_i (mA)	I_o (mA)
6	3	3
7	3	3
8	20	20
9	20	20
10	20	20
11	3	3
12	3	3
13	50	1
14	1	0.1
15	6	2
16	N3	N3
1	3	3
2	3	0.1
3	3	3
4	20	0.1

N1 Terminal No. 4 is connected to a zener reference element, that, if used, should be biased by a positive voltage through a resistor that limits the current to a value which is less than the maximum current rating of terminal No. 4.

N2 The upper voltage limit cannot exceed the power supply input voltage at terminal 13.

N3 Terminal No. 16 should be bypassed for normal operation.

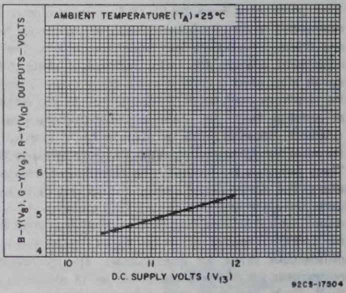


Fig. 8 - DC voltage at color-difference outputs vs supply voltage for CA3067.

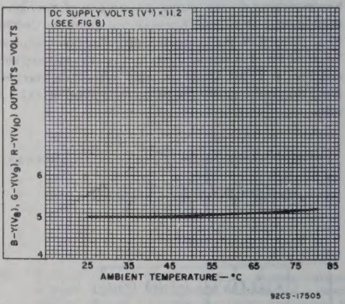


Fig. 9 - Temperature drift of DC voltage at color-difference outputs for CA3067.

Television Video IF System

RCA-CA3068 is a monolithic integrated circuit that incorporates an entire video TV-IF subsystem on a single chip. Innovations in integrated circuit design, in addition to the many active devices and closely matched components utilized in the circuit, make the CA3068 ideally suited for use in color and black-and-white TV receivers.

The primary functions performed by the IF subsystem are video IF amplification, linear detection, video output amplification, AGC from a keyed supply, AGC delay for tuner, sound carrier detection, sound carrier amplification, and a buffered AFT output. The advanced circuit design of the CA3068 also includes secondary functions for improved noise immunity and minimal airplane flutter. An isolated zener reference diode, incorporated in the IC, provides a convenient and economical means for controlling the regulated voltage supply. The inherent wide bandwidth capability (10-70 MHz) and high overall gain (87 dB) make the CA3068 suitable for other AM IF applications whose frequencies range within this bandwidth.

The CA3068 utilizes a unique 20-lead quad-in-line plastic package. This package also includes a wrap-around shield that serves to minimize interlead capacitances.

FEATURES:

- High-gain wide-band IF amplifier: 75 dB typ. at 45 MHz
- Gain reduction with excellent stability: 50 dB typ. at 45 MHz
- Video detector with linear characteristics
- Video amplifier: 12 dB gain
- Impulse noise limiter
- Keyed AGC with noise immunity circuits
- Delayed AGC for tuner
- Buffered AFT output
- Separate sound IF intercarrier amplification
- Sound carrier detector
- 4.5 MHz sound carrier amplifier
- Isolated zener reference diode for regulated voltage supply
- See ICAN-6303, "A Single IC for the Complete PIX-IF System in TV Receivers" for Schematic Diagram

MAXIMUM RATINGS, *Absolute Maximum Values, at $T_A = 25^\circ C$*

DC Supply Voltage:		
Between Terminals 15 and 5*	11.3	V
Terminal 7 (Collector to ground)	20	V
Terminal 9 (Collector to ground)	20	V
DC Current (into Terminal 18)	2	mA
Device Dissipation:		
Up to $T_A = 60^\circ C$	600	mW
Above $T_A = 60^\circ C$	derate linearly 6.7 mW/°C	
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	− 65 to +150	°C
Lead Temperature (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

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* This rating does not apply when using the internal zener reference in conjunction with the pass transistor.

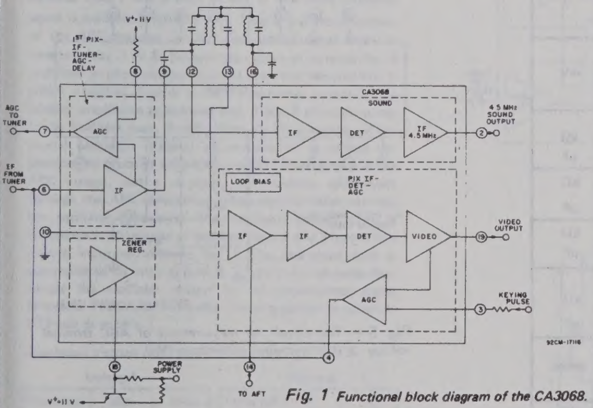


Fig. 1 Functional block diagram of the CA3068.

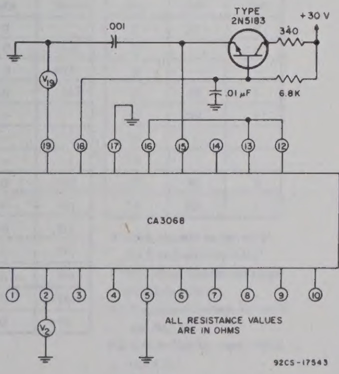
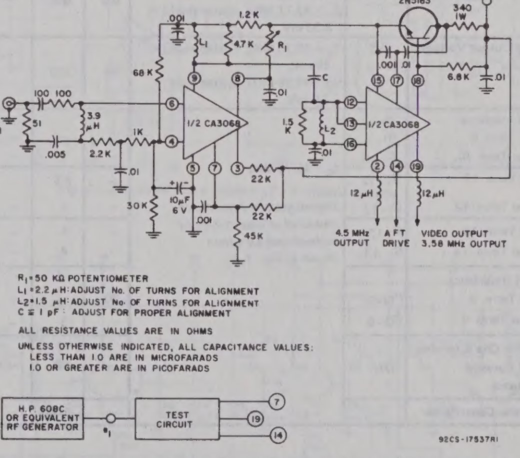
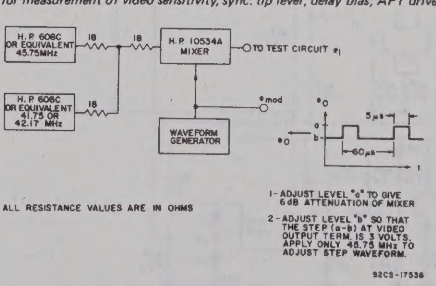


Fig. 2 – Test circuit for measurement of white level (V_{19}) and terminal 2 voltage (V_2).



TYPE 2N5183
V+=28 V
340 1W
.001
1.2 K
4.7 K
R1
L1
68 K
C
.01
.001
.01
6.8 K
.01
100 100
3.9 μH
51
e1
.005
2.2 K
1K
.01
1/2 CA3068
1.5 K
L2
.01
1/2 CA3068
22 K
30 K
10 μF 6 V
.001
22 K
45 K
12 μH
12 μH
4.5 MHz OUTPUT
AFT DRIVE
VIDEO OUTPUT 3.58 MHz OUTPUT
R1=50 KΩ POTENTIOMETER
L1=2.2 μH: ADJUST No. OF TURNS FOR ALIGNMENT
L2=1.5 μH: ADJUST No. OF TURNS FOR ALIGNMENT
C ≅ 1 pF : ADJUST FOR PROPER ALIGNMENT
ALL RESISTANCE VALUES ARE IN OHMS
UNLESS OTHERWISE INDICATED, ALL CAPACITANCE VALUES: LESS THAN 1.0 ARE IN MICROFARADS 1.0 OR GREATER ARE IN PICOFARADS
H.P. 608C OR EQUIVALENT RF GENERATOR
e1
TEST CIRCUIT
92CS-17537R1

(a) Test setup for measurement of video sensitivity, sync. tip level, delay bias, AFT drive voltage.



H.P. 608C OR EQUIVALENT 45.75MHz
18
18
H.P. 10534A MIXER
TO TEST CIRCUIT e1
H.P. 608C OR EQUIVALENT 41.75 OR 42.17 MHz
18
emod
WAVEFORM GENERATOR
eo
a
b
5μs
60μs
t
ALL RESISTANCE VALUES ARE IN OHMS
1- ADJUST LEVEL "a" TO GIVE 6dB ATTENUATION OF MIXER
2- ADJUST LEVEL "b" SO THAT THE STEP (a-b) AT VIDEO OUTPUT TERM. IS 3 VOLTS. APPLY ONLY 45.75 MHz TO ADJUST STEP WAVEFORM.
92CS-17538

(b) Test setup for measurement of sound and chroma outputs.

Fig. 3 – Typical dynamic test circuit diagrams.

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Static (DC) Characteristics						
Quiescent Circuit Current	I_{15}	–	15	–	45	mA
DC Voltages:						
Terminal 2 (Sound)	V_2	–	–	6	–	V
Terminal 3 (Keying Input)	V_3	–	6.4	–	10	V
Terminal 7 (1) (AGC)	V_7	–	16	–	21	V
Terminal 7 (2) (AGC)	V_7	–	–	1	–	V
Terminal 8 (AGC Delay)	V_8	–	–	4	–	V
Terminal 9 (Cascode Collector)	V_9	–	–	8.5	–	V
Terminal 16 (Bias)	V_{16}	–	1.1	–	2.3	V
Terminal 18 (Zener)	V_{18}	$V_5 = V_{17} = 0$ V, $I_{18} = 1$ mA	10.6	11.9	13.2	V
Terminal 19 (White Level)	V_{19}	–	6	–	10	V
Dynamic Characteristics						
Video Sensitivity	e_I	$f_o = 45.75$ MHz, Mod. (AM) = 85% at 400 Hz; Adjust e_I for 4 $V_{p\text{-}p}$ at Term. 19	40	100	200	μV
Sync. Tip Level Voltage	V_{19}	$f_o = 45.75$ MHz, e_I(CW) = 10 mV	0.4	0.8	1.6	V
Automatic Fine Tuning (AFT) Drive Level Voltage	V_{14}		–	15	–	mV
Delay Bias Voltage: At $e_I = 10$ mV	V_7	$f_o = 45.75$ MHz, e_I(CW) = 20 mV;	16	–	–	V
At $e_I = 30$ mV		Adjust R_1 for $V_7 = 14$ V	0.5	–	2	V
3.58 MHz Chroma Output Voltage	V_{19}	$f_o = 45.75$ MHz, e_I(step mod.) = 10 mV; $f_1 = 42.17$ MHz, e_I(step mod.) = 3.33 mV	0.5	0.8	—	V
4.5 MHz Sound Output Voltage	V_2	$f_o = 45.75$ MHz, e_I(step mod.) = 10 mV; $f_2 = 41.25$ MHz, e_I(step mod.) = 2.5 mV	50	200	–	mV
Parallel Input Impedance: Resistance at Term. 6	R_{I-6}	$f_o = 45.75$ MHz Impedance and Admittance measured at bias conditions as developed by circuit shown in Fig. 7	4	–	–	kΩ
Capacitance at Term. 6	C_{I-6}		–	2	–	pF
Resistance at Term. 12	R_{I-12}		–	4.5	–	kΩ
Capacitance at Term. 12	C_{I-12}		–	4	–	pF
Resistance at Term. 13	R_{I-13}		–	5	–	kΩ
Capacitance at Term. 13	C_{I-13}		–	4	–	pF
Parallel Output Impedance: Resistance at Term. 9	R_{O-9}		30	–	–	kΩ
Capacitance at Term. 9	C_{O-9}		–	3	–	pF
Cascode Transfer Characteristics: Magnitude of Forward Transadmittance	$\lvert y_f \rvert$		–	50	–	mmho
Reverse Transfer Capacitance	C_r		–	0.001	–	pF

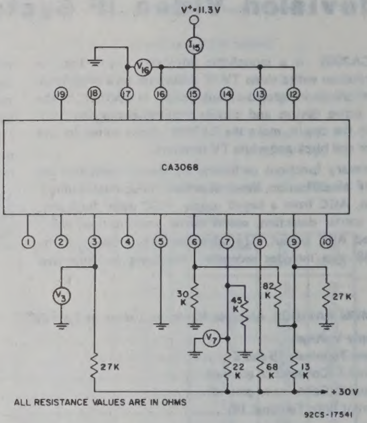


Fig. 4 – Test circuit for measurement of quiescent current (I_{15}), keying terminal voltage (V_3), bias voltage (V_{16}), AGC terminal voltage 1 (V_7), and cascode collector voltage (V_9)

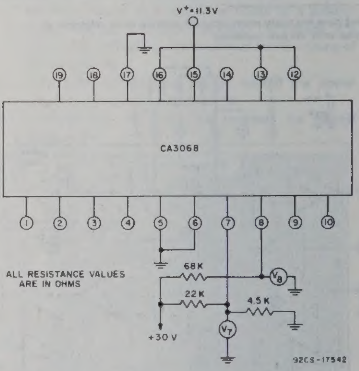


Fig. 5 – Test circuit for measurement of AGC terminal voltage 2 (V_7) and terminal 8 voltage (V_8).

CA3070, CA3071, CA3072 Types

Television Chroma System

The RCA CA3070, CA3071, and CA3072 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3070 is a complete subcarrier regeneration system featuring a new concept of phase control applied to the oscillator circuit. The CA3071 is a chroma amplifier system and the CA3072 performs the demodulation function.

The CA3070 utilizes the 16-lead plastic dual-in-line package; the CA3071 and CA3072 are supplied 14-lead plastic dual-in-line packages.

SYSTEM FEATURES

CA3070

- **Voltage Controlled Oscillator**
- **Keyed APC & ACC Detectors**
- **DC Hue Control**
- **Shunt Regulator**

CA3071

- **ACC Controlled Chroma Amplifier**
- **DC Chroma Gain Control**
- **Color Killer**
- **Amplifier Short-Circuit Protection**

CA3072

- **Synchronous Detector with Color Difference Matrix**
- **Emitter-Follower Output Amplifiers with Short-Circuit Protection**

CA3070
Chroma Signal Processor

The CA3070 is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3071 is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval.

The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 14 of the CA3071. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator.

To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3070 includes a shunt regulator to establish a 12-volt dc supply.

Maximum Voltage and Current Ratings at $T_A = +25^\circ C$

Voltage▲

Terminal No.	Min. Volts	Max. Volts
1	0	*
2	0	+16
3	0	+16
4	–5	N2
6	–	–
7	–	–
8	–	–
10	0	N3
11	0	N1
12	0	N1
13	0	N1
14	0	N1
15	0	+16
16	0	+16

Current

Terminal No.	I_I mA	I_O mA
1	20	1
2	–	–
3	–	–
4	20	1
10	N3	1
11	–	–
12	–	–
13	20	1
14	20	1

▲ With respect to terminal No.5 and with terminal No. 10 connected through 470Ω to +24 V.

N1 Regulated voltage at terminal No. 10.

N2 Controlled by max. input current.

N3 Limited by dissipation.

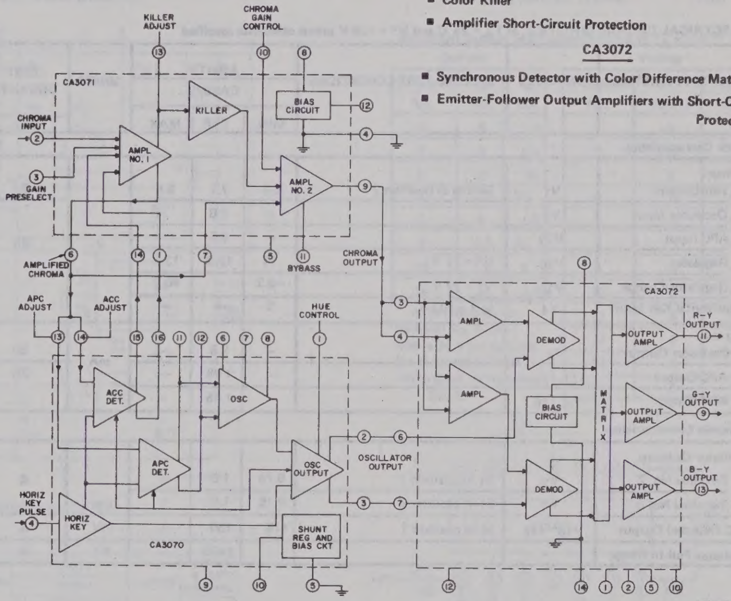


Fig. 1 – Simplified block diagram of TV chroma system.

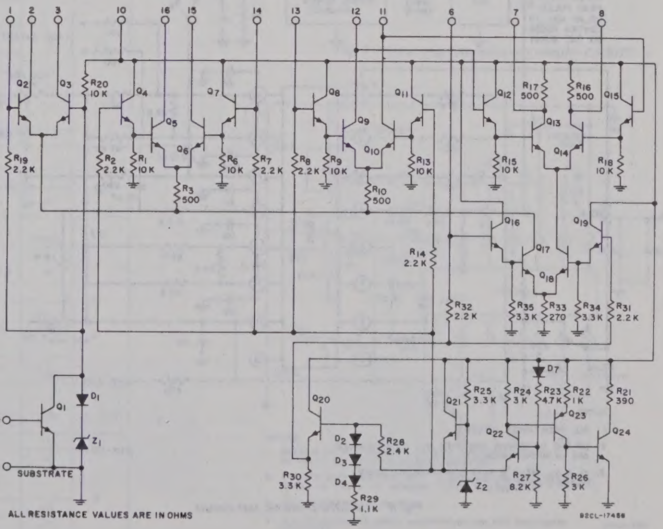


Fig. 2 – Schematic diagram CA3070.

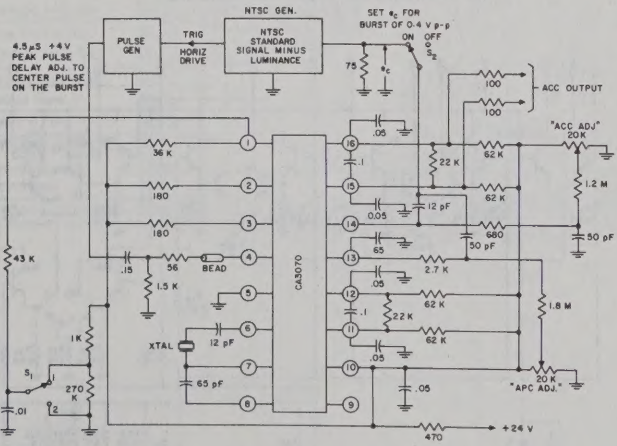
CA3070, CA3071, CA3072 Types

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25°C*

Device Dissipation:
Up to T_A = +70°C .... 530 mW
Above T_A = +70°C ... Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:
Operating .... −40 to +85 °C
Storage .... −65 to +150 °C
Lead Temperature (During Soldering):
At distance 1/32 in. (3.17 mm) from seating plane
for 10 s max. .... +265 °C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3070 MIN.	LIMITS CA3070 TYP.	LIMITS CA3070 MAX.	UNITS	TEST CIRCUITS FIG.
Static Characteristics							
Voltage: Hue Control	V_1	Switch in position 2	6.9	7.7	8.6	V	3c
Oscillator Input	V_6		–	2.8	–		3a
APC Input	V_{13}		–	6.5	–		
Regulator	V_{10}	V^+ = 21 V	11	12.3	13.5		
Regulator Change	V_{10}	V^+ = 27 V	−0.2	–	+0.2		
Horizontal Key Input	V_4	I_4 = −10 µA	5	–	–		
Currents: Oscillator Output	I_2		–	5.8	–	mA	3c
APC Output	I_{11}, I_{12}		–	1.45	–		3b
ACC Output	I_{15}, I_{16}		–	1.45	–		
Dynamic Characteristics							
Oscillator Outputs: Terminal No. 2	V_2	S_1 in position 1	0.75	1.0	–	V_{p-p}	4
Terminal No. 3	V_3	S_1 in position 2	0.75	1.0	–		
ACC Detected Output	$V_{16}-V_{15}$	S_1 in position 1	115	150	–	mV	4
Oscillator Pull-In Range	–		–	±400	–	Hz	4



NOTES:
1. ALL RESISTANCES IN OHMS.
2. UNLESS OTHERWISE SPECIFIED ALL CAPACITANCES ARE IN MICROFARADS.
3. V_2 & V_3 MEAS'D WITH LOW-CAPACITY SCOPE PROBE ≤ 20 pF.

Fig. 4 – CA3070 Dynamic test circuit.

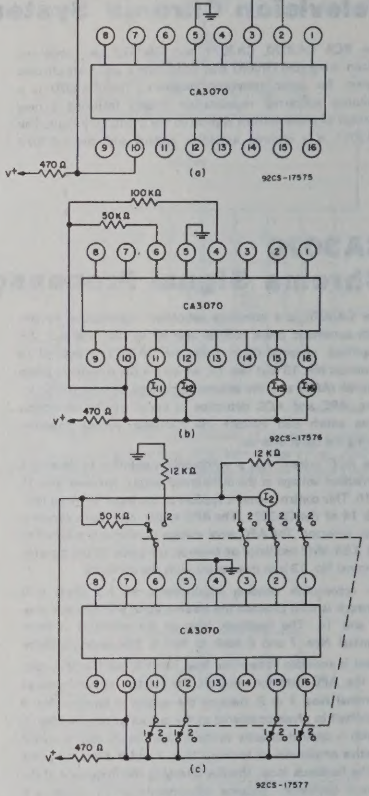


Fig. 3 – Static characteristics test circuits.

Dynamic Test Initial Adjustments

1. APC ADJUST: With S2 in "OFF" position adjust the "APC ADJ" potentiometer to set oscillator frequency at 3.579545MHz ±25 Hz. With S1 in position 1 measure frequency at terminal No. 2 output, using crystal probe shown in Fig. 6.
2. ACC ADJUST: With S2 in "OFF" position adjust "ACC ADJ" potentiometer to give an ACC output reading of 0 ±2 mV.

Procedure to Pull-in Range Measurement

1. Set S1 in position 1 and connect the crystal probe to terminal No. 2.
2. Turn S2 to "OFF" and set "APC ADJ." arm to ground.
3. Turn S2 to "ON" and gradually adjust "APC ADJ" until oscillator "locks" as witnessed by a sharp increase in ACC output voltage between terminal Nos. 15 and 16.
4. Turn S2 to "OFF" and adjust capacitor Cp of crystal probe for maximum deflection on Ballantine Meter.
5. Switch Ballantine meter to "Amplifier" position and read oscillator frequency on counter.
6. Repeat steps 2 – 5 with "APC ADJ" arm set to terminal No. 10 instead of to ground.

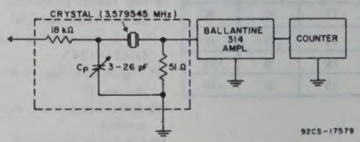


Fig. 5 – Crystal probe for frequency measurements.

CA3071 Chroma Amplifier

The CA3071 is a combined two-stage chroma amplifier and functional control circuit. The input signal is received from the video amplifier and applied to terminal No. 2 of the input amplifier stage. The first amplifier stage is part of the ACC system and is controlled by differential adjustment from the ACC input terminal Nos. 1 and 14. The output of the 1st amplifier is directed to terminal No. 6 from where the signal may be applied to the ACC detection system of the CA3070 or an equivalent circuit. The output at terminal No. 6 is also applied to terminal No. 7 which is the input to the 2nd amplifier stage. Another output of the 1st amplifier at terminal No. 13 is directed to the killer adjustment circuit.

The dc voltage level at terminal No. 13 rises as the ACC differential voltage decreases with a reduction in the burst amplitude. At a pre-set condition determined by the killer adjustment resistor the killer circuit is activated and causes the 2nd chroma amplifier stage to be cut off. The 2nd chroma amplifier stage is also gain controlled by the adjustment of dc voltage at terminal No. 10. The output of the 2nd chroma amplifier stage is available at terminal No. 9. The typical output termination circuit that is shown, provides differential chroma drive signal to the demodulator circuit. Both amplifier outputs utilize emitter-followers with short-circuit protection.

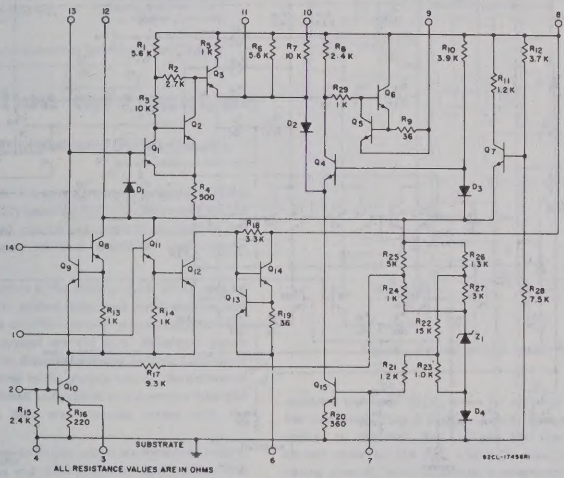


Fig. 6 -Schematic diagram for CA3071.

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

CHARACTERISTICS	SYMBOLS (Measure)	SPECIAL TEST CONDITIONS	LIMITS CA3071 MIN.	TYP.	MAX.	UNITS	CURVES & TEST CIRCUITS FIG.
Static Characteristics							
Voltages Bias Reference Terminal	V_{12}	S_1 Open, S_2 Open	–	17.3	–	V	7
Ampl. No. 1 Chroma Input	V_2	S_1 Open, S_2 Open	–	1.75	–		
Ampl. No. 1 Chroma Output Balanced	V_6	S_1 Open, S_2 Open	–	20	–		
Unbalanced	V_6	S_1 Open, S_2 Closed	–	13.5	–		
Ampl. No. 2 Chroma Input	V_7	S_1 Open, S_2 Open	–	1.5	–		
Ampl. No. 2 Chroma Output	V_9	S_1 Closed, S_2 Open	–	20.6	–		
Supply Current	I_T	S_1 Open, S_2 Open	17	24.5	31	mA	
Dynamic Characteristics							
Amplifier No. 1 Voltage Gain	A_{V1}	E_g 30 mV_{RMS} **Measure** v_6	14	–	–	dB	8
Amplifier No. 2 Voltage Gain	A_{V2}	V_g 1.0 V (RMS) **Measure** v_7	–	14	–	dB	
Max. Chroma Output Voltage	v_9		–	2	–	V_{RMS}	11
10% Chroma Gain Control Reference Voltage	V_8-V_{10}	E_g = 50 mV_{RMS}, adjust Chroma Gain Control to Change v_9 to 10% of Maximum Chroma Output	2.1	3.8	6.8	V	8
Output Voltage, Killer Off	v_9	S_1 in Position 2 E_g = 50 mV_{RMS}, adjust "Killer Adjust" for an abrupt decrease in V_9		–	12	mV RMS	
Output Voltage, Chroma Off	v_9	E_g = 50 mV_{RMS}, adjust Chroma control to min. Chroma Output	–	–	12	mV RMS	
Bandwidth: Amplifier No. 1	BW		–	12	–	MHz	9, 10
Amplifier No. 2			–	30	–		
Ampl. No. 1 Input Impedance	r_i1		–	2	–	kΩ	8
	c_i1		–	4	–	pF	
Ampl. No. 1 Output Impedance	r_o1		–	85	–	Ω	
Ampl. No. 2 Input Impedance	r_i2		–	2.1	–	kΩ	
	c_i2		–	3.5	–	pF	
Ampl. No. 2 Output Impedance	r_o2		–	85	–	Ω	

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25°C*

DC Supply Voltage (Terminal 8 to Terminal 4)	30	VDC
Device Dissipation:		
Up to T_A = +70°C	530	mW
Above T_A = +70°C	Derate Linearly at 6.7 mW/°C	
Ambient Temperature Range:		
Operating	–40 to +85	°C
Storage	–65 to +150	°C
Lead Temperature (During Soldering): At distance 1/32 in (3.17 mm) from seating plane for 10 s max.	+265	°C

Maximum Voltage and Current Ratings @ T_A = +25°C

Current

Terminal No.	I_I mA	I_O mA
1	5	1.0
2	5	1.0
3	10	10
6	1.0	20
7	5	1.0
9	1.0	20
12	1.0	5
14	5	1.0

Voltage*

Terminal No.	MIN VOLTS	MAX VOLTS
1	–5	+15
2	–5	+5
3	0	+2
6	0	+24
7	–5	+5
8	0	+30
9	0	+24
10	0	+24
11	0	+24
12	0	+20
13	0	+20
14	–5	+15

* With reference to terminal No. 4 and with +24 V on terminal No. 8 except for the rating given for terminal No. 8.

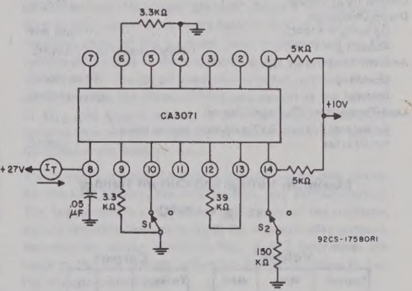
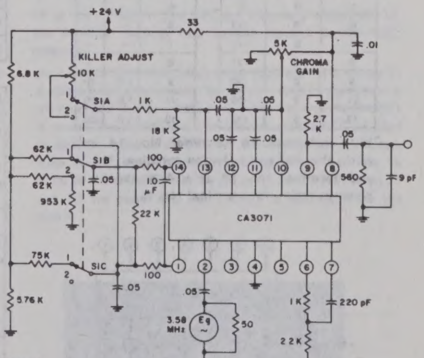


Fig. 7 - Static characteristics test circuit—CA3071.



NOTES:
1. SWITCH S1 IN POSITION 1 UNLESS OTHERWISE NOTED IN TABLE OF DYNAMIC CHARACTERISTICS
2. CHROMA GAIN CONTROL SET TO GROUND UNLESS OTHERWISE NOTED IN TABLE OF DYNAMIC CHARACTERISTICS
3. ALL RESISTANCES IN OHMS
4. ALL CAPACITANCES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED

92CM-17581

Fig. 8 - Dynamic characteristics circuit-CA3071.

CA3070, CA3071, CA3072 Types

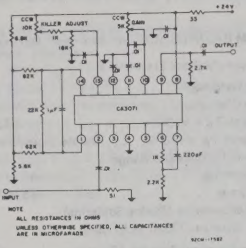


Fig. 9 – CA3071 Wideband amplifier circuit.

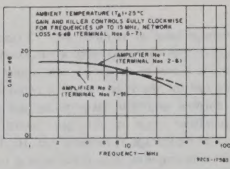


Fig.10— Frequency response for wideband amplifier CA3071.

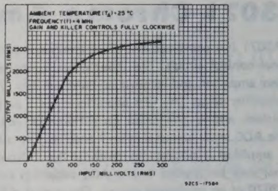


Fig. 11 – Typical CA3071 wideband amplifier linearity

CA3072 Chroma Demodulator

The CA3072 has two sets of synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4 while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color difference signals, after matrix, have a fixed relationship of amplitude and phase nominally equal dc voltage levels. The outputs of the CA3072 are suitable for driving high level color difference or R, G, B output amplifiers. Emitter-follower output stages used to drive the high level color amplifiers have short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25° C*

DC Supply Voltage (Terminal 8 to Terminal 14) .... 27 V
Reference Input Voltage .... 5 v_{p-p}
Chroma Input Voltage .... 5 v_{p-p}
Device Dissipation:
  Up to T_A = +70°C .... 530 mW
  Above T_A = +70°C .... Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:
  Operating .... -40 to +85°C
  Storage .... -65 to +150°C
Lead Temperature (During Soldering):
  At distance 1/32 in (3.17 mm) from seating plane for 10 s max .... +265°C

Maximum Voltage and Current Ratings

at T_A = +25°C

Voltage*

Terminal No.	MIN VOLTS	MAX VOLTS
3	0	+5
4	0	+5
6	0	+12
7	0	+12
8	0	+27
9	0	+20
11	0	+20
13	0	+20

Current

Terminal No.	I_I mA	I_O mA
3	–	–
4	–	–
6	–	–
7	–	–
8	–	–
9	1.0	20
11	1.0	20
13	1.0	20

*With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8.

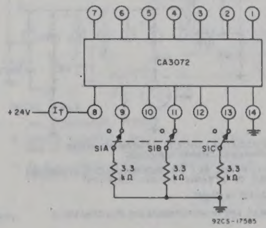


Fig. 13 — Static characteristics test circuit—CA3072.

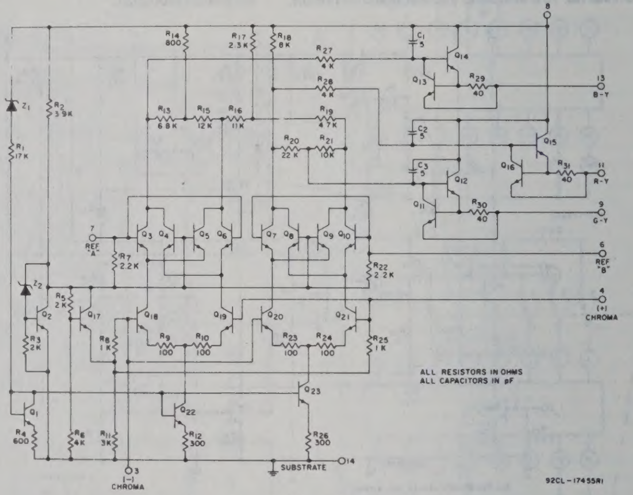
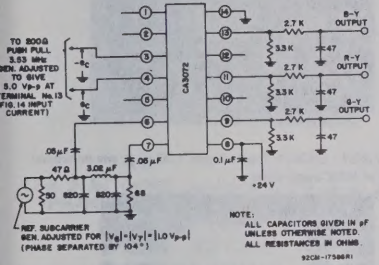


Fig. 12 — Schematic diagram for CA3072.

ELECTRICAL CHARACTERISTICS, at T_A = 25° C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3072 MIN.	LIMITS CA3072 TYP.	LIMITS CA3072 MAX.	UNITS	TEST CIRCUITS FIG.
Static Characteristics							
Supply Current With Output Loads	I_T	S_1 Closed	16.5	–	26.5	mA	13
With No Output Loads		S_1 Open	–	9			
G-Y, R-Y, B-Y Outputs	V_9, V_{11}, V_{13}	S_1 Closed	13.2	14.7	15.8	V	
Chroma Inputs	V_3, V_4	S_1 Open	–	3.3	–		
Reference Subcarrier	V_6, V_7	S_1 Open	–	6.2	–		
Dynamic Characteristics							
Demodulator Unbalance	v_9, v_{11}, v_{13}	$V_3 = V_4 = 0$	–	–	0.8	v_{p-p}	14
Maximum Color Difference Output Voltage	v_{13}	$V_3 = V_4 = 0.6\ V_{P-P}$	8.0	–	–	v_{p-p}	
	v_{11}		5.5	–	–		
	v_9		1.2	–	–		
Chroma Input Sensitivity	v_3	Adjust e_c for 5.0 v_{p-p} @ term No. 13 (B-Y)	–	0.2	0.35		
Relative R-Y Output	v_{11}		3.5	–	4.2		
Relative G-Y Output	v_9		0.75	–	1.25		
V_{DC} Difference Between any two Output Terminals	$\lvert V_9\rvert - \lvert V_{11}\rvert$ $\lvert V_9\rvert - \lvert V_{13}\rvert$ $\lvert V_{11}\rvert - \lvert V_{13}\rvert$	$e_c = 0$	–	–	0.6	V	
Input Impedance Reference Subcarrier Inputs	$r_i6, 7$		–	1.7	–	kΩ	
	$c_i6, 7$		–	6	–	pF	
Input Impedance at Chroma Inputs	$r_i3, 4$		–	0.95	–	kΩ	
	$c_i3, 4$		–	6	–	pF	
Output Resistance	r_o9, r_o11, r_o13		–	180	–	Ω	


CA3072
TO 200Ω PUSH PULL 3.58 MHz GEN. ADJUSTED TO GIVE 5.0 Vp-p AT TERMINAL No.13 (FIG. 14 INPUT CURRENT)
B-Y OUTPUT
R-Y OUTPUT
G-Y OUTPUT
2.7 K
3.3 K
47
.05 μF
47 Ω
3.02 μF
0.1 μF
+24 V
50
820
68
REF. SUBCARRIER GEN. ADJUSTED FOR |V6|=|V7|=|1.0 Vp-p| (PHASE SEPARATED BY 104°)
92CM-17586R1

NOTE:
ALL CAPACITORS GIVEN IN pF UNLESS OTHERWISE NOTED.
ALL RESISTANCES IN OHMS.

Fig. 14 - - Dynamic characteristics test circuit for CA3072.

Application Information

TYPICAL APPLICATION CIRCUIT FOR THE CHROMA SYSTEM

The circuit of *Fig.15* is a complete signal processing system for color TV. The RCA types CA3070, CA3071 and CA3072 monolithic integrated circuits are respectively used as the subcarrier regenerator, chroma amplifier, and chroma demodulator.

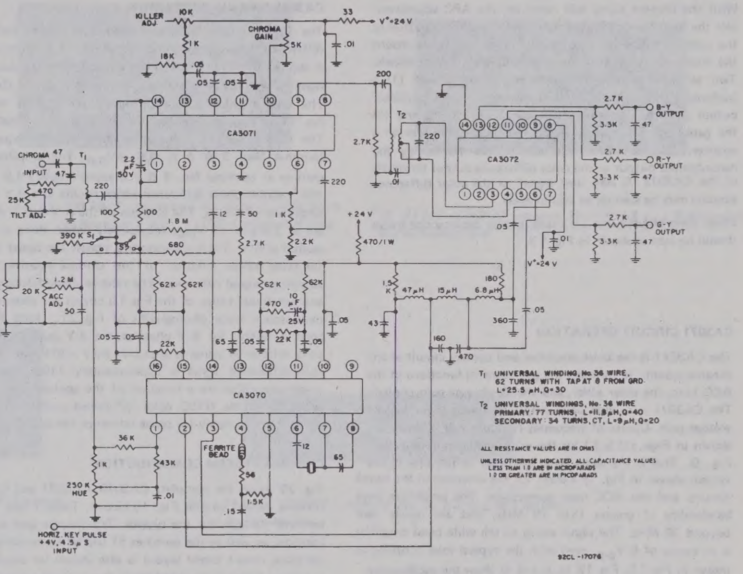
The input to the system is the chroma signal which may be taken from the first or second video stage and is coupled into the CA3071 chroma amplifier through a bandpass filter. The outputs from the system are the color difference signals which are intended to drive high level amplifiers. Luminance mixing may be external to the picture tube or, the difference signals may be amplified and applied to the picture tube grid or cathode, where they are internally mixed with the luminance signal.

Other input requirements to the system are the power supply voltage of +24 volts and the horizontal keying pulse. The power supply voltage should be maintained within ±3 volts of the recommended value of +24 volts. The total current for the system is approximately 70 milliamperes. The horizontal keying pulse input to the subcarrier regenerator is approximately +4 volts peak and centered on the burst as seen at terminal Nos. 13 and 14 of the CA3070. The pulse width should be maintained as close as possible to the recommended value of 4.5 microseconds.

CA3070 Circuit Operation

The CA3070 circuit as shown in Fig. 2, consists of an oscillator, automatic phase control (APC) detector, automatic chroma control (ACC) detector, gated oscillator output amplifier and a shunt regulator. The shunt regulator provides the necessary bias stability for the 3.579545 MHz oscillator, as well as the bias to all functions of the CA3070 circuit. The regulation voltage is nominally +12 volts as measured at terminal No. 10.

The APC and ACC detectors are synchronous detectors which are keyed by the horizontal input pulse. This form of detection eliminates the need for a burst separator as an individual amplifier stage. When a positive pulse is present at terminal No. 4, the oscillator output is cutoff and the oscillator drive signal is diverted to the APC and ACC detectors. Referring to Fig. 2, the APC detector (Q_9 & Q_{10}) and the ACC detector (Q_5 & Q_6) are emitter driven from the oscillator transistor (Q_{17}), when the oscillator output amplifier transistors (Q_2 & Q_3) are cutoff. The chroma signal is applied to terminal Nos. 13 and 14. There is oscillator current drive to the APC and ACC detectors during the keying interval; burst separation is effectively accomplished by the gating action of the detectors. A further advantage of the keying action is the high gain made possible as a result of the low average current flow of the APC and ACC detectors. High resistor values of 62 kilohms at the detector output terminals provide proper detector bias consistent with the duty factor of the keying pulse. For a wider keying pulse, it is necessary that smaller values of detector load resistors be used.



T1 UNIVERSAL WINDING, No. 36 WIRE, 62 TURNS WITH TAP AT 8 FROM GRD. L=25.5 μH, Q=30

T2 UNIVERSAL WINDINGS, No. 36 WIRE PRIMARY: 77 TURNS, L=11.8 μH, Q=40 SECONDARY: 34 TURNS, CT, L=9 μH, Q=20

ALL RESISTANCE VALUES ARE IN OHMS

UNLESS OTHERWISE INDICATED, ALL CAPACITANCE VALUES LESS THAN 1.0 ARE IN MICROFARADS 1.0 OR GREATER ARE IN PICOFARADS

Fig. 15 – Typical chroma system for color-TV receivers utilizing RCA-CA3070, CA3071, and CA3072.

In the absence of the keying pulse (line period), the resistor, R_{20}, biases the oscillator's output amplifier transistors (Q_2 & Q_3) on by keeping their emitters at a higher potential than the base bias voltages of Q_5, Q_6, Q_9, and Q_{10}. The 3.58 MHz signal is now present at terminal Nos. 2 & 3. Photographs of oscilloscope traces for one line period at the terminal Nos. 1, 2, and 3 are shown in Fig. 16. The effect of the keying pulse is shown in Fig.16a, and the cutoff of the oscillator output amplifier is shown in Fig.16(b) and 16c.

The oscillator section of the CA3070 consists of the loop formed by Q_{18} and the emitter driven differential pair, Q_{13} & Q_{14}. The signal output from terminal Nos. 7 & 8 is coupled through the series tuned crystal circuit back through terminal No. 6 to Q_{16} & Q_{17}. The collector of Q_{17} drives the oscillator output amplifier and the APC & ACC detectors. Q_{17} is emitter coupled to transistor Q_{18}. The oscillator frequency and phase control is accomplished by the differential drive from the APC detector to transistors Q_{12} & Q_{15} which control the balance of Q_{13} & Q_{14}. The resulting phase of the feedback loop is determined by the relative amplitudes of the oscillator output signal at terminal Nos. 7 and 8. The 65 pF capacitor between terminal No. 7 and 8 provides the phase shifting component as the balance of Q_{13} and Q_{14} is varied. In this way the APC detector controls the crystal frequency at which the phase shift is cancelled in the feedback loop.

The controls for the CA3070 subcarrier regenerator circuit are the APC balance, the ACC balance, and the hue control. The hue control is a dc balance adjustment of the oscillator output amplifier transistors Q_2 & Q_3. A phase delay network between the output terminals Nos. 2 & 3 determines the range of the hue control, which for the value shown in Fig. 15, is approximately 90°.

The ACC adjustment sets the initial balance of the ACC drive to the input of the CA3071 in Fig. 15 (terminal Nos. 1 and 14 of the CA3071). The APC is a frequency adjustment of the oscillator through the balance control of the APC detector.

As a setup adjustment, for both the ACC and APC, switch S1 is opened and S2 is closed. The chroma input to the system is removed and the dc voltage at terminal No. 6 of the CA3071 is noted. The switch S2 is then opened and the ACC adjusted to set the voltage at terminal No. 6 to that previously noted. Alternatively, the differential dc voltage at terminal Nos. 15 & 16 of the CA3070 may be set to 0 mV (±2 mV) when S1 and S2 are open, and the CA3071 is removed from the circuit.

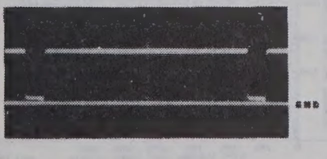


Fig. 16(a) - CA3070 terminal No. 1 7.5 V oscillator "gate off" pulse.

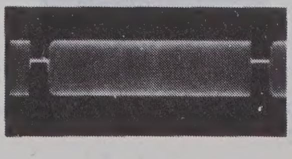


Fig. 16(b) - CA3070 terminal No. 2, 3.5 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

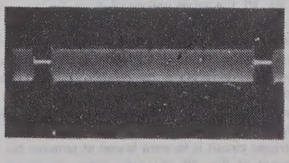


Fig. 16(c) - CA3070 terminal No. 3, 2.0 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

With the chroma signal still removed, the APC adjustment sets the frequency of the oscillator to 3.579545 MHz. Due to the gated off interval, a counter will not accurately record the frequency at the oscillator output amplifier terminals. Two simple and accurate methods are as follows: (1) a buffered crystal filter circuit, connected to the oscillator output amplifier terminals will continue to ring and fill the gated off window providing the proper interface to a counter; (2) the other method involves monitoring the demodulated output at the color difference output terminals of the CA3072. A zero beat signal, at the color difference outputs may be seen on an oscilloscope.

When these adjustments are made, similar oscilloscope traces should be seen as shown in Fig. 17.

CA3071 CIRCUIT OPERATION

The CA3071 is the basic amplifier and control circuit of the chroma system. It contains the gain control functions of the ACC loop, the color killer, and the dc chroma gain control. The CA3071 is a wide band amplifier having two stages of voltage gain. Curves of frequency-response and linearity are shown in Figs. 10 & 11 for the wideband circuits shown in Fig. 9. This is the same basic amplifier as the one in the system shown in Fig. 15 except for the omission of the tuned circuits and the ACC loop connection. The amplifiers have bandwidths of greater than 10 MHz, and are usable well beyond 30 MHz. The signal swing of the wide band amplifier is in excess of 5 V_{p-p}, even with the typical load coupling as shown in Fig. 15. Fig. 18 (a, b and c) show the oscilloscope traces for an NTSC signal at the chroma input. The overall frequency-response curves are shown in Fig. 19.

CA3071 operation is as follows (Refer to Figs. 6 & 15). The input chroma signal is applied to terminal No. 2. This signal is amplified in a cascode differential circuit from Q_{10} to Q_{12} and the output is an emitter follower, Q_{14} (Terminal No. 6.) The signal is divided in the Q_9 & Q_{12} differential amplifier, depending on the applied ACC error signal amplitude at terminal Nos. 1 & 14. The ACC error signal is derived from terminal Nos. 15 & 16 of the CA3070 and after filtering, is applied to terminal Nos. 1 & 14 of the CA3071.

At low signal drive, the 390 kilohm resistor at switch S1 (normally closed) unbalances the differential amplifier for high signal gain through Q_{12}. As the burst level at the chroma input increases, the ACC drive changes differentially in a positive direction at terminal No. 14 and a negative direction at terminal No. 14 and a negative direction at terminal No. 1. At strong signal levels the gain is reduced by diverting the balance of ac current in the differential amplifier from Q_{12} to Q_9, which is shunted to ac ground at terminal Nos. 12 and 13. The ACC loop is completed through the chroma signal at terminal No. 6 of the CA3071 to terminal No. 14 (input) of the CA3070. A typical ACC characteristic is shown in Fig. 23.

The chroma signal is buffer connected from terminal No. 6 to terminal No. 7 of the CA3071 and is amplified in the 2nd stage of voltage gain. Both the color killer adjustment and the dc chroma gain control are applied to the 2nd stage to control the chroma output at terminal No. 9. The color killer section of the CA3071 is a Schmitt trigger & amplifier circuit consisting of transistors Q_1, Q_2 and Q_3. Under maximum chroma output conditions, the diode D_2 is reversed biased, and the signal path is through Q_{15}, Q_4 and Q_5 to terminal No. 9. When the color killer circuit is actuated, or the chroma gain control is adjusted to a higher positive voltage at terminal No. 10, the anode voltage of diode D_2 is increased to draw current from the signal path at the emitter of Q_4. This decreases the chroma gain as the potential at terminal No. 10 is increased. When the potential at terminal No. 10 is the same as terminal No. 8, the chroma output at terminal 9 is cutoff.

The color killer circuit provides an abrupt voltage swing at the anode of D_2 to cutoff the chroma output when the Schmitt trigger circuit is forward biased at terminal No. 13. In the circuit of Fig. 18, the color killer adjustment is a resistance divider circuit which establishes the threshold of burst level at which the killer operates the chroma amplifier.

CA3072 CIRCUIT OPERATION

The CA3072 is a chroma demodulator having full color difference signal demodulation capability. The chroma signal is applied to terminal Nos. 3 & 4 and the reference subcarrier signal is applied to terminals Nos. 6 & 7 of the CA3072. The output color difference signals are B-Y at terminal No. 13, R-Y at terminal No. 11, and G-Y at terminal No. 9. The typical level of differential chroma drive required at terminal Nos. 3 & 4 is 400 mV_{p-p}. The amplitude of chroma at terminal No. 6 & 7 is approximately 1.0 volt at 104° relative phase difference which results in a B-Y output amplitude of $5V_{p-p}$. The voltages of the R-Y & G-Y outputs are at 3.8 and 1.0 V_{p-p} respectively, when there is $5V_{p-p}$ output at B-Y. These comparative signals are based upon a complete phase rotation of the chroma relative to the subcarrier signal reference. The relative demodulation phase and amplitude ratios of the Fig. 15 circuit are shown in the oscilloscope trace photographs of Fig. 21. Using the hue control setting for B-Y phase at the B-Y output, the G-Y color-difference signal is approximately −104° and the R-Y color-difference signal is approximately +106°. Since the amplitude ratios are a function of the applied signal phase relationship, the NTSC color difference output signals are shown here primarily for phase reference conditions.

CHROMA SYSTEM CONSTRUCTION

Fig. 25 shows the complete CA3070, CA3071 and CA3072 chroma system in the Fig. 18 circuit. Table I lists the dc terminal voltages for the system. The chroma gain and hue controls, as well as the switches S1 and S2 are removed. The template circuit board layout is also shown for duplication purposes. It should be noted that a few component values are modified in Fig. 18 from the dynamic circuit values of the data sheet. These are necessary for system matching and overall filter requirements.

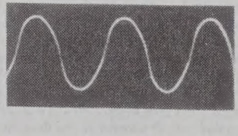


Fig. 17(a) - CA3070 terminal No. 6, oscillator waveform 1.1 V_{p-p} 3.58 MHz.

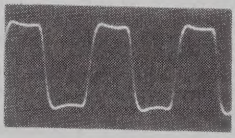


Fig. 17(b) - CA3070 terminal No. 7, oscillator waveform 1.4 V_{p-p} 3.58 MHz.

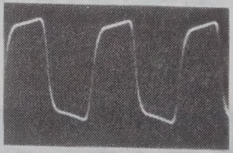


Fig. 17(c) - CA3070 terminal No. 8, oscillator waveform 1.6 V_{p-p} 3.58 MHz.

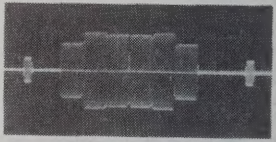


Fig. 18(a) - CA3071 chroma input 1.25 V_{p-p}; one horizontal line of NTSC input signal.

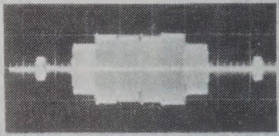


Fig. 18(b) - CA3071 terminal No. 6, amplifier No. 1 chroma output 2.3 V_{p-p}; one horizontal line for 1.25 V_{p-p} chroma input

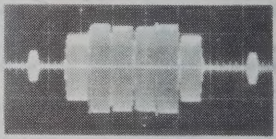


Fig. 18(c) - CA3071 terminal No. 9, amplifier No. 2 chroma output 5.5 V_{p-p}; one horizontal line for 1.25V_{p-p} chroma input

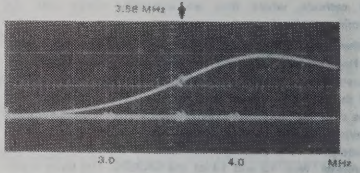


Fig. 19(a) - Frequency response sweep curve between terminal Nos. 2 & 6 for CA3071. f = 250 KHz/div.

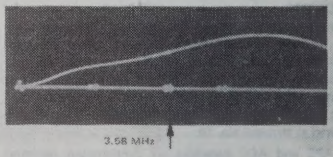


Fig. 19(b) - Frequency response sweep curve between terminal No. 2 of CA3071 and terminal No. 3 of CA3072. f = 250 KHz/div.

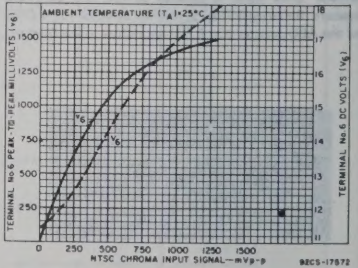


Fig. 20 - Typical ACC characteristics for chroma system of Fig. 18

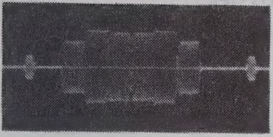


Fig. 21(a) - CA3072 - terminal No. 3 or 4, chroma input signal, 220 mV_{p-p}, one horizontal line

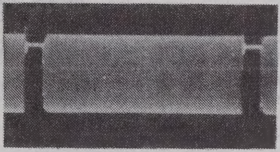


Fig. 21(b) - CA3072 - terminal No. 6 or 7, reference subcarrier 1.2 V_{p-p}, one horizontal line

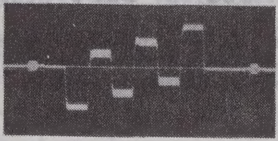


Fig. 21(c) - CA3072 terminal No. 13, 4.8 v_{p-p} B-Y output, one horizontal line

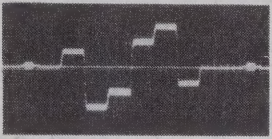


Fig. 21(d) - CA3072 - terminal No. 11, 5.2 v_{p-p} R-Y output, one horizontal line

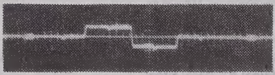


Fig. 21(e) - CA3072 - terminal No. 9, 1.2 v_{p-p} G-Y output, one horizontal line

CA3088E

AM Receiver Subsystem

Includes: AM Converter, IF Amplifiers, Detector and Audio Preamplifier

For Applications in a Variety of AM Broadcast and Communications Receivers and Applications Requiring an Array of Amplifiers

Features:

- **Excellent overload characteristics**
- **AGC for IF amplifier**
- **Buffered output signal for tuning meter**
- **Internal Zener diode provides voltage regulation**
- **Two IF amplifier stages**
- **Low-noise converter and first IF amplifier**
- **Low harmonic distortion (THD)**
- **Delayed AGC for RF amplifier**
- **Terminals for optional inclusion of tone control**
- **Operates from wide range of power supplies: V+ = 6 to 16 volts**
- **Optional AC and/or DC feedback on wide-band amplifier**
- **Array of amplifiers for general-purpose applications**
- **Suitable for use with optional external RF stage, either MOS or bipolar**

RCA-CA3088E*, a monolithic integrated circuit, is an AM subsystem that provides the converter, IF amplifier, detector, and audio preamplifier stages for an AM receiver.

The CA3088E also provides internal AGC for the first IF amplifier stage, delayed AGC for an optional external RF amplifier, a buffer stage to drive a tuning meter, and terminals facilitating the optional use of a tone control.

Fig. 2 is a functional diagram of the CA3088E. The signal from the low-noise converter is applied to the first IF amplifier and is then coupled to the second IF amplifier. This IF signal is then detected and externally filtered. The resultant audio signal is applied to an audio preamplifier. Optionally, a tone control circuit may be connected at the junction of the detector circuit and the audio preamplifier. The gain of the first IF amplifier stage is controlled by an internal AGC circuit. The CA3088E supplies a delayed AGC signal output for use with an external RF amplifier. A buffered output signal is also available for driving a tuning meter. A DC voltage, internally regulated by a Zener diode, supplies the second IF amplifier, the AGC and tuning meter circuits and may also be used with any other stage.

The CA3088E features four independent transistor amplifiers, each incorporating internal biasing for temperature tracking. These amplifiers are particularly useful in general-purpose amplifier, oscillator, and detector applications in a wide variety of equipment designs.

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*Formerly Developmental Type TA5842.

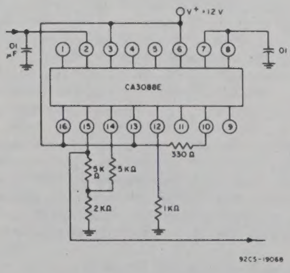


Fig.1—Test circuit for DC characteristics.

MAXIMUM RATINGS, *Absolute Maximum Values, at T_A = 25°C*

DC SUPPLY VOLTAGE:		
Across Term. 5 and Terms. 3, 6, 13, 16, respectively	16	V
DC CURRENT:		
At Terms. 3, 6, 13, 16, respectively	10	mA
At Term. 10	30	mA
DEVICE DISSIPATION:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

The CA3088E is supplied in the 16-lead dual- in-line plastic package.

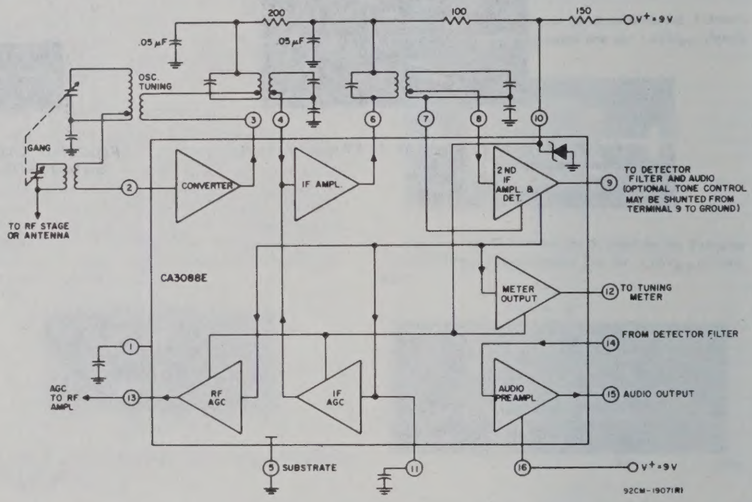


Fig.2—Functional block diagram of the CA3088E.

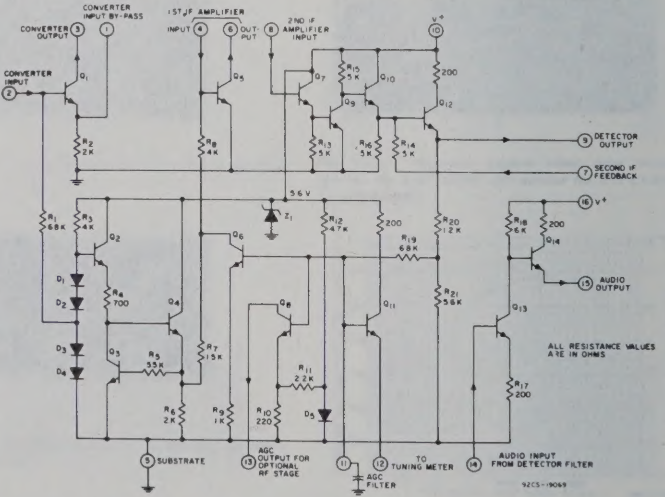
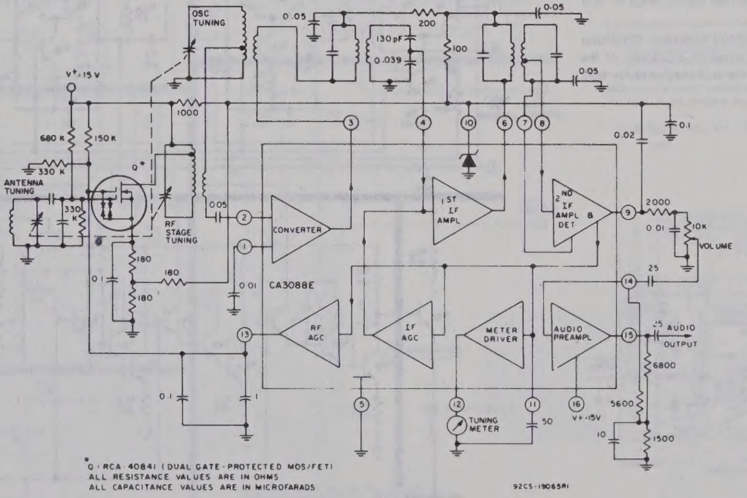


Fig.3—Schematic diagram of the CA3088E.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
		T_A = 25°C V+ = 12 V	TEST CIRCUIT FIG. NO.		
Static (DC) Characteristics					
DC Voltages:					
Terms. 1, 4, 9, 11	$V_{1,4,9,11}$		1	0.7	V
Terms. 2, 7, 8	$V_{2,7,8}$			1.4	V
Term. 10	V_{10}			5.6	V
Term. 12	V_{12}			0	V
Term. 15	V_{15}			3.5	V
DC Current:					
Term. 3	I_3		1	0.35	mA
Term. 6	I_6			1.0	mA
Term. 10	I_{10}			20	mA
Term. 13	I_{13}			0	mA
Term. 16	I_{16}			1.2	mA
Dynamic Characteristics					
Detector Output		30% Modulation	4	75	mV RMS
Audio Amplifier Gain	A_{AF}	f = 1 kHz	4	30	dB
Audio Distortion		V_{OUT} = 100 mV	4	0.2	%
Sensitivity:		f_{IN} = 1 MHz			
At Converter Stage Input		Signal-to-Noise Ratio (S/N) = 20 dB	2	200	µV/m
At RF Stage Input			4	100	µV/m
Total Harmonic Distortion	THD	30% Modulation	4	1.0	%
Input Resistance:	R_I	No AGC, Input signal frequency (f_{IN}) = 1 MHz			
At Transistor Q1				3500	Ω
At Transistor Q5				2000	Ω
Input Capacitance:	C_I				
At Transistor Q1				12	pF
At Transistor Q5				17	pF
Feedback Capacitance:	C_{FB}				
At Transistor Q1				1.5	pF
At Transistor Q5				1.5	pF

The typical characteristics for the CA3088E are intended for guidance purposes in evaluating this device for equipment design.



*Q : RCA 40841 (DUAL GATE-PROTECTED MOS/FET)
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROFARADS

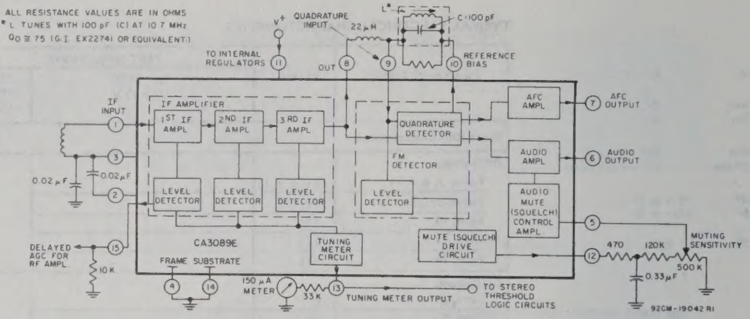
Fig.4—Typical AM broadcast receiver using the CA3088E with optional RF amplifier stage.

CA3089E

FM IF System

Includes–––IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter

For FM IF Amplifier Applications in High-Fidelity Automotive, and Communications Receivers



Block diagram of the CA3089E.

The CA3089E is supplied in the 16-lead dual-in-line plastic package.

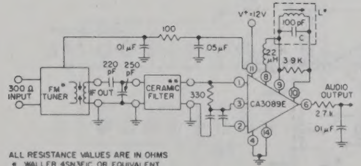
Features:

- Exceptional limiting sensitivity: 12 μV typ. at –3 dB point
- Low distortion: 0.1% typ. (with double-tuned coil)
- Single-coil tuning capability
- High recovered audio: 400 mV typ.
- Provides specific signal for control of interchannel muting (squelch)
- Provides specific signal for direct drive of a tuning meter
- Provides delayed AGC voltage for RF amplifier
- Provides a specific circuit for flexible AFC
- Internal supply-voltage regulators

RCA-CA3089E is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 is a block diagram showing the CA3089E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3089E is ideal for high-fidelity operation. Distortion in a CA3089E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.



ALL RESISTANCE VALUES ARE IN OHMS
* WALLER 4SN3FIC OR EQUIVALENT
** MURATA SFG 10.7 MA OR EQUIVALENT
° L TUNES WITH 100 pF (C) AT 10.7 MHz
Q0 UNLOADED ≅ 75 (G-I EX22741 OR EQUIVALENT)

92CS-19045

Performance data at f_0 = 98 MHz, f_{MOD} = 400 Hz, Deviation = ±75 kHz:

-3dB Limiting Sensitivity	2μV (Antenna Level)
20dB Quieting Sensitivity	1μV (Antenna Level)
30dB Quieting Sensitivity	1.5μV (Antenna Level)

Fig. 1- Typical FM tuner using the CA3089E with a single-tuned detector coil.

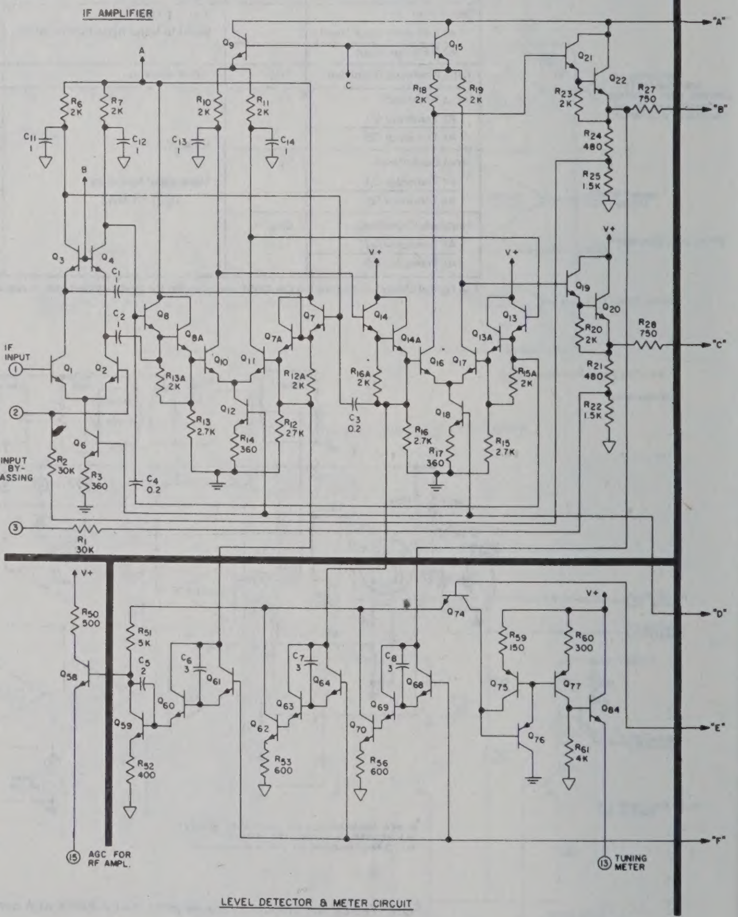
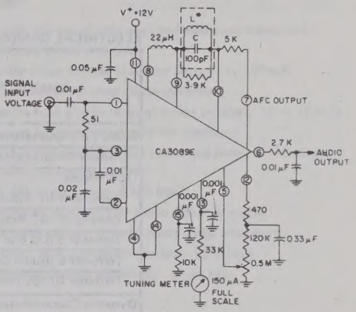


Fig. 2-Schematic diagram of the CA3089E.

MAXIMUM RATINGS, *Absolute Maximum Values, at $T_A = 25^oC$*

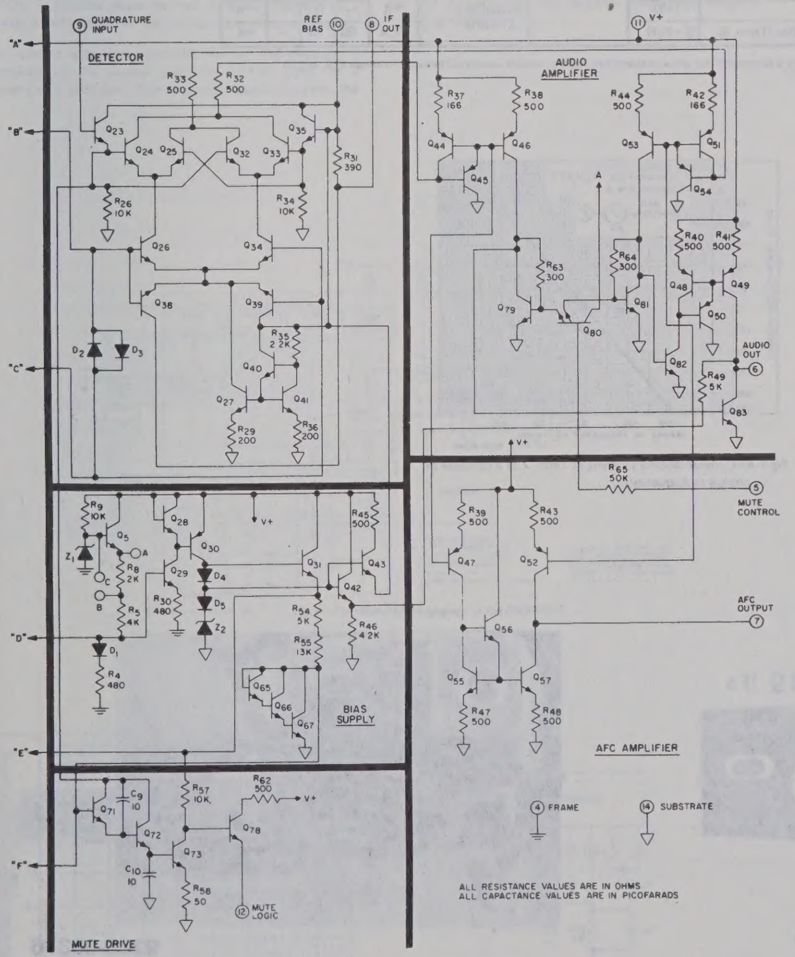
DC Supply Voltage:		
Between Terminals 11 and 4	16	V
Between Terminals 11 and 14	16	V
DC Current (out of Terminal 15)	2	mA
Device Dissipation:		
Up to $T_A = 60^oC$	600	mW
Above $T_A = 60^oC$	derate linearly 6.7 mW/^oC	
Ambient Temperature Range:		
Operating	−55 to +125	^oC
Storage	-65 to +150	^oC
Lead Temperature (During Soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.	+265	^oC



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O(UNLOADED) ≅ 75 (G.I. AUTOMATIC MFG. DIV. EX22741 OR EQUIVALENT)

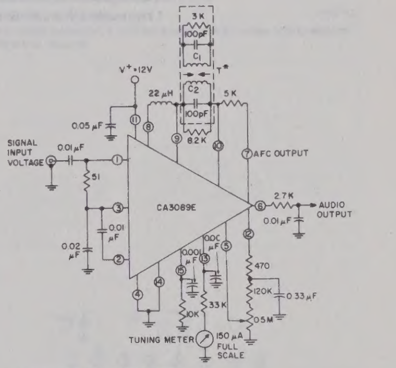
92CM-19040R

Fig.3-Test circuit for CA3089E using a single-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACTANCE VALUES ARE IN PICOFARADS

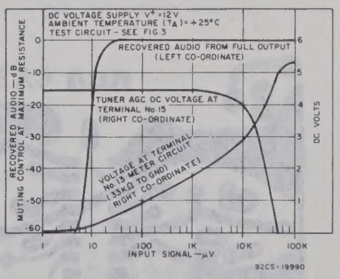
Fig.2-Schematic diagram of the CA3089E.



ALL RESISTANCE VALUES ARE IN OHMS
* T: PRI. – Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20t OF 34e ON 7/32" DIA FORM
SEC. – Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20t OF 34e ON 7/32" DIA FORM
kQ (PER CENT OF CRITICAL COUPLING) ≅ 70%
(ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4mm

92CM-19041R1

Fig.4-Test circuit for CA3089E using a double-tuned detector coil.



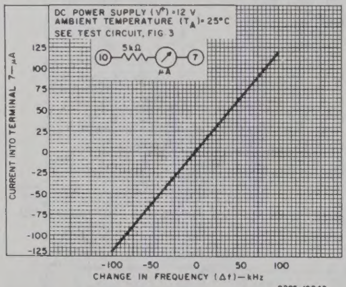
92CS-19990

Fig.5-Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V^+ = 12 Volts

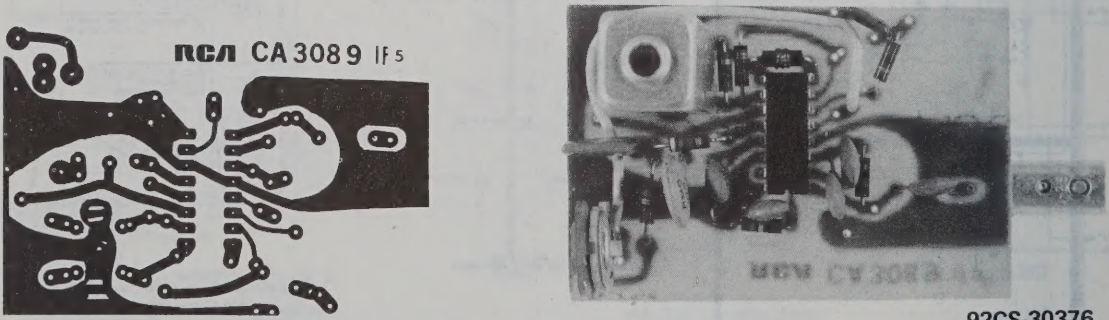
CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
				Circuit Fig. No.	Min.	Typ.	Max.	
Static (DC) Characteristics								
Quiescent Circuit Current	I_{11}	No signal input, Non muted		3, 4	16	23	30	mA
DC Voltages:								
Terminal 1 (IF Input)	V_1				1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2				1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3				1.2	1.9	2.4	V
Terminal 6 (Audio Output)	V_6				5.0	5.6	6.0	V
Terminal 10 (DC Reference)	V_{10}				5.0	5.6	6.0	V
Dynamic Characteristics								
Input Limiting Voltage (-3 dB point)	V_I(lim)	–	f_0 = 10.7 MHz, $f_{mod.}$ = 400 Hz, Deviation = ±75 kHz	3, 4	–	12	25	μV
AM Rejection (Term. 6)	AMR	V_{IN} = 0.1 V, AM Mod. = 30%			45	55	–	dB
Recovered AF Voltage (Term. 6)	V_O(AF)	V_{IN} = 0.1 V			300	400	500	mV
Total Harmonic Distortion: *								
Single Tuned (Term. 6)	THD			3	–	0.5	1.0	%
Double Tuned (Term. 6)	THD			4	–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)	S + N/N			3, 4	60	67	–	dB

* THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.



92CS-19043

Fig.6-AFC characteristics (current at Term. 7 as a function of change in frequency).



92CS-30376

a) Bottom view of printed-circuit board.

b) Component side — top view.

CA3089E and outboard components mounted on a printed-circuit board.

Stereo Multiplex Decoder

For FM Stereo Multiplex Systems

RCA-CA3090AQ , a monolithic silicon integrated circuit, is a stereo multiplex decoder intended for FM multiplex systems.

The CA3090AQ is the successor to the CA3090Q; it offers three major advantages over the CA3090Q as follows:

1. Can directly drive a stereo indicator lamp with a current drain of up to 100 mA.
2. Stereo Defeat/Enable control-voltage specifications.
3. Capable of operation with lower distortion.

This stereo multiplex decoder requires only one low-inductance tuning coil (requires only one adjustment for complete alignment), provides automatic stereo switching, energizes a stereo indicator lamp, and operates from a wide range of voltage supplies.

Figure 1 shows the block diagram for the CA3090AQ. The input signal from the detector is amplified by a low-distortion preamplifier and simultaneously applied to both the 19-kHz and 38-kHz synchronous detectors. A 76-kHz signal, generated by a local voltage-controlled oscillator (VCO), is counted down by two frequency dividers to a 38-kHz signal and to two 19-kHz signals in phase quadrature.

The 19-kHz pilot-tone supplied by the FM detector is compared to the locally generated 19-kHz signal in a synchronous detector. The resultant signal controls the voltage controlled oscillator (VCO) so that it produces an output signal to phase-lock the stereo decoder with the pilot tone. A second synchronous detector compares the locally generated 19-kHz signal with the 19-kHz pilot tone. If the pilot tone exceeds an externally adjustable threshold voltage, a Schmitt trigger circuit is energized. The signal from the Schmitt trigger lights the stereo indicator, enables the 38-kHz synchronous detector, and automatically switches the CA3090AQ from monaural to stereo operation. The output signal from the 38-kHz detector and the composite signal from the preamplifier are applied to a matrixing circuit from which emerge the resultant left and right channel audio signals. These signals are applied to their respective left and right post amplifiers for amplification to a level sufficient to drive most audio amplifiers.

The CA3090AQ may be used without the stereo defeat/enable function (see Fig. 6) if a control voltage for this function is not readily available. In this case, **Terminal 4 should be grounded.**

The CA3090AQ utilizes the 16-lead quad-in-line plastic package and operates over the ambient temperature range of −55°C to +125°C.

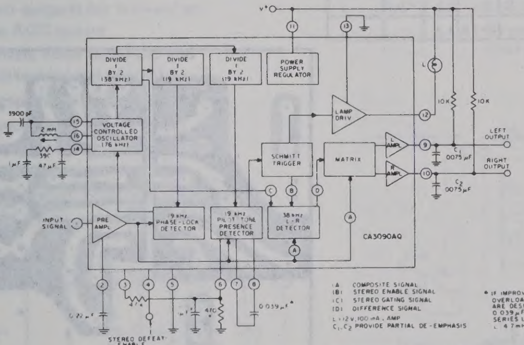
Features:

- **Requires the use of only one low-inductance tuning coil**
- **Automatic stereo switching**
- **Directly drives a stereo indicator lamp up to 100 mA**
- **Includes driver for stereo-lamp indicator**
- **Operates from a wide range of power supplies: 10 to 16 volts**
- **Requires only one adjustment for alignment**
- **Switching from monaural to stereo and stereo to monaural produces no audible thumps**
- **Low distortion: under 0.22% (typ.)**
- **Separate dc input permits stereo defeat or enable**
- **High signal output: directly drives audio amplifiers**
- **Excellent SCA (storecast) rejection: 55 dB typ.**
- **High audio channel separation: 40 dB typ.**

MAXIMUM RATINGS, ***Absolute-Maximum Values at T_A = 25°C***

DC SUPPLY VOLTAGE	16 V
CURRENT AT TERM. 12	100 mA
INPUT SIGNAL VOLTAGE (COMPOSITE)■	400 mV
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C

■ For stereo operation, a minimum input signal voltage (composite) of 40 mV is required

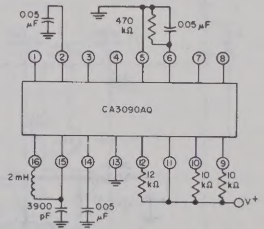


(A) COMPOSITE SIGNAL
(B) STEREO ENABLE SIGNAL
(C) STEREO GATING SIGNAL
(D) DIFFERENCE SIGNAL
L = 12 V, 100 mA, AMP
C_1, C_2 PROVIDE PARTIAL DE-EMPHASIS

* IF IMPROVED SENSITIVITY AND OVERLOAD CHARACTERISTICS ARE DESIRED, REPLACE THE 0.039 µF CAPACITOR WITH A SERIES L C NETWORK WHERE: L = 4.7 mH AND C = 0.015 µF

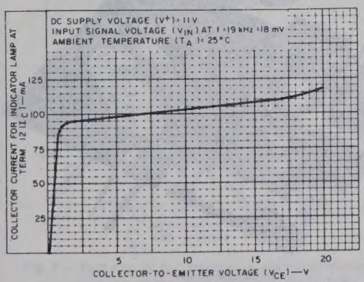
RESISTANCE VALUES ARE IN OHMS

Fig. 1 – Functional block diagram of the CA3090AQ.



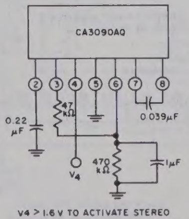
92CS-22550

Fig. 2 – Test circuit for DC characteristics.



92CS-22551

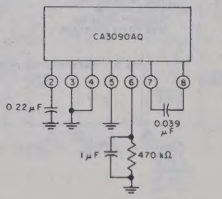
Fig. 3 – Indicator lamp characteristics (I_C vs. V_{CE}).



V4 > 1.6 V TO ACTIVATE STEREO
V4 < 0.9 V TO DEACTIVATE STEREO

92CS-22552

Fig. 4 – Test circuit for use with stereo defeat/enable.



92CS-22553

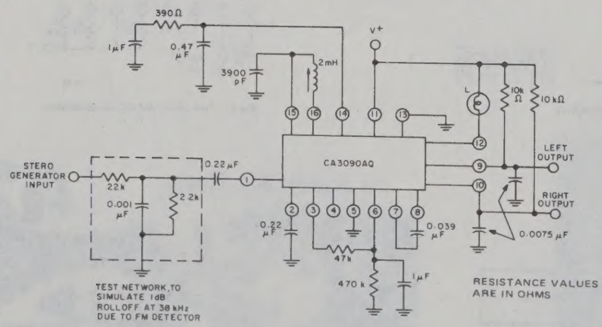
Fig. 5 – Test circuit for use without stereo defeat/enable.

CA3090AQ

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS	LIMITS			UNITS
		$T_A = 25^\circ C$ V+ = 12 V (unless specified otherwise)	Min.	Typ.	Max.	
Static Characteristics						
Total Current (Terms. 9, 10, 11)	I_{total}	Lamp OFF	–	22	27	mA
DC Voltage:						
Term. 1	V_1		1.6	2.3	3.1	V
Term. 6 (Indicator Lamp OFF)	V_6		–	2.1	3.6	V
Terms. 9 and 10	$V_{9\,\&\,10}$		4.7	6.4	8.4	V
Term. 12 (Indicator Lamp OFF)	V_{12}	$V^+ = 16$ V	12.7	–	–	V
Voltage Differential (Term. 2–Term. 1)	$V_2 \cdot V_1$		–	0	0.1	V
Current at Term. 12 (In actual use external circuit resistance (e.g. lamp should limit Term. 12 to the maximum rated value of 100 mA.)		V_{IN} (at f = 19 kHz) = 18 mV	75	100	–	mA
Dynamic Characteristics						
Input Impedance	Z_{IN}		–	50k	–	Ω
Channel Separation (L + R Reference)*		V_{IN} = 180 mV	25	40	–	dB
Channel Balance (Monaural)			–	0.3	3	dB
Monaural Gain			3	6	9	dB
Stereo/Monaural Gain Ratio*			–	±0.3	±3	dB
Indicator Lamp – Turn-ON Voltage		19-kHz pilot-tone @ Term. 1	–	4	–	mV
Capture Range (Deviation from 76-kHz center frequency)		19-kHz pilot-tone voltage = 18 mV	±6.6	±10	–	%
Distortion (75-μs de-emphasis):						
2nd Harmonic		V_{IN} = 240 mV	–	0.2	–	%
3rd, 4th, and 5th Harmonic			–	<0.1	–	%
19-kHz Rejection			–	35	–	dB
38-kHz Rejection			–	48	–	dB
SCA (storecast) Rejection			–	70	–	dB
Stereo Defeat Voltage (V_4)			–	1.2	<0.9	V
Stereo Enable Voltage (V_4)			>1.6	1.2	–	V

* For stereo operation, test conditions require a composite stereo input signal (modulated at 1 kHz) including a 19-kHz (18 mV) pilot-tone signal.



92CM-22554

Fig. 6 – Test circuit for measurement of dynamic characteristics.

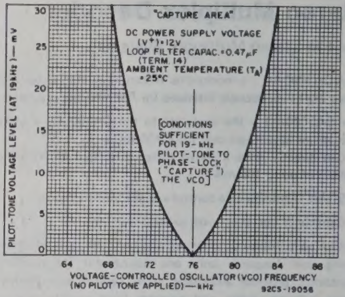


Fig. 7 – Pilot-tone voltage level vs. VCO frequency with no pilot-tone applied.

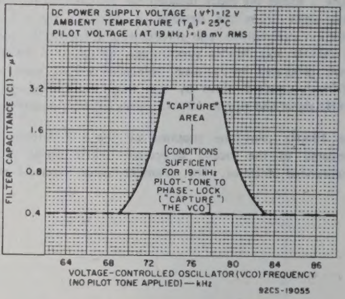
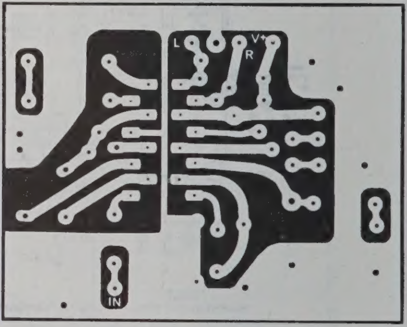
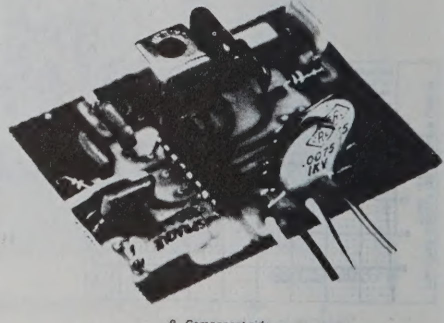


Fig. 8 – Filter capacitance vs. VCO frequency with no pilot-tone applied.



A–Foil side.



B–Component side.

Fig. 9 – Photographs of the CA3090AQ and outboard components mounted on a 2 X 2½-inch printed-circuit board to constitute a complete stereo multiplex decoder.

TV Signal Processors ("Jungle" Circuits)

For Color and Monochrome Receivers

The RCA-CA3120E and CA3142E are monolithic silicon integrated circuit TV signal processors for use in color or monochrome receivers. These circuits provide low-impedance video output signals, stripped synchronization signals in both polarities, and AGC output signals for IF (reverse) and tuner (forward and/or reverse).

The circuit designs of the CA3120E and CA3142E feature impulse noise inversion, delay techniques to reduce the deleterious effects of impulse noise in the receiver AGC and sync circuits. In addition, they incorporate standard AGC strobing techniques. The AGC noise lockout circuit is deleted in the CA3142E.

These devices are supplied in the 16-lead dual-in-line plastic package.

Features:

- Internal impulse noise processing
- Sync separator — low impedance, dual polarity
- Strobed AGC system
- IF AGC output
- Delayed outputs for forward or reverse AGC tuners
- Automatic noise threshold and AGC detector level control
- High-impedance video input
- Low-impedance video output
- Choice of external time constants for sync separator
- Negative power supply not required
- RF AGC delay externally controlled

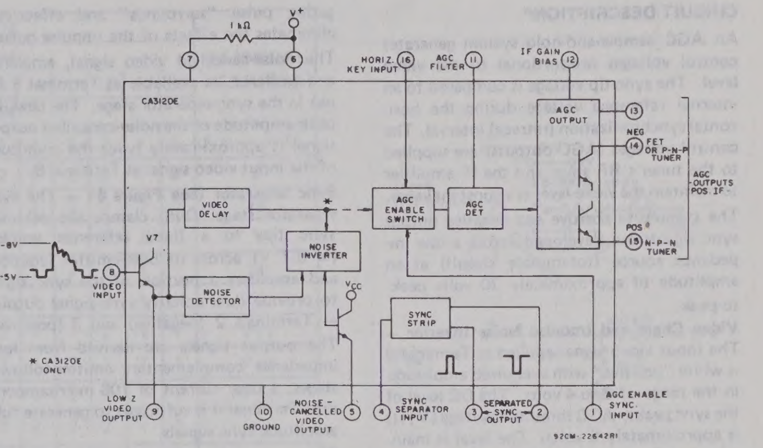


Fig.1 — Simplified block diagram of the CA3120E and CA3142E.

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

DC SUPPLY VOLTAGE	30 V
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	Derate linearly at 7.9 mW/^oC
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85 ^oC
Storage	−65 to +150 ^oC
LEAD TEMPERATURE (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265 ^oC

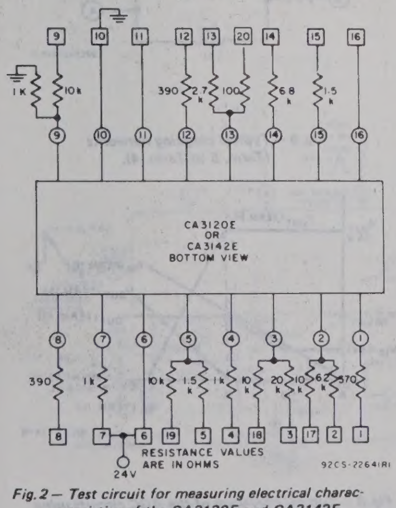


Fig.2 — Test circuit for measuring electrical characteristics of the CA3120E and CA3142E. Refer to Figs. 7 and 8 for switch selector positions.

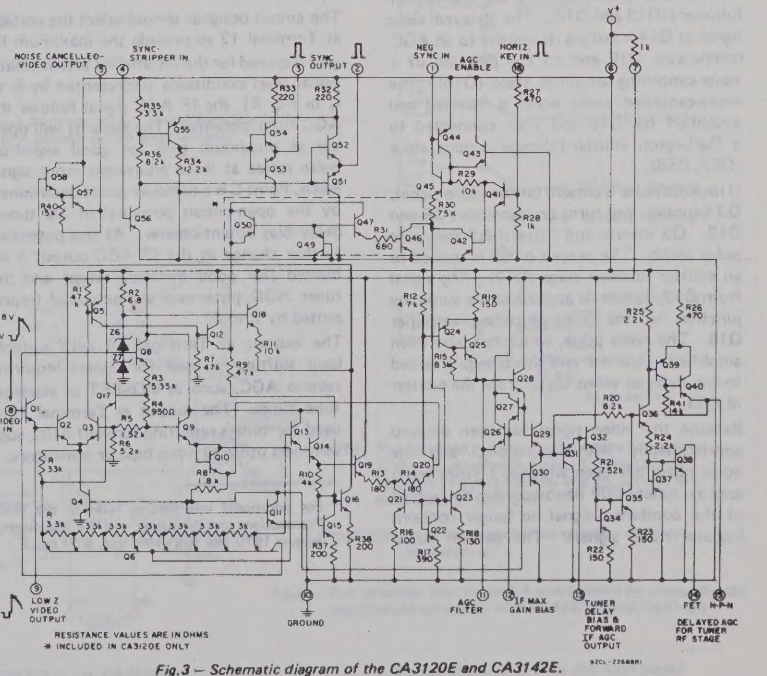


Fig.3 — Schematic diagram of the CA3120E and CA3142E.

CA3120E, CA3142E

CIRCUIT DESCRIPTION*

An AGC sample-and-hold system generates control voltages proportional to the video level. The sync-tip voltage is compared to an internal reference voltage during the horizontal synchronization (retrace) interval. The control voltages (AGC outputs) are supplied to the tuner's RF stage and the IF amplifier to maintain the video level at a constant value.

The composite positive and negative output sync signals are developed across a low impedance source (totem-pole circuit) at an amplitude of approximately 20 volts peak-to-peak.

Video Chain and Impulse Noise Inverter – The input video signal applied at Terminal 8 is white "positive" with a required amplitude in the range of 2 to 4 volts. The DC level of the sync peaks, AGC threshold voltage (V_{TH}) is approximately 5 volts. The level is maintained at 5 volts by the AGC loop in the circuit, comprised of the CA3120E or CA3142E and the TV receiver RF and IF amplifiers. A low source impedance video signal is available from the emitter of Q1 (Terminal 9 in Fig. 3). The external resistor (R_{X1} in Fig.9) reduces the dissipation of Q1. The emitter-follower output of Q1 is directly coupled to a differential comparator stage (Q2, Q3). Unless a negative-going pulse is present, Q2 functions as an emitter follower and also cuts off transistors Q3, Q5, and Q12.

The output of Q2 is applied through a signal delay network, consisting of transistor Q60 and associated resistors, to the Darlington followers (Q13 and Q14). The delayed video signal at Q14 is fed via its emitter to an AGC comparator Q19 and to the junction of a noise-cancelling amplifier stage (Q16). The noise-cancelled video signal is inverted and amplified by Q16 and then connected to a Darlington emitter-follower output stage (Q57, Q58).

If impulse noise is present on the video signal, Q3 conducts and turns on transistors Q5 and Q12. Q5 inverts and "stretches" the noise pulse width. The output of Q5 is applied to an emitter follower stage (Q12). The signal from Q12, in turn, is applied to the summing junction to the noise-cancelling amplifier Q16. The noise pulse, which has now been amplified, inverted and stretched, is added to the delayed video signal from the emitter of Q14.

Because the video signal has been delayed approximately 300 nanoseconds and the noise pulse has been widened ("stretched") approximately 500 nanoseconds, the output of the combined signal no longer contains impulse noise signals. The derived noise-gating pulse "surrounds" and effectively eliminates the effects of the impulse noise.

The noise-cancelled video signal, amplified and buffered, is available at Terminal 5 for use in the sync-separator stage. The peak-to-peak amplitude of the noise-cancelled output signal is approximately twice the amplitude of the input video signal at Terminal 8.

Sync Separator (See Figure 4) – The sync separator stage (Q56) clamps the detected sync tips to a fixed reference voltage (≅ 0.7 V) across its base-emitter junction, and amplifies a portion of the sync signal to provide dual polarity sync-signal outputs at Terminals 2 (negative) and 3 (positive). The output signals are derived from low-impedance complementary emitter-follower stages; a base current of 100 microamperes into Terminal 4 is sufficient to generate full-amplitude sync signals.

The choice of coupling the noise-cancelled video-signal from the emitter-follower (Terminal 5) to the sync separator (Terminal 4) is a user option. Fig. 5 shows three typical coupling networks.

Fig. 6 illustrates the operation of the AGC circuits. An input ramp signal, simulating the potential to which the AGC filter capacitor may be charged, is applied to Terminal 11. The forward IF AGC output voltage appears at Terminal 13. Under low-signal level conditions (represented by A to B in Fig. 6) the output level is approximately 1.4 volts less than the voltage applied to Terminal 12.

The circuit designer should select the voltage at Terminal 12 to provide the maximum IF gain required for the system. At intermediate signal level conditions (represented by B to C in Fig. 6), the IF AGC signal follows the AGC filter potential. The tuner(s) will operate at maximum gain for good signal-to-noise ratios at these equivalent input signal levels. Point C is a turnover point determined by the open-circuit potential of the tuner-delay bias potentiometer. At this potential, further change in the IF AGC output is inhibited (for good dynamic range) and the tuner AGC potentials are activated (represented by C to D).

The output at Terminal 14 with suitable level shifting is used for tuners requiring reverse AGC, such as MOSFET or electron-tube types. The output at Terminal 15 is used for tuners requiring forward AGC, such as tuners utilizing n-p-n bipolar transistors.

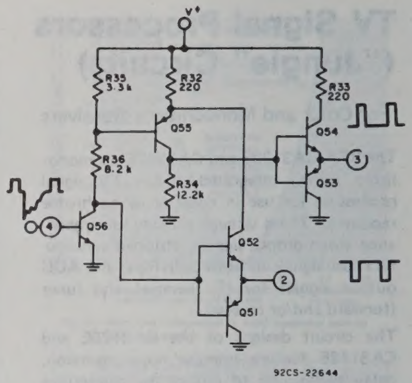


Fig.4 – Sync separator stage.

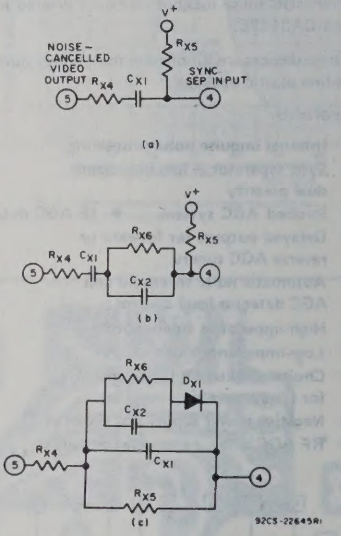


Fig. 5 – Typical coupling networks (Term. 5 to Term. 4).

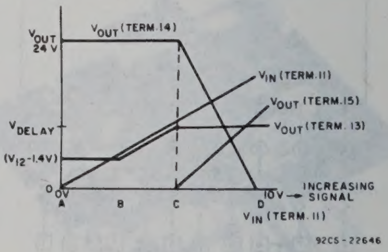


Fig.6 – Typical operation of the AGC circuits using the CA3120E and CA3142E.

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* For additional information refer to the IEEE Transactions on Broadcast and TV Receivers," August 1970, pp. 185–195, Vol. BTR No.3.

CHARAC-TERISTIC	TEST CONDITIONS SWITCH NUMBERS SWITCH POSITION *1*	*2*	*3*	*4*	*5*	*8*	*9*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*19*	*20*	TERMINAL MEASURED
I_{T24}	2	3	1	2	1	2	3	1	1	3	2	1	2	2	2	1	5	*2 6 7 9 14*
V_{TH}	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	1	3	*8*
V_5	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	2	3	*19*
$V_{TH(SEP)}$	3	1	2	1	1	*	3	3	4	1	1	2	1	2	2	2	1	*
$I_{4(OFF)}$	3	1	2	4	2	1	1	1	1	1	1	2	1	2	2	1	1	I_4
V_{2L}	1	2	2	3	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{2H}	3	3	1	1	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{3L}	3	3	1	1	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
V_{3H}	3	3	1	3	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
$I_{11(CH)}$	2	1	2	5	2	1	1	5	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(DISCH)}$	2	1	2	5	1	2	3	6	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(LEAK)}$	2	1	2	5	2	1	1	6	4	3	2	2	1	2	2	1	5	I_{11}
V_{11}	2	1	2	5	1	2	3	2	3	3	1	2	2	2	2	1	5	V_{11}
V_{12}	3	1	2	5	2	1	1	3	4	3	1	2	1	2	2	1	5	V_{12}
$V_{13(LOW)}$	3	1	2	5	2	2	3	1	1	2	1	2	1	2	2	1	2	V_{13}
$V_{13(HIGH)}$	3	1	2	5	2	2	3	7	4	3	2	1	1	2	2	1	4	V_{20}
$I_{14(OFF)}$	3	1	2	5	2	2	3	3	4	3	3	1	1	2	2	1	5	I_{14}
$I_{14(ON)}$	3	1	2	5	2	2	3	8	4	3	3	1	1	2	2	1	5	I_{14}
$I_{15(OFF)}$	3	1	2	5	2	2	3	3	4	3	2	3	1	2	2	1	5	I_{15}
$I_{15(ON)}$	3	1	2	5	2	2	3	8	4	3	2	3	1	2	2	1	5	I_{15}

CAUTION: Remove power before selecting or adjusting switches.

* Reduce voltage at Terminal 8 until V_{19} decreases. $V_{TH(SEP)} = V_{TH} - V_8$.

NOTE: Switch numbers in italics correspond to numbers in square boxes in Figs. 2 and 8.

Fig.7 – Test condition values for associated switches 1 through 20 (switches 6, 7, and 10 are omitted). Refer to Figs. 2 and 8 for test circuit and test-condition selector-switch arrangements.

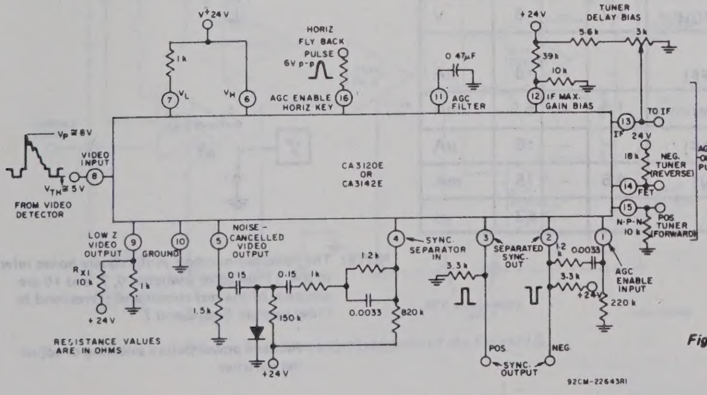
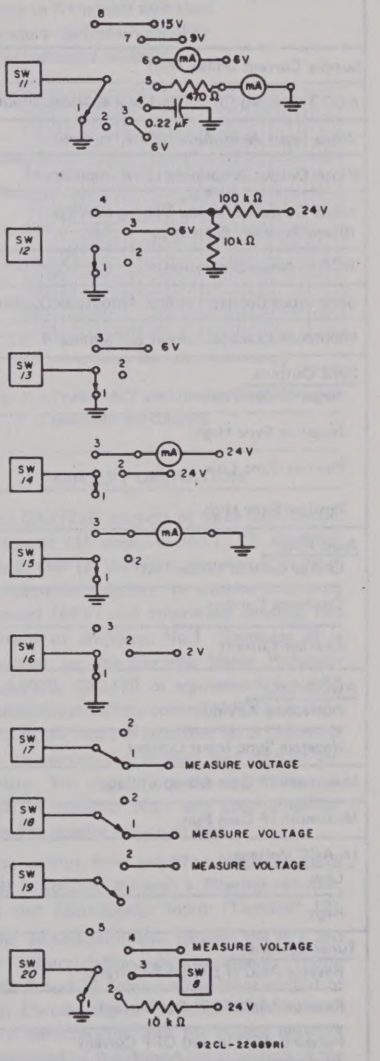


Fig.9 – Typical application using the CA3120E and CA3142E.



NOTE: The italicized numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 2 and 7.

CAUTION: Remove power before selecting or adjusting switches

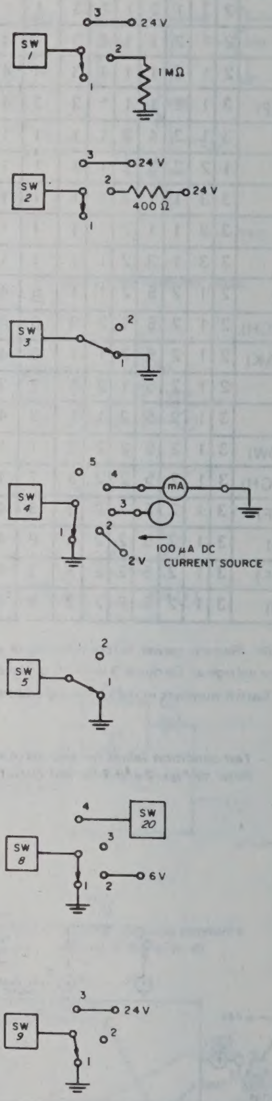
Fig.8 – Test condition selector switch arrangement for measuring the electrical characteristics of the CA3120E and CA3142E.

(Figure 8 continued on the next page)

CA3120E, CA3142E

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, Supply Voltage (V^+) = 24 V and Referenced to Test Circuits and Test Conditions (Figs. 2, 7, and 8).

CHARACTERISTICS	TERMINAL MEASURED AND SYMBOL	CA3120E CA3142E LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current (Pulse Test)	I_{T24}	20	–	40	mA
AGC Threshold (Sync Tip Level at Video Input)	V_{TH}	4.5	–	5.5	V
Video Input Amplitude (White Positive)	V_8	–	3	–	Vp-p
Video Output Amplitude (Low Impedance)	V_9	–	3	–	Vp-p
Noise Cancelled Video Output at V_{TH} (Black Positive, Gain ≅ 2)	V_5	3.6	–	9.2	V
AGC to Noise Separation	$V_{TH\ (SEP)}$	1.1	–	2.2	V
Sync Input Current for Full Amplitude Outputs	$I_{4\ (ON)}$	–	–	100	μA
Maximum Leakage Current at Terminal 4	$I_{4\ (OFF)}$	–	–	±6	μA
Sync Outputs:					
Negative Sync Low	$V_{2(L)}$	0	–	2.6	V
Negative Sync High	$V_{2(H)}$	23.8	–	24	V
Positive Sync Low	$V_{3(L)}$	0	–	0.2	V
Positive Sync High	$V_{3(H)}$	20.1	–	24	V
AGC Filter:					
Charge Current (Pulse Test)	$I_{11(CH)}$	12	–	36	mA
Discharge Current	$I_{11(DISCH)}$	1.1	–	2.6	mA
Leakage Current	$I_{11(LEAK)}$	–	–	±6	μA
AGC Enable:					
Horizontal Keying	$V_{16\ (ON)}$	3	–	6	V
Negative Sync Input Current	$I_{1\ (ON)}$	–	1	–	mA
Maximum IF Gain-Clamp Voltage	V_{11}	4.8	–	5.7	V
Maximum IF Gain Bias	V_{12}	4.2	–	5.2	V
IF AGC Voltage:					
Low	$V_{13\ (LOW)}$	0	–	3.3	V
High	$V_{13(HIGH)}$	5.7	–	6	V
Tuner Currents:					
Reverse AGC (FET) OFF Current	$I_{14\ (OFF)}$	–	–	±6	μA
Reverse AGC (FET) ON Current	$I_{14\ (ON)}$	1.8	–	5.5	mA
Forward AGC (n-p-n) OFF Current	$I_{15\ (OFF)}$	–	–	±6	μA
Reverse AGC (n-p-n) ON Current	$I_{15\ (ON)}$	4.5	–	15	mA
Internal Noise-Lockout Time (CA3120E only)	T	1	–	63	μs



NOTE: The italicized numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 2 and 7.

CAUTION: Remove power before selecting or adjusting switches

Fig.8 – Test condition selector switch arrangement for measuring the electrical characteristics of the CA3120E and CA3142E.

TV Chroma Amplifier/ Demodulator

Provides Complete System for Processing Chroma When Used with RCA-CA3070 or CA3170
"G" Suffix Type-Hermetic Gold-CHIP in Dual-in-Line Plastic Package

RCA-CA3121G is a monolithic silicon integrated circuit chroma amplifier/demodulator with ACC and killer control for color-TV receivers. It is designed to function compatibly with the CA3070 or CA3170 in a two-package chroma system. Figs. 5 and 6 show a functional block diagram and the outboard circuitry of a typical two-package chroma system incorporating the CA3121G and CA3170, respectively.

The CA3121G is supplied in a 16-lead dual-in-line plastic package with hermetic Gold-CHIP (G suffix).

The transistor chips used in the hermetic Gold-CHIP plastic packages are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminents without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multilayered, highly corrosion-resistant, terminal-connection system of unique design is employed.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Supply Voltage	30 V
Device Dissipation:	
Up to T_A = 15°C	1 W
Above T_A = 55°C	derate linearly 10.5 mW/°C
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (During Soldering)	
At distance 1/16" ±1/32" (1.59 ±0.79 mm) from case for 10 s max.	+265°C

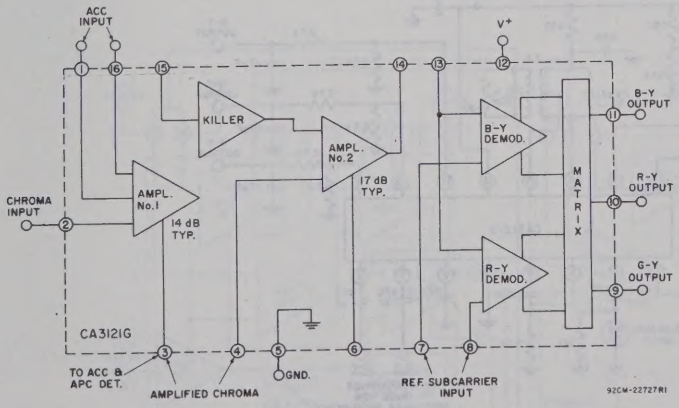


Fig. 1 – Functional block diagram of the CA3121G.

Features:

- **Excellent linearity in dc chroma gain-control circuit**
- **Improved filtering resulting in reduced 7.2 MHz output from the color demodulators**
- **Current limiting for short-circuit protection**
- **Good tolerance to B+ supply variations**
- **Good temperature coefficient stability**
- **Gold-CHIP for increased reliability**

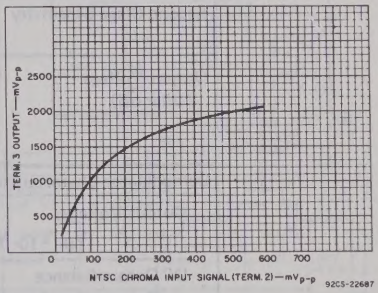


Fig. 2 – Typical ACC plot for the CA3121G when used with the CA3070.

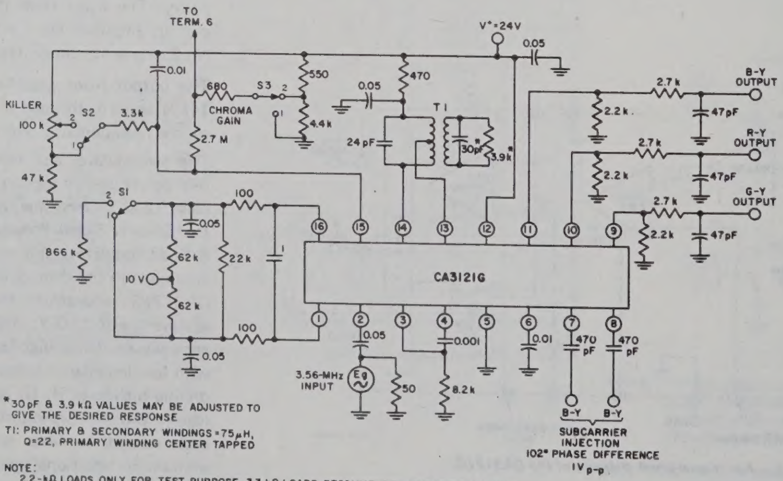
CIRCUIT OPERATION

The CA3121G consists of three basic circuit sections: (1) amplifier No.1, (2) amplifier No.2, and (3) demodulator. Amplifier No.1 contains the circuitry for automatic chroma control (ACC) and color-killer sensing. The output of amplifier No.1 (Terminal 3) is coupled to the Chroma Signal Processor (CA3070, CA3170 or equivalent) for ACC and automatic phase control (APC) operation and to the input of amplifier No.2 (Terminal 4) containing the chroma gain control circuitry. The signal from the color-killer circuit in amplifier No.1 acts upon amplifier No.2 to greatly reduce its gain.

The output from amplifier No.2 (Terminal 14) is applied, through a filtering network, to the demodulator input (Terminal 13). The demodulator also receives the R-Y and B-Y demodulation subcarrier signals (Terminals 7 and 8) from the oscillator output of the Chroma Signal Processor. The R-Y and B-Y demodulators and the matrix network contained in the demodulator section of the CA3121G reconstruct the G-Y signal to achieve the R-Y, G-Y, and B-Y color difference signals. These high-level outputs signals with low impedance outputs are suitable for driving high-level R, G, and B output amplifiers. Internal capacitors are included on each output to filter out unwanted harmonics. For additional operating information and signal waveforms, refer to Television Chroma System (utilizing RCA-CA3070, CA3071, CA3072), File No. 468.

ELECTRICAL CHARACTERISTICS at T_A = 25°C and Reference to Test Circuit (Fig. 3)

CHARACTERISTIC, TERMINAL MEASURED, AND SYMBOL		TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Supply Current	I_T	–	–	40	50	mA
Input Sensitivity	V_2	Vary Eg; set V_4 for 55 mV RMS	6	10	15	mV RMS
Second-Stage Sensitivity	V_4	Vary Eg; set V_{11} for 2 V RMS	25	55	100	mV RMS
Output Voltage (Killer off)	V_{11}	Switch Position: S1=2, S2=2, S3=2 Adjust killer potentiometer until output drops	–	–	70	mV RMS
Demodulator Characteristics:						
Output Voltages	V_9, V_{10}, V_{11}	–	13	14.3	15.6	V
DC Output Balance (Between any 2 outputs)		–	–0.6	–	+0.6	V
Unbalance	V_9, V_{10}, V_{11}	Eg=0; Swith Position: S1=1, S2=1, S3=1	–	–	0.8	Vp-p
Relative Outputs— R-Y	V_{10}	Vary Eg; set V_{11} for 2 V RMS	1.4	1.52	1.68	V RMS
G-Y	V9		0.3	0.4	0.5	V RMS
Relative Phase— R-Y	V_{10}	Vary Eg; set V_{11} for 2 V RMS; read phase of V_{10} and V_9	–101	–106	–111	degrees
G-Y	V_9	with V_{11} as reference	112	104	96	degrees
Max. Output Voltage	V_{11}	Eg = 750 mV	2.8	–	–	V RMS



*30 pF & 3.9 kΩ VALUES MAY BE ADJUSTED TO GIVE THE DESIRED RESPONSE

TI: PRIMARY & SECONDARY WINDINGS = 75 μH, Q=22, PRIMARY WINDING CENTER TAPPED

NOTE:
2.2-kΩ LOADS ONLY FOR TEST PURPOSE, 3.3-kΩ LOADS RECOMMENDED FOR APPLICATIONS.
RESISTANCE VALUES ARE IN OHMS.
CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE INDICATED.

Fig. 3 – Typical characteristics test circuit for the CA3121G.

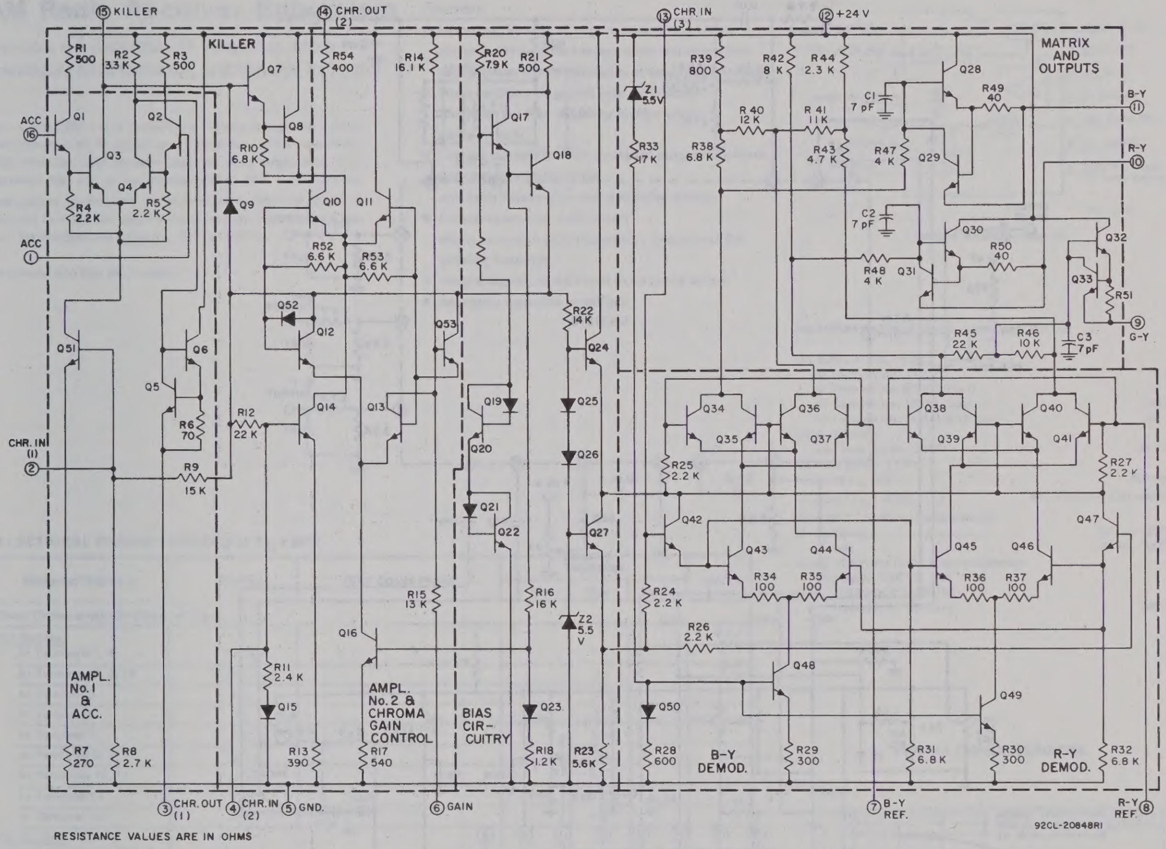


Fig. 4 – Schematic diagram of the CA3121G .

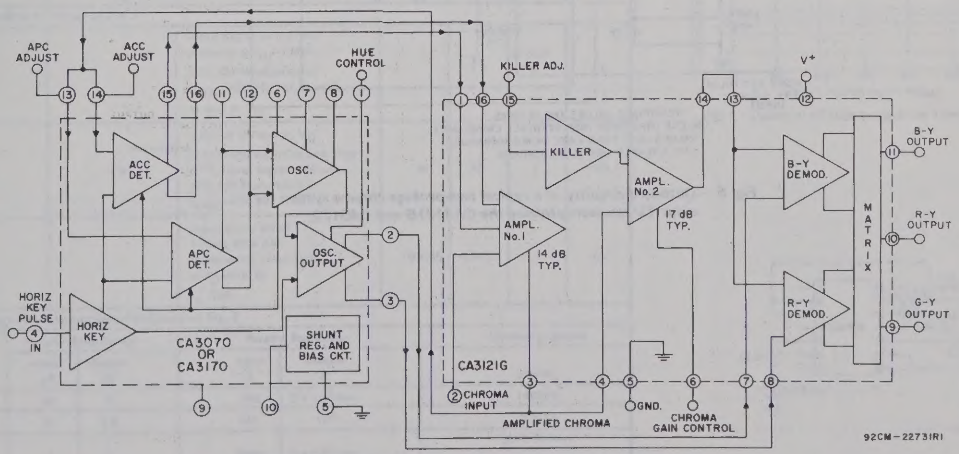
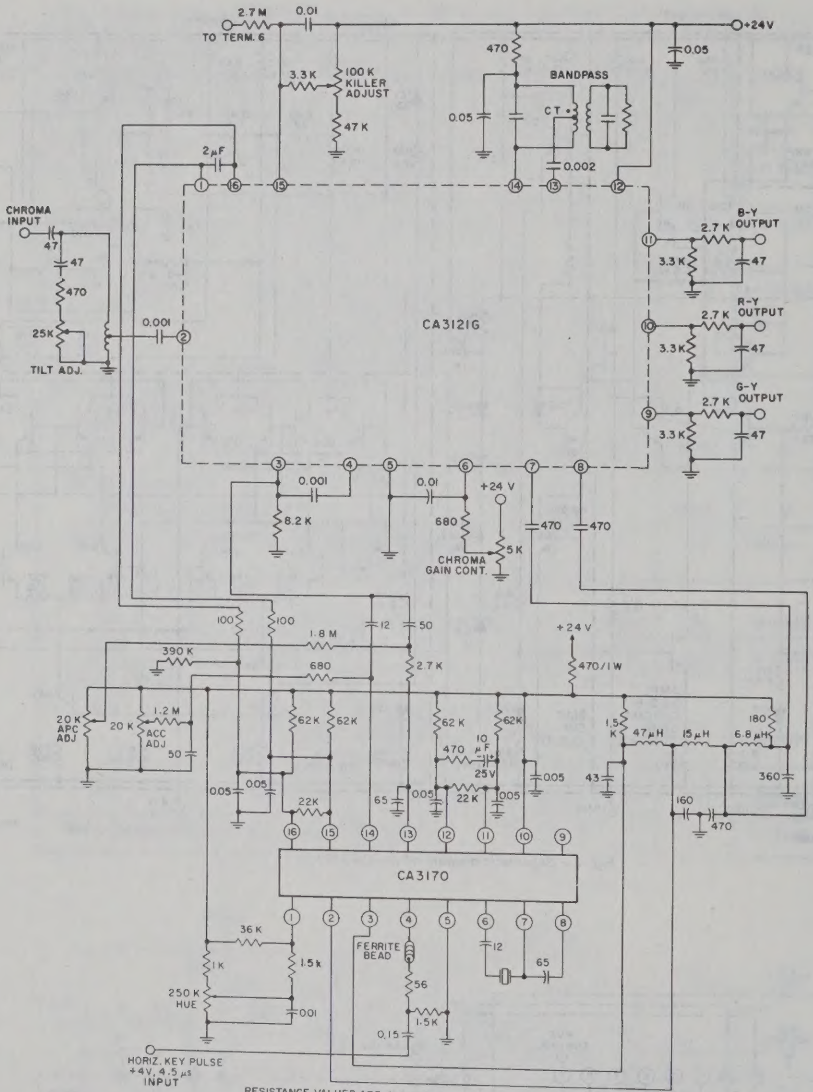


Fig. 5 – Simplified functional diagram of a two-package TV chroma system utilizing the CA3121G and CA3070 or CA3170 .



RESISTANCE VALUES ARE IN OHMS.
UNLESS OTHERWISE INDICATED, ALL CAPACITANCE VALUES LESS THAN 1 ARE IN MICROFARADS, 1 OR GREATER ARE IN PICOFARADS.

92CL-22726R1

Fig. 6 – Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3121G and CA3170.

CA3123E

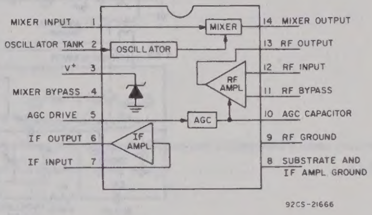
AM Radio Receiver Subsystem

Includes RF Amplifier, IF Amplifier, Mixer, Oscillator, AGC Detector, and Voltage Regulator

The CA3123E* is a monolithic silicon integrated circuit that provides an rf amplifier, if amplifier, mixer, oscillator, AGC detector, and voltage regulator on a single chip. It is intended for use in super-heterodyne AM radio receiver applications particularly in automobiles. The CA3123E is supplied in a 14-lead dual-in-line plastic package and operates over the temperature range of -55° to $125^{\circ}C$.

Features:

- **Low-noise, low-R_b' rf stage in cascode connection — eliminates Miller-Effect regeneration and allows controlled power rise by the choice of external components**
- **Mixer-oscillator stage with internal feedback — eliminates need for tapped or multi-winding oscillator coils**
- **Cascode if amplifier with controlled output impedance and negligible Miller Effect — eliminates regeneration and selectivity skewing**
- **Frequency-counter AGC circuit — allows control of AGC response by selection of the coupling capacitor**
- **Integral regulation with built-in surge protection**
- **Separately accessible amplifiers**



Terminal assignment diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
At Terminal No. 3 (V^+)	9 V
At Terminal No. 6 (IF Output)	40 V
At Terminal No. 13 (RF Output)	20 V
At Terminal No. 14 (Mixer Output)	20 V
DC CURRENT:	
Into Terminal No. 3 (V^+)	35 mA
DEVICE DISSIPATION:	
Up to $T_A = 55^{\circ}C$	750 mW
Above $T_A = 55^{\circ}C$	derate linearly 6.67 mW/$^{\circ}C$
AMBIENT TEMPERATURE RANGE:	
Operating	-55 to $+125^{\circ}C$
Storage	-65 to $+150^{\circ}C$
LEAD TEMPERATURE (During Soldering):	
At distance 1/16" ± 1/3" (1.59 mm ± 0.79 mm) from case for 10 s max.	$265^{\circ}C$

ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Static Characteristics In Circuit of Fig. 3						
DC Voltage:						
At Terminals 1, 4	V_1, V_4			4.7		V
At Terminals 2, 3, 14	V_2, V_3, V_{14}			6.8		V
At Terminal 5	V_5			0.25		V
At Terminal 6	V_6			12		V
At Terminal 7	V_7			0.76		V
At Terminals 8, 9	V_8, V_9			0		V
At Terminals 10, 11	V_{10}, V_{11}			0.71		V
At Terminal 12	V_{12}			0.71		V
At Terminal 13	V_{13}			4.0		V
DC Current:						
Into Terminals 1, 4, 5, 7 8, 9, 10, 11, 12	$I_1, I_4, I_5, I_7, I_8, I_9, I_{10}, I_{11}, I_{12}$			0		mA
Into Terminal 2	I_2			1.2		mA
Into Terminal 3	I_3			15		mA
Into Terminal 6	I_6			4.3		mA
Into Terminal 13	I_{13}			4.5		mA
Into Terminal 14	I_{14}			0.170		mA
Performance Characteristics In Circuit of Fig. 3						
Sensitivity		Input Signal to Dummy Antenna at f_{IN}=1 MHz, 30% AM Modulation at f_{MOD}=400 Hz, for 11 mV output at V_O	–	2.3	5	μV
Signal-to-Noise Ratio	S/N	Ratio of Output at V_O with Modulation ON and then OFF, Input Signal=100 μV, 30% AM Modulation at f_{MOD}=400 Hz	34	43	–	dB
Overload Distortion		Input Signal set at 1 MHz, 90% AM Modulation, Distortion at V_O must be $\leq$ 10%	160000	400000	–	μV

Dynamic Characteristics For Indicated Stages In Circuit of Fig. 3

Stage	Parallel Capacitance		Parallel Resistance		Transconductance
	Input pF	Output pF	Input Ω	Output Ω	μmhos
RF Amplifier	80	6	750	2×10^6 min.	140000
IF Amplifier	35	3.5	950	10^4	80000
Mixer	6	2	2000	2×10^6 min.	2500 (Mixer) 3000 (Amplifier)

* Formerly RCA Dev. No. TA6155

TYPICAL CHARACTERISTICS

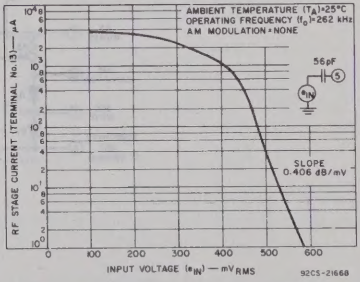


Fig. 1 – Control of RF stage by signal into Terminal No.5.

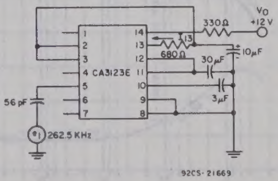
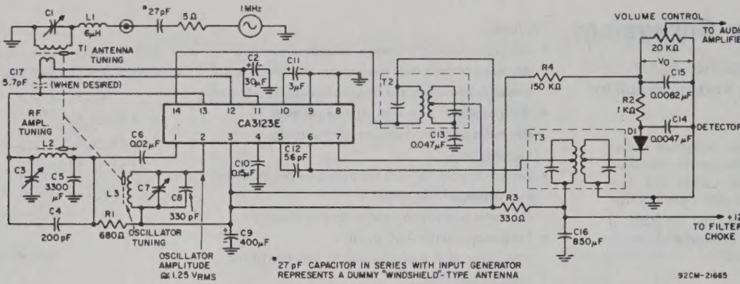


Fig. 2– Test circuit for Fig. 1.



*27 pF CAPACITOR IN SERIES WITH INPUT GENERATOR REPRESENTS A DUMMY "WINDSHIELD"-TYPE ANTENNA

92CM-21665

Transformer	Symbol	Frequency	Inductance µh (≈)	Capacitance pF (≈)	Q (≈)	Total Turns To Tap Turns Ratio	Coupling
First IF: Primary	T_2	262 kHz	2840	130	60	none	
Secondary			2840	130	60	or 30:1 31:1	critical ≈0.017 ≈ 1/Q
Second IF: Primary	T_3	262 kHz	2840	130	60	8.5:1	–
Secondary			2840	130	60	8.5:1	critical ≈0.017 ≈ 1/Q
Antenna: Primary	T_1	1 MHz	195	(C_1)–130	65		
Secondary		Adjusted to an impedance of 75 Ω with primary resonant at 1 MHz. Coupling should be as tight as practical. Wire should be wound around end of coil away from tuning core.					
Coils	L_1	7.9 MHz	6		50		
	L_2	1 MHz	55		50		
	L_3	1.262 MHz	41		40		

Fig. 3– Schematic diagram of AM radio receiver using CA3123E.

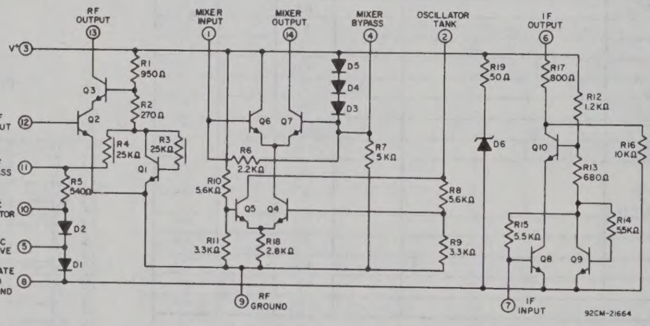
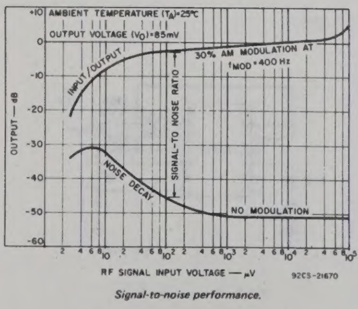


Fig. 4 – Schematic diagram of CA3123E.

PERFORMANCE CHARACTERISTICS IN CIRCUIT OF FIG. 3



Signal-to-noise performance.

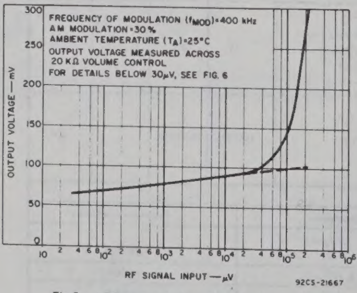


Fig.6 – AGC curve showing voltage rise (controlled by external capacitance of 5.7 pF: C_{17}, Fig.3).

Change in slope in the vicinity of 40000 µV signal input voltage is the result of the use of C_{17} (5.7 pF) in Fig.3. The dotted curve indicates expected performance if C_{17} = 0.

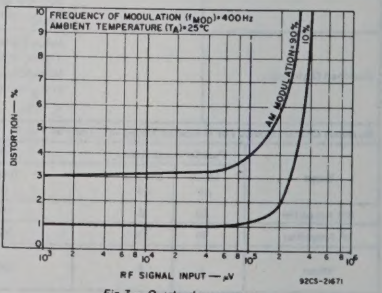


Fig.7 – Overload response.

Television Chroma Demodulator

RCA-CA3125E is a monolithic silicon integrated-circuit chroma demodulator having three separate demodulators with independent phase control. It is designed to function compatibly with the CA1398E IC Chroma Processor as well as other commercially available Chroma Processors in R-G-B Systems of color-TV receivers. The CA3125E is supplied in a 14-lead dual-in-line plastic package.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^\circ C$*

SUPPLY VOLTAGE	25 V
SUPPLY CURRENT	20 mA
AMBIENT-TEMPERATURE RANGE:	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

Features:

- **Luminance input**
- **Blanking control input**
- **Three separate demodulators with independent phase control**
- **Low output offset voltage . . . . 0.4 V**

TYPICAL STATIC CHARACTERISTICS AT $T_A = 25^\circ C$, $V^+ = +20$ VOLTS

SUPPLY CURRENT	9.6 mA
BRIGHTNESS CONTROL VOLTAGE: Measured with 8 volts at Terminals 11, 12, and 13	1.4 V
MAX. OUTPUT DIFFERENCE VOLTAGE: Measured between any two of Terminals 11, 12, and 13	±0.4 V
MAXIMUM DC DETECTOR UNBALANCE VOLTAGE: DC voltage shift on Terminals 11, 12, and 13 when Terminals 1, 2, and 3 are alternately biased 0.5 volt positive, then negative with reference to Terminal 14	+150 mV

TYPICAL DYNAMIC CHARACTERISTICS AT $T_A = 25^\circ C$, $V^+ = +20$ volts

BLUE CHROMA GAIN: Peak-to-peak voltage at Terminal 11 with 1.0 volt peak-to-peak applied differentially between Terminals 6 and 7, and with a subcarrier injection voltage of 1 volt peak-to-peak	7.36 Vp-p
RED GAIN RATIO: $\frac{\text{Peak-to-peak voltage at Terminal 13}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100$	100%
GREEN GAIN RATIO: $\frac{\text{Peak-to-peak voltage at Terminal 12}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100$	30%
LUMINANCE GAIN: Peak-to-peak voltage measured at Terminals 11, 12, and 13, with a peak-to-peak voltage of 0.1 volt applied to Terminals 6 and 7 (common mode), and with no subcarrier injection	0.7 Vp-p

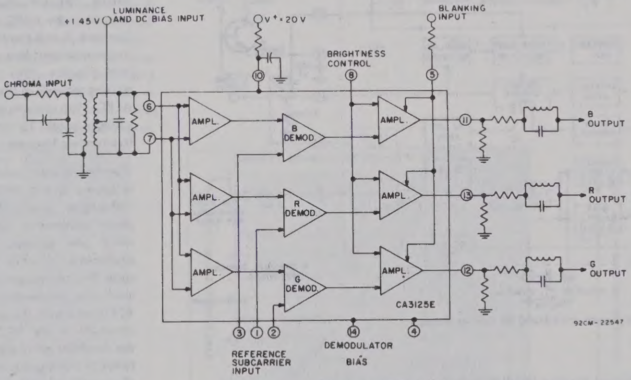


Fig. 1 – Functional block diagram of the CA3125E.

CA3126Q

TV Chroma Processor

RCA-CA3126Q is a monolithic silicon integrated circuit designed for chroma processing applications in color TV receivers. It is compatible with the CA3067 chroma demodulator as well as other chroma demodulators.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DEVICE DISSIPATION:
Up to $T_A = 55^oC$ .... 750 mW
Above $T_A = 55^oC$ .... derate linearly 7.9 mW/°C
DC SUPPLY VOLTAGE (Across Terms. 5 and 12)▲ .... 13.2 V
DC CURRENT:
Into Term. 12 .... 38 mA
Into Term. 14 .... 20 mA
DC VOLTAGE (Terminal 9):
Negative Rating .... −5 V
Positive Rating .... 3 V
AMBIENT TEMPERATURE RANGE:
Operating .... −40 to +85°C
Storage .... −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At a distance not less than 1/32 in. (0.79 mm)
from case for 10 seconds max. .... +265°C

▲This rating does not apply when using the internal zener reference in conjunction with an external pass transistor.

The CA3126Q is supplied in the 16-lead quad-in-line plastic package.

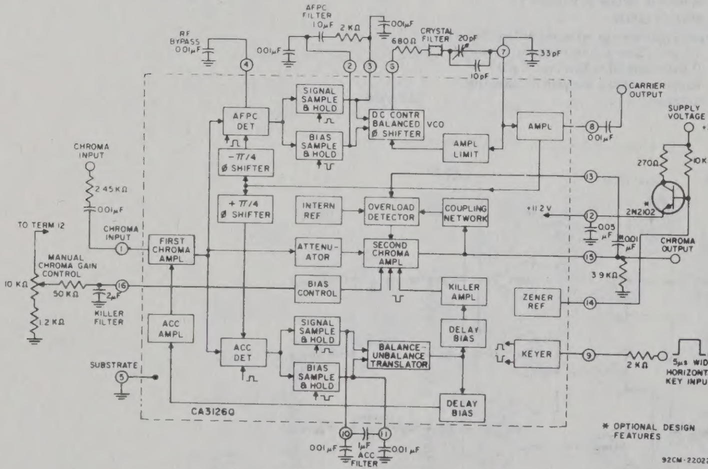


Fig. 1 – Block diagram of CA3126Q TV Chroma Processor.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, chroma control at maximum position for all characteristics tests except for chroma output test. For this test, control should be set at minimum position. Electrical characteristics referenced to test circuit, Fig.2.

CHARACTERISTIC	TERMINAL, MEASURE-MENT, AND SYMBOL	SWITCH POS.		CHROMA INPUT TP1	LIMITS			UNITS
		S1	S2		Min.	Typ.	Max.	
Static Characteristics								
Voltage Regulator	V_{12}	2	2	0	10.1	11.2	12.1	V
Supply Current	I_{12}	2	2	0	16	25	38	mA
Dynamic Characteristics (See Note 1)								
Pull-in Range*	V_8	*	2	0.5 $V_{p\text{-}p}$	±250	–	–	Hz
Oscillator Output	V_8	2	2	0	0.6	1.0	–	$V_{p\text{-}p}$
100% Chroma Output	V_{15}	1	2	0.5 $V_{p\text{-}p}$	1.4	2.7	–	$V_{p\text{-}p}$
Overload Detector	V_{15}	1	1	0.5 $V_{p\text{-}p}$	0.4	–	0.7	$V_{p\text{-}p}$
Minimum Chroma Output	V_{15}	1	2	0.5 $V_{p\text{-}p}$	–	–	20	$mV_{p\text{-}p}$
200% Chroma Output	V_{15}	1	2	1 $V_{p\text{-}p}$	70	100	140	% of 100% reading
20% Chroma Output	V_{15}	1	2	0.1 $V_{p\text{-}p}$	40	–	105	
Kill Level	V_{TP1}	1	2	vary	5	–	60	$mV_{p\text{-}p}$

Note 1 Except for pull-in range testing, tune oscillator trimmer capacitor for free-running frequency of 3.579545 MHz ± 10 Hz.
*Set Switch 1 to Position 2, detune oscillator ± 250 Hz, set Switch 1 to Position 1, and check for oscillator pull-in.

Features:

- **Phase-locked subcarrier regeneration utilizes sample-and-hold techniques**
- **Automatic chrominance control (ACC)/killer detector employs sample-and-hold techniques**
- **Supplementary ACC with an overload detector to prevent oversaturation of the picture tube**
- **Sinusoidal subcarrier output**
- **Keyed chroma output**
- **Emitter-follower buffered outputs for low output impedance**
- **Linear dc saturation control**
- **Internal zener-regulated reference potentials**
- **Only the initial crystal filter tuning is required. . . no killer or ACC adjustments required at any time**
- **Few external components required**
- **Compensation for temperature and supply variations**
- **All terminals protected against short circuits**

CIRCUIT DESCRIPTION

The following paragraphs briefly describe the circuit operation of the CA3126Q (shown in Fig. 1). A detailed description of the operation of various portions of the CA3126Q is given in ICAN-6247, "Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Techniques".

The chroma input is applied to Terminal 1 through the desired band-shaping network. A 2,450-ohm resistor should be placed in series with Terminal 1 to minimize oscillator pickup in the first chroma amplifier. This amplifier supplies signals to the second chroma amplifier and to the ACC and AFPC detectors. The first chroma amplifier is gain-controlled by the ACC amplifier.

A horizontal keying pulse is applied to Terminal 9. This pulse must be present to ensure proper operation of the oscillator circuit. The subcarrier burst is sampled during the keying interval in the AFPC detector. The error voltage, produced at Terminal 2 and proportional to the burst phase, is compared to the quiescent bias voltage at Terminal 3 by the sample-and-hold circuitry. This "compared" voltage controls the phase-shifting network in the phase-locked loop. The operation of the AFPC loop is independent of any external adjustments or voltages except for an initial capacitor adjustment to set the free-running frequency.

The regenerated oscillator signal at Terminal 8 is applied internally to the AFPC and ACC detectors through +45- and −45-degree phase-shifter networks to establish the proper phase relationship for these detectors. The ACC detector, which also samples the burst during the keying interval, produces a correction voltage proportional to the burst amplitude. The correction voltage is compared to the quiescent bias level using sample-and-hold circuitry similar to that used in the AFPC portion of the circuit. The "compared" voltage is applied internally to the ACC amplifier and killer amplifier. Because the amplifier gains and killer threshold are determined by the ratios of the internal resistors, these functions are independent of external voltages or controls.

The attenuated chroma signal is fed to the second chroma amplifier, where the burst is removed by keyer action. The killer amplifier, the chroma gain control, and the overload detector control the action of the second chroma amplifier, whose gain is proportional to the dc voltage at Terminal 16. The overload detector (Terminal 13) receives a sample of the chroma output (Terminal 15) and detects the peak of the signal. The detected voltage is stored in an external capacitor connected to Terminal 16. This stored voltage on Terminal 16 affects the gain of the second chroma in the same manner as the chroma gain control.

APPLICATIONS INFORMATION

General Considerations

The block diagram shown in Fig. 1 is typical of the type of circuit used in the practical application of the CA3126Q. Several items are critical for proper operation of the circuit.

1. A series resistor of approximately 2,450 ohms (or high source impedance) must be used at the chroma input, Terminal 1. This high impedance minimizes pickup of unbalanced currents, particularly of the subcarrier oscillator signal.

2. When the overload detector is used, a large resistor (nominally 47,000 ohms) must be placed in series with Terminal 16 to set the required RC time constant. The same RC network series serves to set the killer time constant.
3. The setting of the free-running oscillator frequency requires the presence of the keying pulse. The free-running frequency will be erroneous if Terminal 1 is dc shorted during the setting operation because of the dc offset voltage introduced to the AFPC detector.
4. Care must be taken in PC board designs to provide reasonable isolation between the oscillator portion of the circuit (Terminals 6, 7, and 8) and the chroma input (Terminal 1).

Overload Detector

The overload detector accomplishes two purposes:

1. It prevents oversaturation due to low burst-to-chroma ratios.
2. It prevents overload conditions due to noise.

Both of these conditions are discussed in more detail in ICAN-6247. The extent to which the overload detector is used depends upon the individual receiver design goals. If greater than 0.5-volt peak-to-peak output is desired, the chroma output at Terminal 15 can be tapped to yield any desired degree of overload detector action.

Chroma Gain Control

The chroma gain control operates by varying the base bias on current source transistor Q25. To ensure proper temperature tracking of the chroma gain control, it is essential that the control be operated from a supply source derived from the reference voltage at Terminal 12. Because the control operates from a current source, chroma gain is much more predictable and far less temperature sensitive than controls that steer current by means of a differential amplifier. The typical chroma gain characteristic for the CA3126Q is shown in Fig. 3.

Subcarrier Regenerator Oscillator

The oscillator filter consists of a 3.579545-MHz crystal, a 680-ohm resistor, and a 10-pF capacitor connected in series across Terminals 6 and 7. A 33-pF capacitor, shunt connected from Terminal 7 to ground, rolls off higher-order harmonics, thereby preventing oscillation at the crystal third-harmonic frequency. A curve of the typical static phase error as a function of the free-running oscillator frequency is shown in Fig. 4. It should be noted that the slope of the curve determines the dc gain of the phase-locked loop, i.e., 40 Hz per degree.

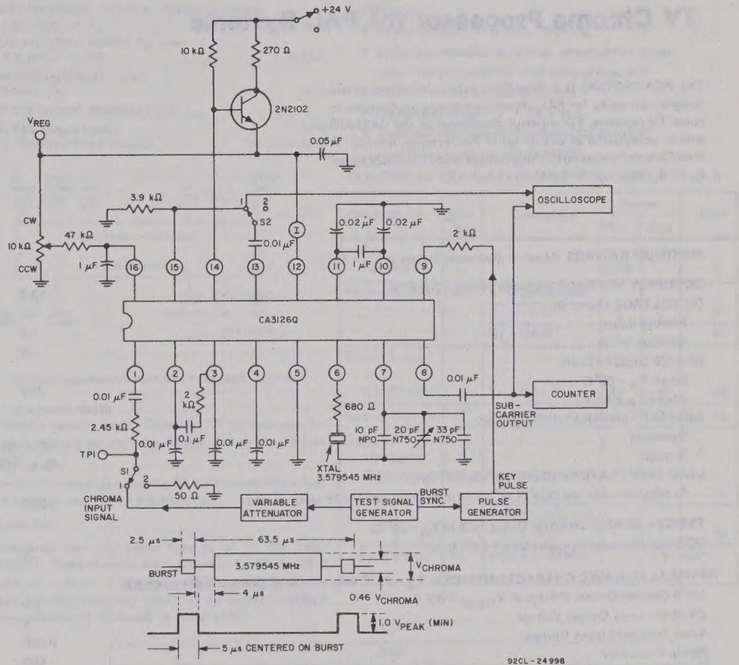


Fig. 2–Test circuit for CA3126Q.

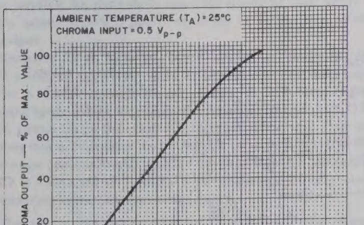


Fig. 3 –Chroma gain control.

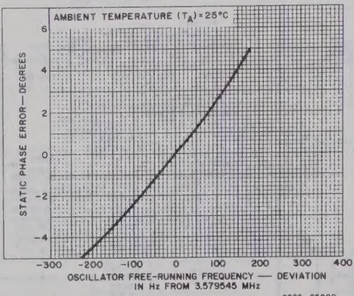


Fig. 4–Static phase error.

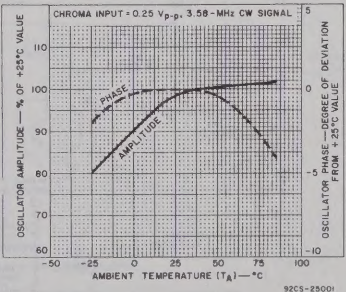


Fig. 5–Amplitude and phase variations of oscillator output vs. temperature.

Thermal Considerations

The circuit of the CA3126Q is thermally compensated to achieve the optimal operating characteristics over the normal operating temperature range of TV receivers. Figs. 5 and 6 show the oscillator- and chroma-output amplitudes and phases as a function of temperature (Terminals 8 and 15), respectively. Both the oscillator- and chroma-output amplitudes and phases are measured relative to the chroma-input phase. The performance of the oscillator free-running frequency as a function of temperature is shown in Fig. 7. All the temperature plots are characteristic of the test circuit with the indicated component types and values given in Fig. 2.

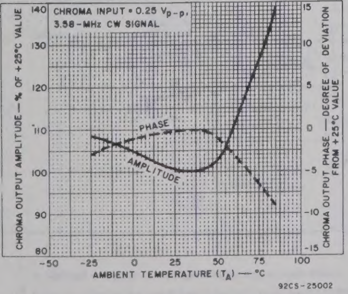


Fig. 6–Amplitude and phase variations of chroma output vs. temperature.

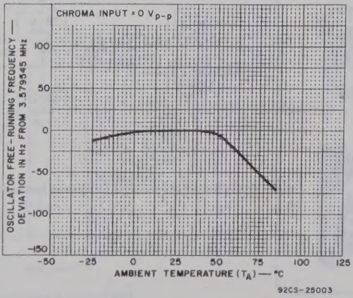


Fig. 7–Variation of oscillator free-running frequency vs. temperature.

CA3128Q

Preliminary Data

TV Chroma Processor for PAL Systems

The RCA-CA3128Q is a monolithic silicon integrated circuit designed primarily for PAL chroma processing applications in color TV receivers. For a circuit description of the CA3128Q and an explanation of this device in PAL systems, refer to "A New Chroma Processing IC Using Sample -and-Hold Techniques" by L. A. Harwood (ST6144).

Features:

- Phase-locked subcarrier regeneration utilizes sample-and-hold techniques in the automatic frequency phase control (AFPC) servo loop
- Automatic chrominance control (ACC)/ killer detector employs sample-and-hold techniques
- Supplementary ACC with an overload detector to prevent oversaturation of the picture tube
- Sinusoidal subcarrier output
- Keyed chroma output
- Emitter-follower buffered outputs for low output impedance
- Linear dc saturation control
- PAL identification output
- Only the initial crystal filter tuning is required . . . no killer and ACC adjustments required at any time
- Few external components required
- Compensation for temperature and supply variations
- All terminals protected against short circuits

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC SUPPLY VOLTAGE (Between Terms. 12 and 5)	13.2	V
DC VOLTAGE (Term. 9):		
Positive Value	+3	V
Negative Value	−5	V
DEVICE DISSIPATION:		
Up to T_A = 55°C	750	mW
Above T_A = 55°C	derate linearly at 7.9 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):		
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

TYPICAL STATIC CHARACTERISTICS at T_A = 25°C:

DC Supply Current (I_{12})with V_{12} = 11.2 V dc	25	mA

TYPICAL DYNAMIC CHARACTERISTICS at T_A = 25°C with a Burst-to-Chroma Ratio of 46.5%:

100% Chroma Output Voltage at $V_{I\,(p\text{-}p)}$ = 0.5 V	3.5	Vp-p
Oscillator-Level Output Voltage	1	Vp-p
Killer Threshold Input Voltage	0.018	Vp-p
Pull-in Frequency	500	Hz
PAL Identification Output Voltage	1	Vp-p

The CA3128Q is supplied in the 16-lead quad-in-line plastic package.

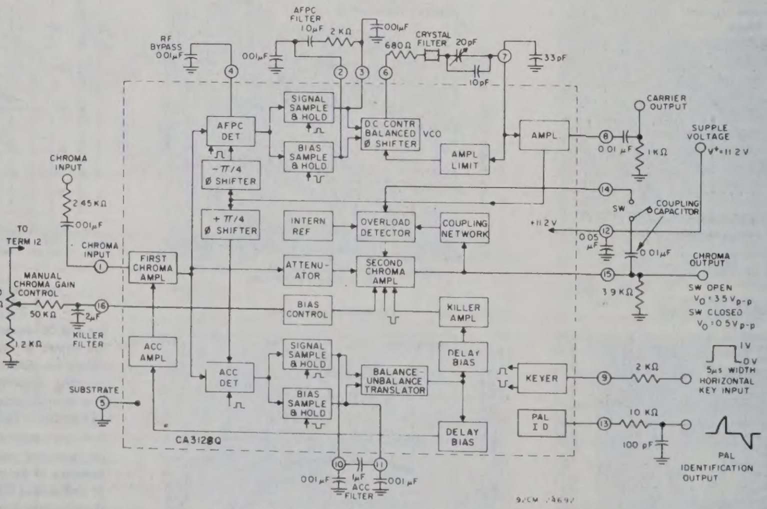


Fig. 1 – Block diagram of CA3128Q TV Chroma Processor.

CA3131EM, CA3132EM

5-Watt Audio Amplifiers

With Integral Heat Sink

RCA-CA3131EM and CA3132EM are audio amplifiers with integral preamplifier stages on single integrated-circuit monolithic chips.

Utilizing a uniquely designed package with an integral heat sink, these devices can provide a power-output signal in excess of five watts at an ambient temperature of 25°C.

The CA3131EM employs an internal feedback network that sets the over-all gain of the amplifier to typically 48 dB.

The CA3132EM omits the internal feedback network. This arrangement offers the circuit designer a wide latitude in the choice of an external feedback network more suitable to a specific application.

Both types are encapsulated in a 16-lead dual-in-line plastic package with 4 center leads removed.

The CA3131EM and CA3132EM are electrically equivalent to and pin compatible with types SN76013 and SN76023, respectively.

Determining External Component Values (Refer to Figs. 2 & 3)

The dc quiescent output voltage is set by the voltage at Terminal 1. This voltage, in turn, is set by the internal voltage at Terminal 2 less I_I (input current, fixed by $R_A + R_B$, for Q4). The voltage at Terminal 2 is set slightly above half the supply voltage to allow for the voltage drop across $R_A + R_B$. Filter R_BC3 attenuates any ac ripple injected from the supply line and prevents positive feedback to Terminal 1. The rejection of supply voltage is a direct function of the filter attenuation.

The input impedance of the audio amplifiers is a function of the closed-loop gain and the magnitude of the Q8 current. In practice the input impedance is well above 1 megohm. The input signal, applied through C2, sees an impedance equivalent to the resistance of R_A connected in parallel with the amplifier input impedance. Hence, the value of R_A in most cases is dominant in establishing the input signal impedance.

The value of C1 depends on the regulation of the power supply. It is possible for the amplifier to work with a value of C1 as low as 0.1 μF to attenuate high-frequency signals in the supply line. Ideally, C1 should be placed as near Terminal 10 as possible. An electrolytic capacitor should be used for C1 if the power supply is poorly regulated to avoid ripple at the output.

Capacitor C6 at Terminal 15 provides over-all compensation. If a 1000-pF capacitor is used for C6, then the first breakpoint for a 46-dB closed-loop gain occurs at 200 kHz. Higher capacitance values will cause the constant current from Q10 to charge C6 on the positive voltage swing and thus limit the slew rate at high-signal levels. Because p-n-p transistor Q19 has a lower gain-bandwidth product (f_T) than the n-p-n transistors, C7 is connected to Terminal 9 to compensate for gain losses occurring in the negative voltage swings.

The use of the filter networks C8 and R_D at the output Terminal 6 is a standard requirement for class B audio outputs driving reactive speaker loads. Capacitor C8 compensates for the speaker inductance and R_D limits the current surges through C8.

The value of the coupling capacitor C9 to the load determines the low-frequency response of the amplifier.

Closed-Loop Gain

The closed-loop gain for either type is set by the ratio (R1 + R2)/R1. These resistors are included in the CA3131EM circuit and are external when used with the CA3132EM. In either type, the low-frequency value (−3 dB point) is reached when the impedance of C5 equals the value of R1.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE, V^+ .... 28 V

CONTINUOUS OUTPUT POWER, P_O (with R_L = 8 Ω and V^+ = 24 V) .... 8 W RMS

MINIMUM RECOMMENDED LOAD IMPEDANCE, R_L .... 8 Ω

AMBIENT OPERATING TEMPERATURE, T_A (at 6 W RMS Output Power) .... 70 °C

STORAGE TEMPERATURE RANGE .... −55 to +150 °C

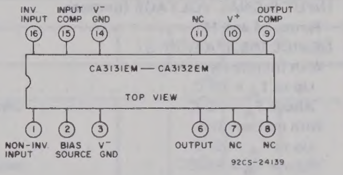


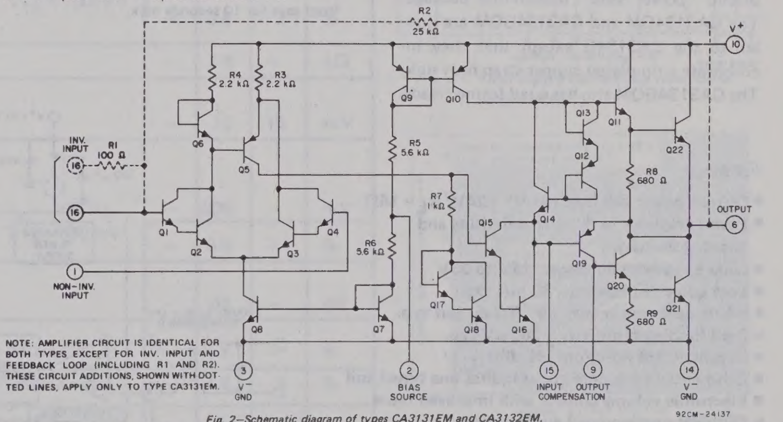
Fig. 1–Terminal assignment of the CA3131EM and CA3132EM.

Features:

- Power Output: 4 W min., 5 W typ.
- Complete amplifier including: preamplifier stages, power-output amplifier, and integral heat sink
- High power-supply rejection ratio
- Operating voltage: V^+ = 24 V typ.
- Available with internal feedback (CA3131EM) or without feedback (CA3132EM)

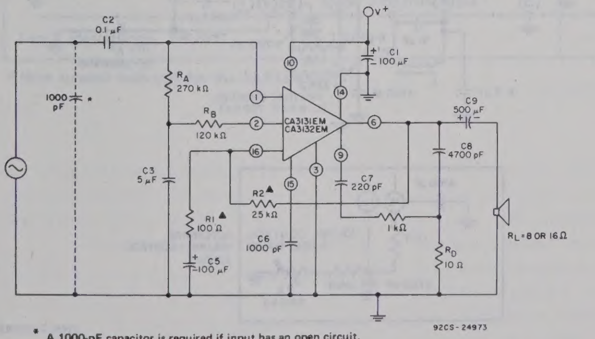
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 24 V

Characteristic	Symbol	Conditions	Values		Unit
			Min.	Typ.	
Input Impedance	Z_I		200k	–	Ω
Power Output	P_O	At clipping onset			
		R_L = 8 Ω	4	–	W
		R_L = 16 Ω	3	–	W
Closed-Loop Gain – CA3131EM	A	f = 1 kHz	46	48	dB
Supply Current	I^+	Zero signal	–	10	mA
Total Harmonic Distortion	THD	P_O = 50 mW–4 W, R_L = 8 Ω	–	1	%
		P_O = 50 mW–3 W, R_L = 15 Ω	–	1	%
Noise Voltage	V_n	f=20 Hz–20 kHz	–	1.5	mV RMS



NOTE: AMPLIFIER CIRCUIT IS IDENTICAL FOR BOTH TYPES EXCEPT FOR INV. INPUT AND FEEDBACK LOOP (INCLUDING R1 AND R2). THESE CIRCUIT ADDITIONS, SHOWN WITH DOTTED LINES, APPLY ONLY TO TYPE CA3131EM.

Fig. 2–Schematic diagram of types CA3131EM and CA3132EM.



* A 1000-pF capacitor is required if input has an open circuit.

▲ External resistors R1 and R2 are used only with the CA3132EM. When testing the CA3131EM, omit R1 and R2 and connect the (+) termination of C5 to Terminal 16.

Fig. 3–Test circuit for types CA3131EM and CA3132EM.

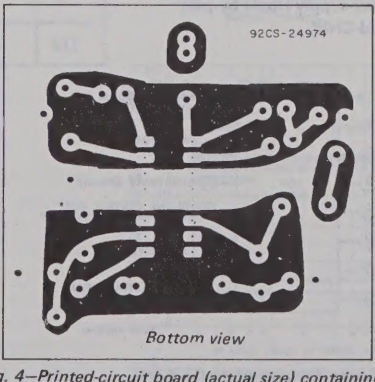


Fig. 4–Printed-circuit board (actual size) containing the test circuit, shown in Fig. 3, for the CA3131EM.

CA3134G, CA3134GM, CA3134GQM

TV Sound IF and Audio Output Subsystems

The RCA-CA3134 combines the sound if and audio output subsystems on a single monolithic integrated circuit to provide a television sound system for color or black and white applications. Each device includes a multistage if amplifier-limiter, and fm detector, and an audio power amplifier that is designed to drive an 8-, 16-, or 32-ohm speaker.

The CA3134 is supplied in the hermetic Gold-CHIP, which is of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure. This hermetic chip is encapsulated in a 16-lead plastic "power stud" dual-in-line package, which has an inherently low junction-to-case (stud) thermal resistance. This package lends itself to a wide variety of heat-sink methods, depending on the application requirements.

The CA3134G is supplied in the 16-lead plastic "power stud" dual-in-line package. The CA3134GM and CA3134GQM are similar to the CA3134G except that they incorporate a tin-plated copper-strap heat sink. The CA3134GQM also has quad-formed leads.

Features:

- Output power 3W (typ.) at $V^+ = 24V$, $R_L = 16\Omega$
- Power amplifier with current limiting and thermal shutdown
- Wide power-supply range: 12V to 33V
- Low quiescent current: 30 mA typ.
- 5-kHz deviation sensitivity: 1W output typ.
- 3-dB limiting sensitivity: 200 μV typ.
- Excellent AM rejection: 50 dB typ.
- Differential peak detector—requires one tuned coil
- Electronic volume control with improved taper
- Optional unattenuated audio output
- Optional power-supply ripple by-pass
- Hermetic Gold-CHIP

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		CA3134G	CA3134GM, CA3134GQM	
DC SUPPLY VOLTAGE (Between Term. 1, V+ and Terms.4, audio-output ground and 13, substrate)		33	33	V
INPUT SIGNAL VOLTAGE (Between Terms. 14 and 15)		±3	±3	
DEVICE DISSIPATION:				
With Infinite Heat Sink—				
Up to $T_A = 70°C$		6.5	–	
Above $T_A = 70°C$	derate linearly	83.3	–	mW/°C
With no Heat Sink—				
Up to $T_A = 25°C$		1.4	–	W
Above $T_A = 25°C$	derate linearly	11.1	–	mW/°C
With Copper-Strap Heat Sink—				
Soldered to PC Board				
Up to $T_A = 25°C$		–	3.9	W
Above $T_A = 25°C$	derate linearly	–	31.2	mW/°C
Unsoldered				
Up to $T_A = 25°C$		–	2.5	W
Above $T_A = 25°C$	derate linearly	–	20	mW/°C
THERMAL RESISTANCE				
Junction to Stud		12	12	°C/W
AMBIENT TEMPERATURE RANGE:				
Operating		–40 to +85		°C
Storage		–65 to +150		°C
LEAD TEMPERATURE (During Soldering):				
At a distance 1/16 in. ±1/32 in. (1.59 ±0.79 mm) from case for 10 seconds max.		+265		°C

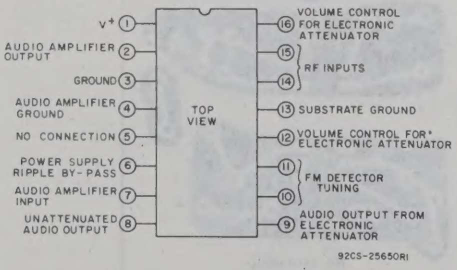

V+ ①
AUDIO AMPLIFIER OUTPUT ②
GROUND ③
AUDIO AMPLIFIER GROUND ④
NO CONNECTION ⑤
POWER SUPPLY RIPPLE BY-PASS ⑥
AUDIO AMPLIFIER INPUT ⑦
UNATTENUATED AUDIO OUTPUT ⑧
TOP VIEW
⑯ VOLUME CONTROL FOR ELECTRONIC ATTENUATOR
⑮ ⑭ RF INPUTS
⑬ SUBSTRATE GROUND
⑫ VOLUME CONTROL FOR ELECTRONIC ATTENUATOR
⑪ ⑩ FM DETECTOR TUNING
⑨ AUDIO OUTPUT FROM ELECTRONIC ATTENUATOR
92CS-25650R1

Fig. 1 – Terminal diagram of the CA3134G, CA3134GM, and CA3134GQM.

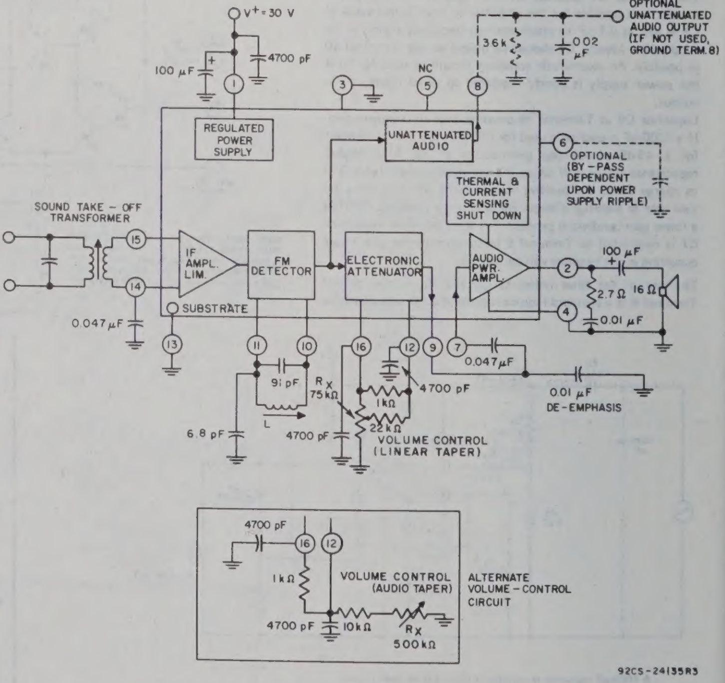


Fig. 2 – Block diagram of the CA3134 in a typical circuit application.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V^+ = +30$ V (applied to Term. 1), DC Volume Control, $R_X = 75$ kΩ, $R_L = 16$ Ω, unless otherwise indicated. Refer to Fig.2

CHARACTERISTIC	SPECIAL TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Static Characteristics					
Current into Term. 1, I_1	$P_O = 0$	15	30	45	mA
Dynamic Characteristics					
IF AMPLIFIER: Input Limiting Voltage, V_{15}(lim) (at −3 dB point)	$f_O = 45$ MHz $f_m = 400$ Hz $\Delta f = \pm 25$ kHz	–	200	400	μV
AM Rejection, AMR	$f_O = 4.5$ MHz, $f_m = 400$ Hz, Modulation Index = 0.3, $V_{15} = 20$ mV	40	50	–	dB
Input Resistance, R_I	$V_{15} = 35$ mV	–	25	–	kΩ
Input Capacitance, C_I	$V_{15} = 35$ mV	–	3	–	pF
DETECTOR: Recovered af Voltage (Term. 9), V_O(af)	$f_O = 4.5$ MHz, $f_m = 400$ Hz, $\Delta f = \pm 25$ kHz, $V_{15} = 100$ mV	–	700	–	mV
Total Harmonic Distortion, (THD)		–	0.8	3	%
Output Resistance, R_O	At Term. 9	–	7.5	–	kΩ
ATTENUATOR: Maximum Attenuation	$R_X = 0$	–	10	15	mV
UNATTENUATED AUDIO: Recovered af Voltage (Term. 8), V_O(af)	$f_O = 4.5$ MHz, $f_m = 400$ Hz, $\Delta f = \pm 25$ kHz, $V_{15} = 100$ mV	–	600	–	mV
Total Harmonic Distortion (THD)		–	0.8	–	%
AUDIO POWER AMPLIFIER: Voltage Gain, A(af)	f = 1 kHz	–	35	–	dB
System Total Harmonic Distortion THD (System)	$P_O = 1$ W ($I_T = 140$ mA typ.)	–	1.5	–	%
	$P_O = 2$ W ($I_T = 180$ mA typ.)	–	1.6	3	%
Power Output, P_O	THD (System) = 10% ($I_T = 210$ mA typ.)	–	5*	–	W
Input Resistance, (R_I(af)	f = 1 kHz	–	100	–	kΩ

* With suitable heat sink for the CA3134G.

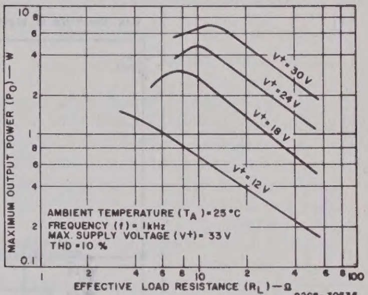


Fig. 3 – Maximum output power as a function of effective load resistance.

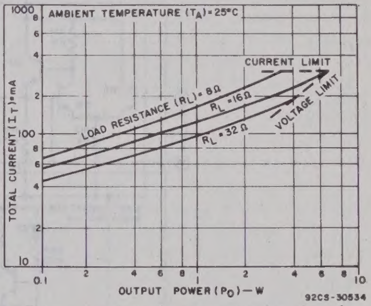


Fig. 4 – Total supply current as a function of output power.

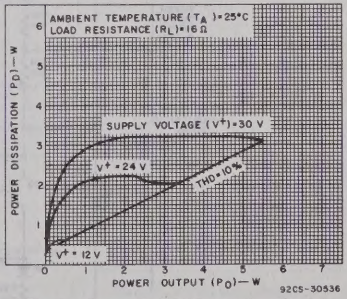


Fig. 5 – Power dissipation as a function of output power.

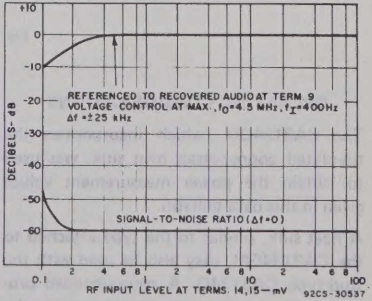
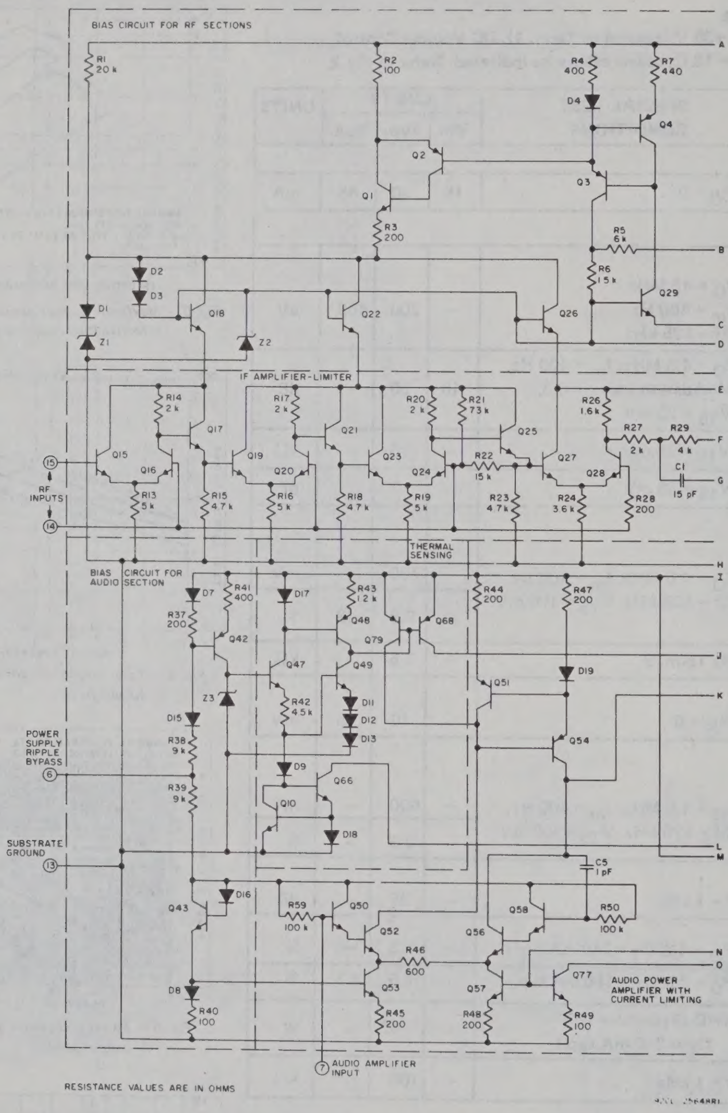


Fig. 6 – Recovered audio, and signal-to-noise ratio as a function of rf input level.



RESISTANCE VALUES ARE IN OHMS

Fig. 7 – Schematic diagram of the CA3134

OPERATING CONSIDERATIONS

The CA3134GM, which incorporates the tin-plated copper-strap heat sink, was used to obtain the power measurement values given in this data bulletin.

A heat sink, similar to the type attached to the CA3134GM, may also be used with the stud-type CA3134G. A recommended procedure for attaching the heat sink to the CA3134G is described as follows:

Apply a non-conductive epoxy (Uniset structural adhesive or equivalent) to the top side of the plastic package. Then apply a conductive epoxy (DuPont 5504A or equivalent) in the hole of the heat sink and around the stud projecting from the plastic package. To assure good thermal conduction, use sufficient conductive epoxy to allow the excess to be forced through the hole when the heat sink is fitted over the stud. Stress applied to the stud should be limited to less than 0.34 newton-meters (3 in-lb) of torque 66.7 newtons (15 lb) of tension, and 444.8 newtons (100 lb) of compression.

The assembly when soldered to a 7.6 cm (3 in.) x 10.2 cm (4 in.) PC board has an overall thermal resistance ($\theta_{\text{Junction-to-Ambient}}$) of 32°C/W.

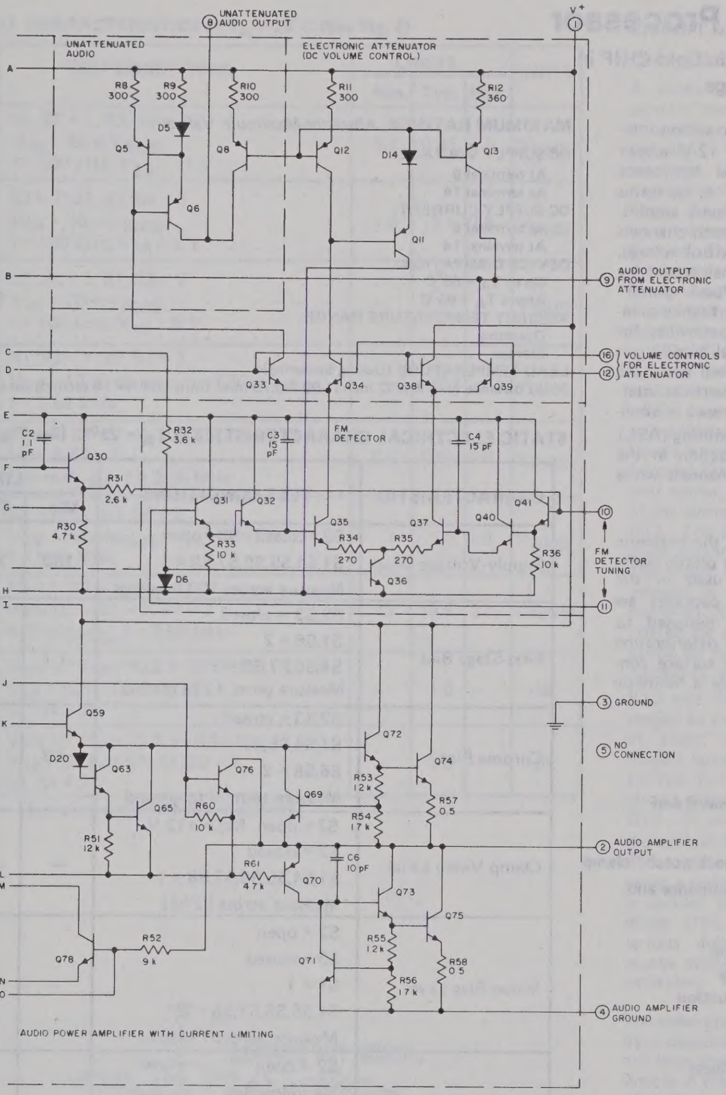


Fig.7 — Schematic diagram of the CA3134 .

CA3135G

TV Luminance Processor

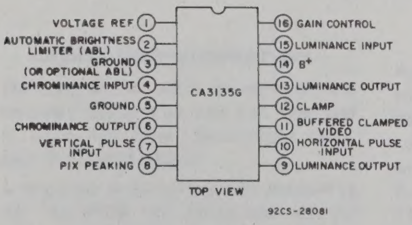
"G" Suffix Type — Hermetic Gold-CHIP in Dual-In-Line Plastic Package

The RCA-CA3135G monolithic silicon integrated circuit operates from a 12-V supply and is used as a low-level luminance processor in TV applications. It performs the function of video and chroma amplification and allows the gain of both channels to be adjusted with a single control voltage. The dc level of "black" is maintained by clamping the level of the "back porch" (black-level reference) of the blanking interval. This clamping feature provides for 100% dc restoration. Vertical blanking is applied to the luminance as well as to the chrominance channel so that vertical interval test signals (VITS) interference is eliminated. Automatic brightness limiting (ABL) is accomplished by gain reduction in the luminance and chrominance channels while maintaining black level.

The CA3135G is supplied in the hermetic Gold-CHIP 16-lead dual-in-line plastic package (G suffix). The chips used in the hermetic Gold- Chip plastic packages are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure.

System Features:

- **Single gain control for luminance and chrominance channels**
- **100% dc restoration with "back porch" clamp**
- **Vertical blanking of both luminance and chrominance channels**
- **Automatic brightness limiting**
- **Operates from a 12-V supply**
- **Hermetic Gold-CHIP construction**
- **Gold-CHIP metallization**
- **Silicon-nitride passivated**
- **Platinum-silicide ohmic contacts**



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
At terminal 9	28 V
At terminal 14	15 V
DC SUPPLY CURRENT:	
At terminal 9	30 mA
At terminal 14	50 mA
DEVICE DISSIPATION:	
Up to $T_A = 55^\circ C$	750 mW
Above $T_A = 55^\circ C$	Derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (See Fig. 3)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply-Voltage Drop	S2 = closed S3 = open S1,S4,S5,S6,S7,S8 = 1 Measure across 10 Ω resistor	130	215	300	mV
First-Stage Bias	S2,S3 = closed S1,S6 = 2 S4,S5,S7,S8 = 1 Measure term. 13 to ground	1.7	2.7	3.7	V
Chroma Bias	S2,S3 = closed S1,S4,S5,S7 = 1 S6,S8 = 2 Measure term. 6 to ground	7.3	8	9.1	V
Clamp Video Level	S2 = open Ref.= +12 V S3 = closed S1,S4,S5,S6,S7,S8 = 1 Measure across 82 kΩ	—	−8.7	—	V
Video Bias Level	S2 = open S3 = closed S1 = 1 S4,S5,S6,S7,S8 = 2 Measure across 1 kΩ	–	9	–	V
Luminance Blanking	S2 = open S3 = closed S1,S8 = 1 S4,S5,S6,S7 = 2 Measure across 1 kΩ	–	−50	–	mV
Chroma Blank	Setup same as above, measure term. 6	10.38	11.2	11.58	V
Chroma Input Impedance	Max. horizontal input = 10 V_{p-p} Max. vertical input = 2 V_{p-p}	–	2.5	–	kΩ
Chroma Output Impedance		–	150	–	Ω
Luminance Input Impedance		–	50	–	Ω
Luminance Output Impedance		–	10	–	kΩ

DYNAMIC ELECTICAL CHARACTERISTICS at T_A = 25°C (See Fig. 4)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Min. Video Gain	S1, S2 = 1; S3, S4 = 2 V_{IN} = 70 mV_{RMS}, f = 100 kHz, V_{16} = 12 V	0.2	0.35	0.5	V_{RMS}
Max. Video Gain	S2 = 1; S1, S3, S4 = 2 V_{IN} = 70 mV_{RMS}, f = 100 kHz, V_{16} = 0 V	1.6	2.1	2.6	V_{RMS}
Limited Video Gain	S2, S4 = 1, S1, S3 = 2 V_{IN} = 70 mV_{RMS}, f = 100 kHz, V_{16} = 0 V	–	0.3	–	V_{RMS}
Min. Chroma Gain	S1, S3 = 1; S2, S4 = 2; V_{16} = 12 V; chroma in = 530 mV_{RMS}, f = 3.58 MHz	–	0.095	–	V_{RMS}
Max. Chroma Gain	S3 = 1; S2 = 2, V_{16} = 0 V; chroma in; S1 = 2, S4 = 2 530 mV_{RMS}, f = 3.58 MHz	0.5	0.65	0.8	V_{RMS}
Video Freq. Response	S2 = 1, S1, S3, S4 = 2 V_{IN} = 70 mV_{RMS}; V_{16} = 0 V; f = 3.58 MHz	1	1.9	2.8	V_{RMS}
Chroma Phase Angle	S3 = 1; S2 = 2; V_{16} = 0 V; chroma in; S1 = 2, S4 = 2 530 mV_{RMS}, f = 3.58 MHz	12	19.5	27	Degrees
Chroma Gain with V^+ Variation	Vary V^+ from 10.8 V (REF.) to 13.2 V V_{16} = 50% of V^+; S1, S3 = 1 S2, S4 = 2	–	1.5	–	dB
Video Gain with V^+ Variation	Vary V^+ from 10.8 V (REF.) to 13.2 V V_{16} = 50% of V^+; S1, S2 = 1 S3, S4 = 2	–	1.5	–	dB

Typical max. luminance input before clipping (f = 100 kHz):

V_{16}	INPUT
+12 V	2.5 V_{p-p}
+6 V	0.75 V_{p-p}
0 V	0.45 V_{p-p}

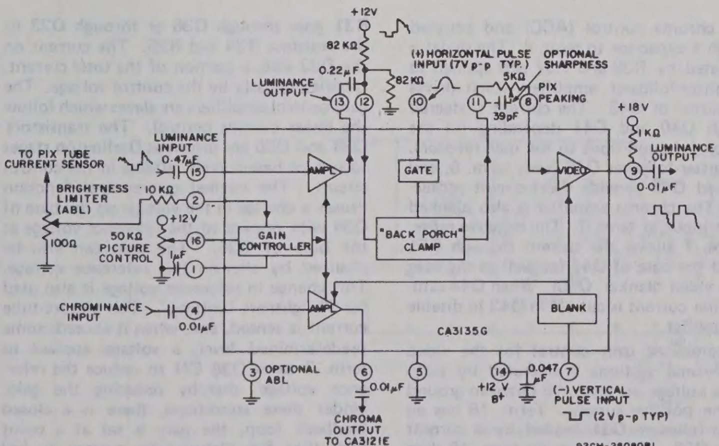


Fig. 1 — Block diagram.

CIRCUIT DESCRIPTION

(See fig. 2 for schematic diagram).

A video (luminance) signal from the receiver's "second detector" is coupled through a capacitor to term. 15 with sync-negative polarity. For purposes of the following amplifier, the level is clamped at the most negative point (sync tips) at the input (this is not the point at which the final "black"-level clamping, or dc restoration, is performed). The capacitor at term. 15 is charged on the most negative excursions of the signal by conduction of Q4. Positive signal excursions lift the emitter of Q4 into cutoff. The signal voltage on R3 develops a signal current in Q6. The current passes through Q7 and Q8, the division of current depends on the condition of the gain-adjusted signal voltage on the load resistors (discussed below). The gain-adjusted signal voltage on the load resistors is converted to current by the emitter-follower Q14 into R9, and fed into the current mirror, Q15, Q16, and Q17. The output of the current mirror develops a voltage across R13. The dc level is shifted by withdrawing some current from the input to the mirror. The fixed dc-level shifting current is developed in R6 and its diode string and is mirrored in Q13. Because the dc level is altered by adjustment of the gain, compensating dc currents that depend on these adjustments are fed into the mirrors through R13 and R29. The compensations are arranged so that, as gain is varied, the dc level of "black" is approximately constant at the output term. 13. The output is driven by emitter follower Q18, which has a short-circuit pulldown protection circuit, R14 and Q19. A constant-current source Q20 loads the emitter-follower to prevent distortion in the emitter-follower that may result from using a resistive load. The constant current is derived by mirroring the current in the diode D23. The resistor R15 prevents serious interaction with another current source mirrored from this point in case Q20 saturates.

The video output signal at term. 13 is coupled by a capacitor to term. 12. The polarity has not been inverted by the first amplifier, and sync is in the negative direction at this point. Black-level clamping is accomplished by application of a flyback pulse to term. 10. Between pulse peaks, Q29 is not conducting, and the base of Q24 goes up to the supply voltage so that term. 12 can be at any voltage between ground and the supply. While the flyback pulse is positive, that is during the blanking interval, the base of Q24 is held at about 2.8 volts. The most positive signal excursion during that time will cause Q24 to conduct with the result that the capacitor feeding term. 12 is charged until the most positive point of the signal is just at the conduction point, about 3.5 volts. The most positive part of the signal *during blanking* is the "back porch" or black-level reference. During trace time, the signal swings more positive, but the dc level of black is preserved regardless of the levels

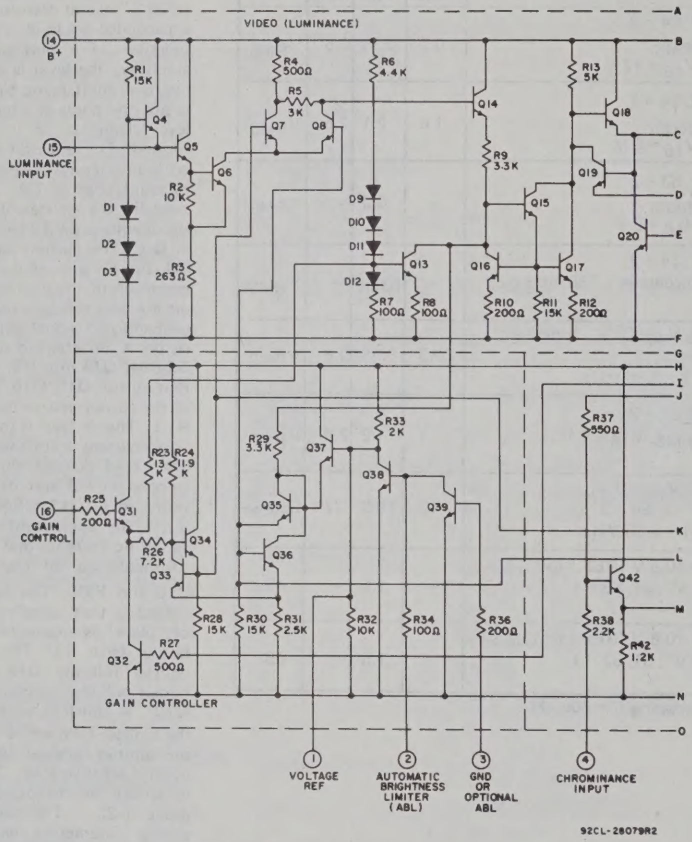


Fig. 2 – Schematic diagram

of sync or video signals. Term. 12 is a high-impedance point, and the emitter-follower Q26 is used to bring the signal out to term. 11.

The signal voltage at term. 11 is directly coupled through a resistor to term. 8, generating a current in term. 8. This current is amplified 10 times by the current mirror Q51, Q52, and Q53. Blanking during the vertical retrace interval is accomplished at Q50 via term. 7. Term. 7 is normally high enough to keep Q49 in saturation. A negative pulse from the vertical circuit cuts Q49 off, allowing some of the current through R51 to saturate Q50. When Q50 sinks the term. 8 input current, there is no output from term. 9 – as if the signal were blacker-than-black. The output current from term. 9 is used to drive the receiver's RGB matrix and the amplifiers that drive the picture tube.

The chrominance signal is taken from the first chroma amplifier following the automatic chroma control (ACC) and coupled through a capacitor to term. 4. The signal is attenuated by R38 and R37 and applied to an emitter-follower amplifier which drives the emitter of Q43. The current is steered through Q40 and Q41 depending on the gain-control conditions to the load resistors. An emitter-follower Q46 feeds term. 6, and R46 and Q45 provide short-circuit protection. The chroma amplifier is also blanked via the input at term. 7. The negative pulse at term. 7 allows the current through R51 to feed the base of Q44 (as well as the base of the video blanker, Q50). When Q44 saturates, the current is cut off in Q43 to disable the amplifier.

The combined gain control for the video and chroma sections is operated by varying the voltage on term. 16 between ground and the positive supply. Term. 16 has an emitter-follower Q31 loaded by a current source Q32. The voltage on term. 16 then determines whether the flow of current in R31 goes through Q36 or through Q33 to the resistors R24 and R26. The current on the Q33 side, a portion of the total current, is varied linearly by the control voltage. The gain-control amplifiers are slaves which follow the linear current control. The transistors Q34 and Q35 are driven as Darlington stages to reduce base-current effects in the control circuit. The normal gain-control function causes a change in the voltage on the base of Q34 with respect to the reference voltage at the base of Q35. The gain can also be changed by altering this reference voltage. This change in reference voltage is also used for "brightness limiting". The picture-tube current is sensed, and, when it exceeds some predetermined level, a voltage applied to term. 2 turns Q38 ON to reduce the reference voltage, thereby reducing the gain. Under these conditions, there is a closed feedback loop; the gain is set at a point such that the picture-tube current is just sufficient to cause a little conduction in Q38.

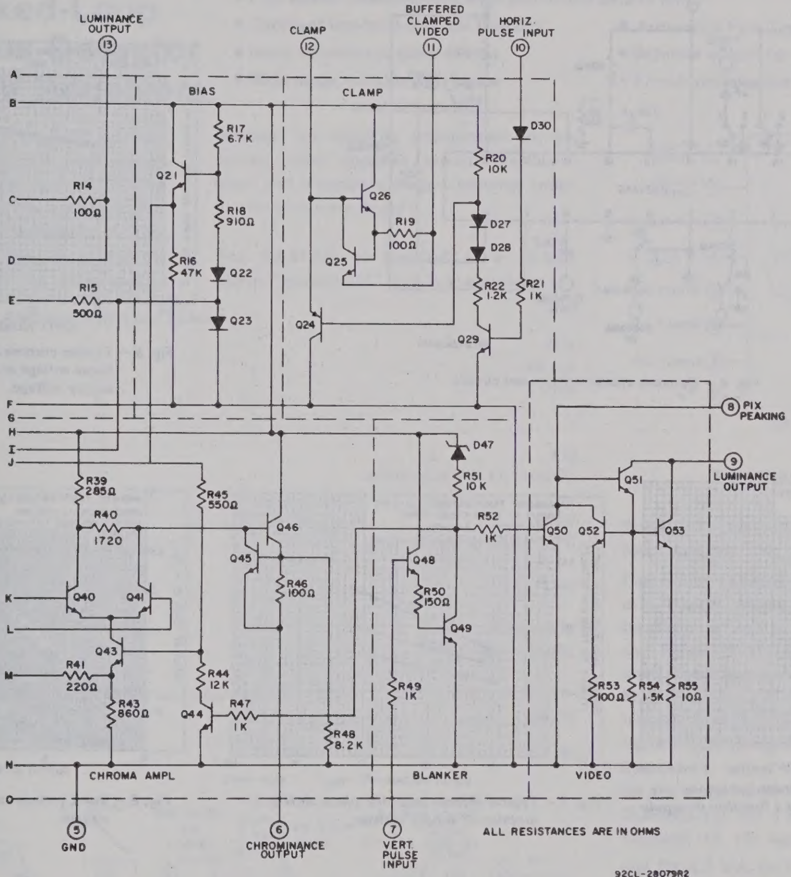


Fig. 2 – Schematic diagram

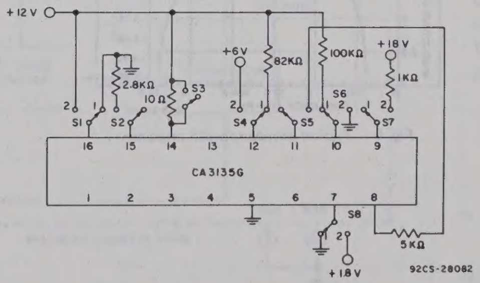


Fig. 3 – Static characteristics test circuit.

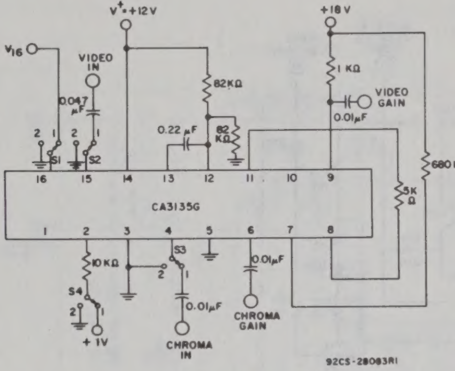


Fig. 4 – Dynamic characteristics test circuit.

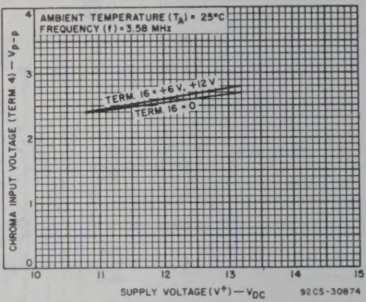


Fig. 5 – Typical chroma amplifier maximum linear voltage as a function of supply voltage.

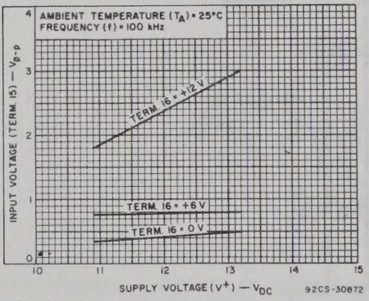


Fig. 6 – Typical maximum linear luminance voltage at terminal 15 as a function of supply voltage.

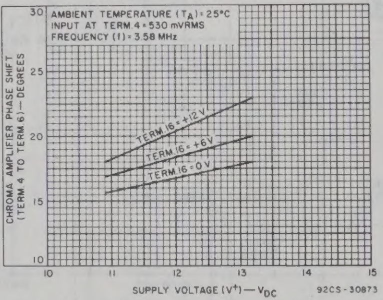


Fig. 7 – Typical chroma amplifier phase shift as a function of supply voltage.

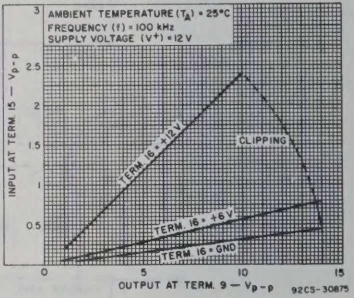


Fig. 8 – Input voltage as a function of output voltage.

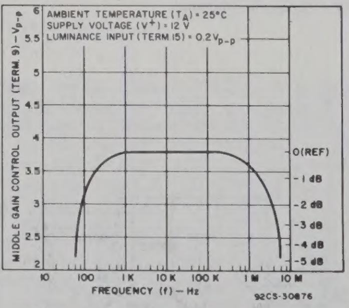


Fig. 9 – Typical gain-bandwidth response.

Preliminary Data

CA3136E

TV Video IF Phase-Locked-Loop Synchronous Detector for Color TV Receivers

Features:

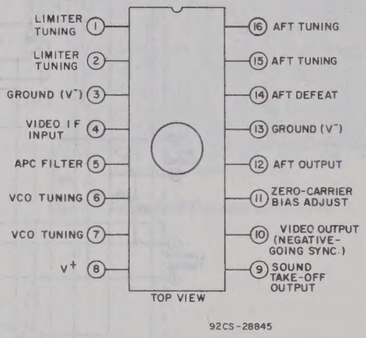
- PLL carrier oscillator with wide pull-in and hold-in range
- Excellent low-level detector linearity
- Noise inversion at video output
- Wide range, variable zero-carrier level adjustment
- Automatic Fine Tuning (AFT) Detector
- Separate output for sound take-off
- 12-volt power supnly

The RCA-CA3136E is a linear IC synchronous detector employing a phase-locked oscillator to demodulate the 45.75-MHz video if signals in color-TV receivers. The CA3136E features AFT voltage for dc control of the tuner; an adjustment for the zero-carrier dc level at the video output terminal; an amplifier arrangement for inverting noise impulses toward the black level; and a separate output terminal (non-inverting) for the sound if.

The CA3136E is supplied in a 16-lead plastic "power-stud" dual-in-line package.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Power Supply Voltage	15 V
Power Supply Current	100 mA
Input Signal Voltage -	1 Vrms
Device Dissipation:	
With no Heat Sink:	
Up to T_A = 25°C	1.4 W
Above T_A = 25°C	derate linearly at 11.1 mW/°C
With Infinite Heat Sink:	
Up to T_A = 70°C	6.5 W
Above T_A = 70°C	derate linearly at 83.3 mW/°C
Thermal Resistance:	
$R_{\theta JS}$ (Junction to Stud)	12 °C/W
Ambient Temperature Range:	
Operating	−40 to +85°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At a distance 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	265°C



TERMINAL DIAGRAM

SUGGESTED GENERAL ALIGNMENT PROCEDURE

Fig. 1 shows a block diagram of the CA3136 in a typical circuit indicating the internal functions as well as the external circuitry and signals. A 45.75-MHz, 100-mVrms (50-ohm) signal is applied to the VIDEO IF INPUT (Terminal 4). While monitoring the VIDEO OUTPUT (Terminal 10), make the following adjustments in the indicated sequence; (1) adjust the VCO TUNING coil for a dc signal (lock). (2) Adjust the LIMITER TUNING coil for a minimum dc voltage on Terminal 10. (3) Adjust the VCO TUNING coil for 5.2 Vdc on Terminal 5 (with 12 volt supply on Terminal 8). (4) Close the AFT DEFEAT switch and note the dc voltage at the AFT OUTPUT (Terminal 12). (5) Return the AFT DEFEAT switch to its open position, and adjust the AFT TUNING coil for the same dc voltage noted when the AFT DEFEAT switch was closed. (6) Remove the rf input and adjust the ZERO CARRIER BIAS potentiometer for 7 volts dc on the VIDEO OUTPUT (Terminal 10). This final adjustment completes the alignment procedure.

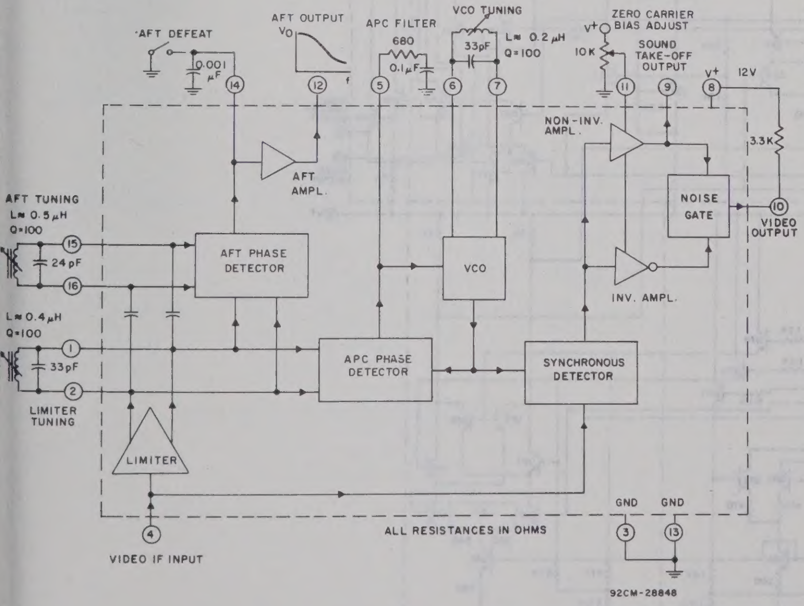


Fig. 1 – Block diagram of the CA3136 in a typical circuit application.

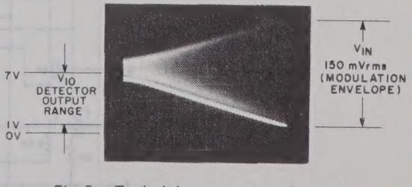


Fig. 2 – Typical detector output linearity.

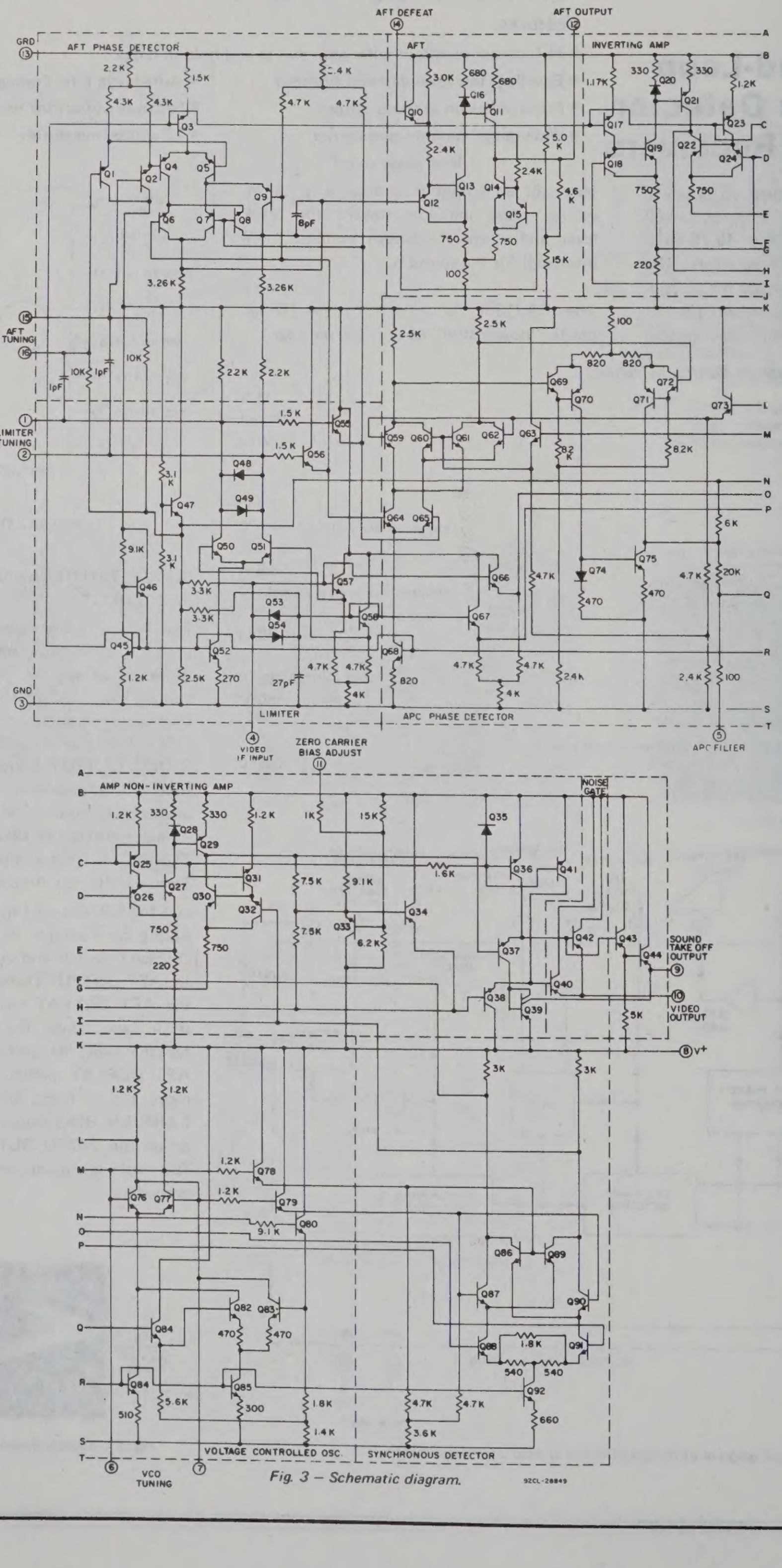


Fig. 3 – Schematic diagram.

TYPICAL ELECTRICAL CHARACTERISTICS
At V^+ = 12 VDC, f_c = 45 MHz, T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	VALUE	UNITS
Supply Current	$I_8 + I_{10}$		60	mA
Video-Output Voltage	V_{10}	Zero Carrier Bias Adjust	7	V_{DC}
Noise-Inversion Offset Voltage	V_{10}	Referenced to Zero-Carrier Level	0.3	V_{DC}
Sound IF-Take-Off Output Voltage	V_9	$V_{10} = 7\ V_{DC}$	7.7	V_{DC}
AFT Output Voltage	V_{12}	AFT Defeat Switch Closed	3	V_{DC}
Oscillator Pull-In Range			3	MHz
Oscillator Hold-In Range			6	MHz
Detector Conversion Gain			30	dB
Video Bandwidth			9	MHz
Carrier Rejection at Video Output:				
fc = 45 MHz			30	dB
2 fc = 90 MHz			40	dB
Video IF				
Parallel Input Impedance:				
Resistance at Term. 4	R_p		4	kΩ
Capacitance at Term. 4	C_p		5	pF
Sound Take-Off Output Resistance at Term. 9	R_o	1 MHz	50	Ω
Video Output Resistance at Term. 10	R_o	1 MHz	50	Ω

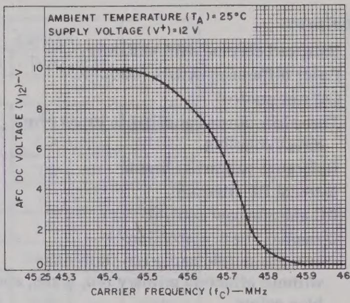


Fig. 4 – Typical AFT output of CA3136.

CA3137E

TV Chroma Demodulator

Features:

- Balanced chroma demodulators
- Color difference matrix (6500°K)
- DC tint control
- Three low-output-impedance drivers for direct coupling
- Reference subcarrier limiter
- Internal RF filtering
- DC chroma gain control
- Dynamic "flesh correction" –– corrects purple and green flesh colors without affecting primary red, green, and blue colors
- Requires few external components
- No tuning adjustments are necessary

The RCA-CA3137E is a monolithic silicon integrated circuit that performs the demodulation, dynamic "flesh correction", tint control, and chroma gain-control functions. It is designed to function compatibly with the CA3126Q Chroma Processor, and is supplied in the 16-lead dual-in-line plastic package.

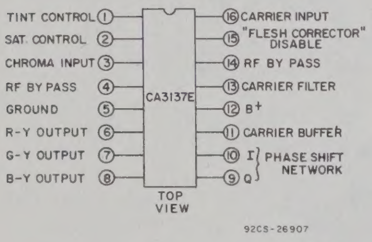


Fig.1 – CA3137E terminal assignment.

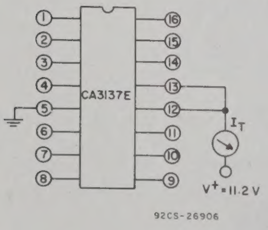


Fig.2 – DC test circuit.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

DC SUPPLY VOLTAGE (between Terms. 5 and 12)	13.2 V
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly 7.9 mW/°C
AMBIENT-TEMPERATURE RANGE:	
Operating	–40 to +85°C
Storage	–65 to +150°C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

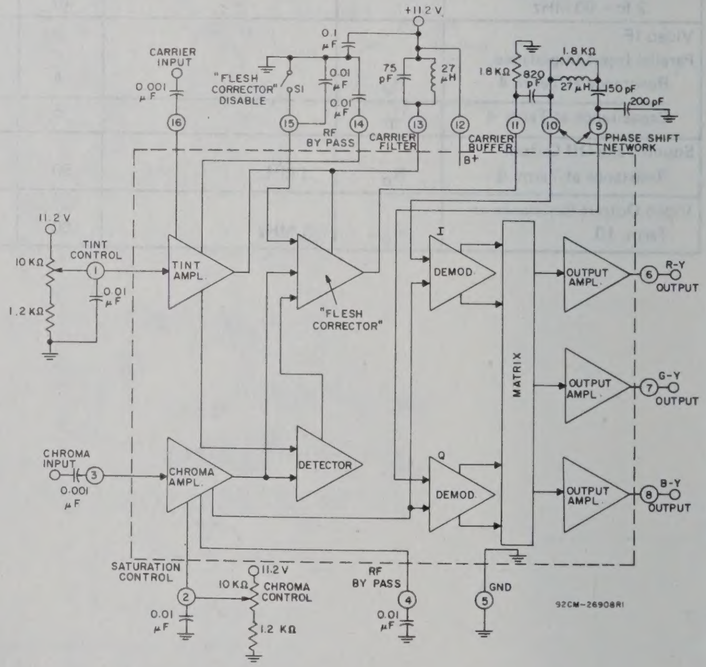


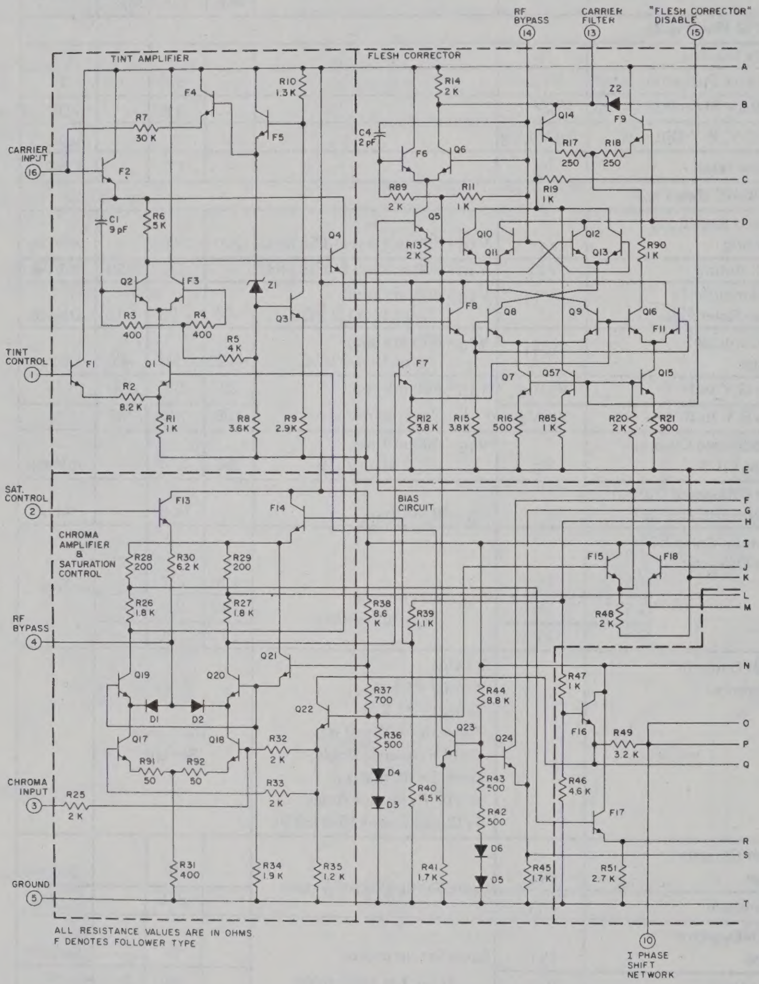
Fig.3 – Functional diagram and typical dynamic test circuit.

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $V^+ = 11.2$ V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
STATIC (See Fig.2)						
Supply Current	I_T		–	35	47	mA
Reference Subcarrier Input	V_{16}		–	6.7	–	VDC
Oscillator Reference Inputs	V_9, V_{10}		–	3.8	–	VDC
R-Y, G-Y, B-Y Outputs	V_6, V_7, V_8		–	5	–	VDC
Chroma Input	V_3		–	1.2	–	VDC
DYNAMIC (See Fig.3)						
Tint and Sensitivity Limiting	V_{11}	V_{16} = 200 mV p-p @ 3.58 MHz	200	300	–	mVp-p
Tint Limiting	V_{11}	V_{16} = 800 mV p-p @ 3.58 MHz	–	425	600	mVp-p
Tint Amplifier* Phase Reference	ϕV_{11}	V_{16} = 400 mV p-p, Term.1 = 11.2 VDC	–35	–25	–15	Degrees
Tint Control▲ Range	$\Delta\phi_{11}$	V_{16} = 800 mV p-p, Term.1 = 1.2 VDC	–130	–110	–80	Degrees
Ratio G-Y to R-Y	V_7/V_6	V_{16} = 400 mV p-p,	28	33	38	%
Ratio B-Y to R-Y	V_8/V_6	V_3 = 40 mV p-p	108	120	132	%
Demodulated Chroma Output R-Y	V_6	V_{16} = 400 mV p-p, V_3 = 40 mV p-p	350	550	–	mV p-p
Color Difference Output (Bandwidth at 3 dB)		V_3 = 40 mV p-p	–	900	–	kHz
Maximum Color Difference Outputs: R-Y	V_6	V_{16} = 400 mV p-p, V_3 = 300 mVp-p	1.5	2.2	–	V_{p-p}
G-Y	V_7		0.42	0.7	–	
B-Y	V_8		1.6	2.65	–	
"Flesh Detector" Reference:		Set-Up: Term.2 = 1.6 V Term.1 = 11.2 V Term.16 = 400 mV p-p @ 0° Reference Angle Term.3 = 40 mV p-p @ 10° Reference Angle S_1 Closed (Term.15 at GND)	Reference Set-Up			
"Flesh Detector": Phase	ϕ_{11}	Same Set-up except S_1 open	–	0	–	Degrees
Amplitude	V_{11}		–	275	–	%
"Flesh Detector": Phase	ϕ_{11}	Same Set-up except Term.3 at 190° angle	–	0	–	Degrees
Amplitude	V_{11}		–	100	–	%
Small-Signal Output Resistance (Terms.6,7,8)	r_o		–	50	–	Ω
Small-Signal Input Resistance: Term.3	r_i		–	3	–	kΩ
Terms.9&10			–	2.5	–	

* Phase angle of term. 11 referenced to term. 16 phase angle.

▲ Phase angle of term. 11 with term. 1 = 1.2 V minus phase angle of term. 11 with term. 1 = 11.2 V.



ALL RESISTANCE VALUES ARE IN OHMS
F DENOTES FOLLOWER TYPE

Fig.4 – CA3137E Schematic diagram.

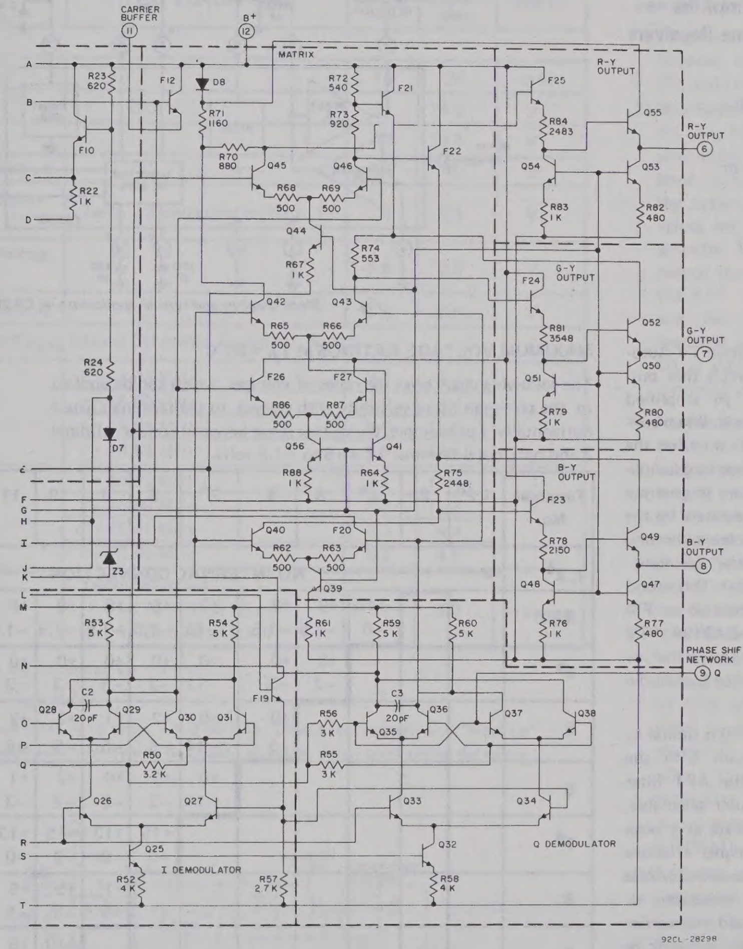


Fig.4 – CA3137E Schematic diagram.

CA3139E, CA3139Q

TV Automatic Fine Tuning Circuit

With Intercarrier Mixer/Amplifier For Color and Monochrome Receivers

Features:

- **Cascode-type high-gain amplifier (15-mV input for rated output)**
- **AFT differential peak detector**
- **Differential amplifier**
- **Bipolar outputs**
- **Five-stage intercarrier mixer/amplifier**
- **Internal voltage regulator**
- **For use in either color or monochrome receivers**

The RCA-CA3139 is a monolithic TV Automatic Fine Tuning (AFT) circuit that provides an AFT voltage and an amplified 4.5-MHz intercarrier sound signal. When connected to an output of an IF amplifier the CA3139 provides the signal processing (amplification and detection) necessary to generate the AFT correction signals required by the TV tuner. It also mixes the video and sound IF carriers and amplifies the resultant 4.5-MHz intercarrier sound signal. This sound output may then be connected to an FM detector such as the RCA-CA3134 "TV Sound IF and Audio Output Subsystem", or the RCA-CA3065 "FM Detector and Audio Driver".

The AFT portion of the CA3139 is similar to the RCA-CA3064 AFT circuit with the following exceptions: (a) the AFT filter capacitors are external and user selectable, allowing the detector to operate as a peak detector and resulting in a higher effective gain for the TV signal; (b) the detector bias resistor is external and user selectable, allowing the gain of the AFT and intercarrier signals to be adjusted; (c) the dynamic resistance of the shunt regulator has been decreased.

The CA3139 is supplied in a 14-lead dual-in-line plastic package (CA3139E) or a 14-lead plastic package with quad-formed leads (CA3139Q).

MAXIMUM RATINGS,

Absolute-Maximum Values:

DEVICE DISSIPATION:
Up to T_A = 25°C . . . . 630 mW
Above T_A = 25°C. . . . .derate linearly 6.7 mW/°C
AMBIENT TEMPERATURE:
Operating . . . . −40 to +85°C
Storage. −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32"
(1.59 mm ± 0.79 mm)
from case for 10 s max. . . . . 265°C

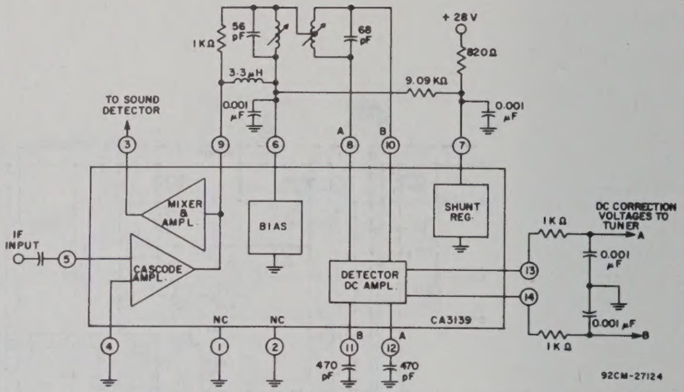


Fig. 1 – Block diagram and typical application of CA3139.

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 3 and horizontal terminal 12 is +8 to −1.5 volts.

MAXIMUM CURRENT RATINGS

Terminal No.	1, 2♠	3	4■	5	6	7▲	8	9	10	11	12	13	14	I_{IN}, I_{OUT} mA
1, 2♠	← NO INTERNAL CONNECTION →													
3			+10 −0	+9 −1.5	+8 −1.5	+0 −10	+8 −1.5	+8 −1.5	+8 −1.5	+8 −1.5	+8 −1.5	+8 −1.5	+8 −1.5	10
4■				+0 −2	+0 −3	+0 −11	+0 −3	+0 −3	+0 −3	+0 −3	+0 −3	+0 −11	+0 −11	50
5					+0 −5	+0 −14	+2 −5	+1 −5	+2 −5	+2 −5	+2 −5	+1 −8	+1 −8	1
6						+0 −14	+2 −2	+0 −2	+2 −2	+1 −3	+1 −3	+0 −10	+0 −10	2
7▲							+15 −0	+13 −0	+15 −0	+13 −0	+13 −0	+10 −0	+10 −0	50
8								+1 −5	+5 −5	+5 −5	+1 −5	+0 −14	+0 −14	2
9									+10 −2	+8 −2	+8 −2	+0 −10	+0 −10	10
10										+1 −5	+5 −5	+1 −10	+1 −10	2
11											*	*	*	2
12												*	*	2
13													+14 −14	2
14														2

▲ Terminal number 7 may be connected to any positive voltage source greater than the internal zener regulating voltage through a suitable dropping resistor – provided the dissipation rating is not exceeded.

■ This terminal should be connected to the most negative potential of the complete circuit.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

♠ It is recommended that unused terminals 1 and 2 be grounded to act as shields.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $V^+ = 28$ V (Unless Otherwise Specified)

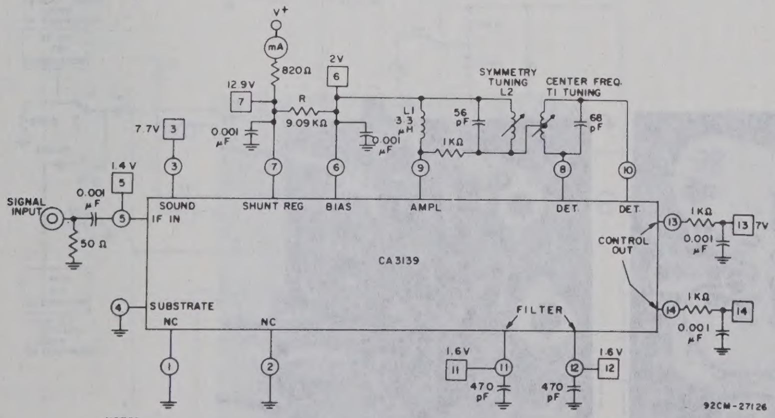
See Test Circuit, Fig. 2

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
NO SIGNAL INPUT				
Supply Current, I^+		15	20	mA
Low Voltage at Term. 7[1]	$V^+ = 20.8$ V	11	14.5	V
Shunt Reg. Voltage		12	14.5	V
Quiescent Voltage at Term. 3		4.5	10	V
Quiescent Voltage[2] at Terms. 13 and 14	Term. 13 connected to Term. 14	6	8.5	V
Quiescent Difference Voltage, Terms. 13 to 14		–0.8	+0.8	V
Quiescent Voltage at Term. 6		1.4	2.6	V
SIGNAL INPUT = 15 mV_{RMS} (Unless Otherwise Specified), Note 3				
Correction Voltage at Term. 13	f = 44.65 MHz	2.2	4.7	V
	f = 45.69 MHz	1.2	4.4	
	f = 45.81 MHz	9.6	13.8	
	f = 46.85 MHz	9.1	12.1	
Correction Voltage at Term. 14	f = 44.65 MHz	9.1	12.1	V
	f = 45.69 MHz	9.6	13.8	
	f = 45.81 MHz	1.2	4.4	
	f = 46.85 MHz	2.2	4.7	
4.5 MHz Output	Two-Tone Input f1 = 45.75 MHz at 15 mV f2 = 41.25 MHz at 5 mV	50	200	mV_{RMS}

NOTES: 1. $I_7 = 12$ mA maximum at $V_7 = 11$ V.

2. $V_{13} = 0.55\ V_Z \pm 0.7$ V

3. Resistor from term. 6 to term. 7 = 9.09 KΩ. Crossover steepens and "bow tie" width increases when resistor is decreased in value. Total peak swing decreases slightly.



NOTES:

1. Use 10 KΩ Isolation Resistor at DC Voltmeter Probe Tip When Making DC Measurements.
2. Typical No-Signal DC Potentials Are Shown.
3. Boxes Represent Test Points.

L1: RCA P.N. 122205
L2: RCA P.N. 14133
4½ Turns #22 Wire, O.D. = 0.25" (Typ.)
Q (Unloaded) = 100 (Min.)
f = 41.25 MHz
Inductance = 0.18 μh (Typ.)

T1: RCA P.N. 140507
3½ Turns (Center Tapped) #20 Wire,
O.D. = 0.36" (Typ.)
Q (Unloaded) = 140 (Min.)
f = 45.75 MHz
Inductance = 0.18 μh (Typ.)

Fig. 2 – Test circuit.

CIRCUIT DESCRIPTION

The CA3139 consists of five functional circuits as shown in the block diagram, Fig. 1 (see Fig. 5 for schematic diagram).

1) **Cascode Amplifier** – Consists of emitter-follower Q1, common-emitter amplifier Q2, and common-base amplifier Q3.

2) **Bias Circuit** – Consists of Q4 and resistors R1, R4, R5, and an external resistor (user selectable) connected to the voltage regulator, terminal 7. The nominal value of the external resistor is 9.1 kΩ. Reduced values will raise the gain of the cascode amplifier chain, and higher values will reduce the gain. If the gain is increased, the AFT "Bow Tie" width will increase and the crossover slope will increase (become steeper). The input transistor Q1 is internally biased, so AC coupling is normally used to the input terminal 5.

3) **Intercarrier Mixer/Amplifier** – The output of the cascode amplifier at terminal 9 is also internally connected to the intercarrier mixer/amplifier chain consisting of transistors Q13 through Q17 and associated components. The video IF carrier at 45.75-MHz and the FM sound IF carrier at 41.25-MHz are down-converted to a 4.5-MHz FM signal by Q14. A low-pass filter removes the carriers and upper conversion signal components. The 4.5-MHz FM signal is further amplified and filtered by Q16 and C3. The FM sound output signal is at terminal 3. The gain with respect to a 5-mV sound carrier (tested with a 15-mV video carrier) input signal at terminal 5 is 10 to 40 when the resistor is connected between terminals 6 and 7 is 9.09 kΩ.

4) **AFT Detector and DC Amplifier** – Consists of Q6 through Q12 and related components. The detector inputs at terminals 8 and 10 are connected to the external discriminator transformer and biased through the transformer at terminal-6 potential. The total current through transistors Q7 and Q8 is held constant by the current-mirror transistors Q10, Q11, and Q12. External filter capacitors connected to terminals 11 and 12 assure that peak detection is accomplished. The AFT output voltages are shown in the Electrical Characteristics chart, and a graphical representation is shown in Fig. 4.

5) **Voltage Regulator** – An active shunt regulator, consisting of D1, D2, Z1, Z2, and Q5, is included to reduce the dynamic resistance.

CA3139E, CA3139Q

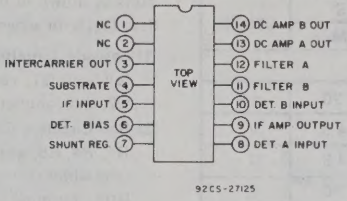


Fig. 3 – Terminal assignment.

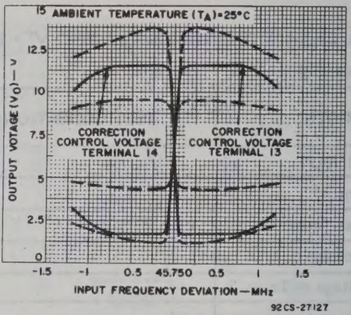


Fig. 4 – Dynamic control-voltage characteristics.

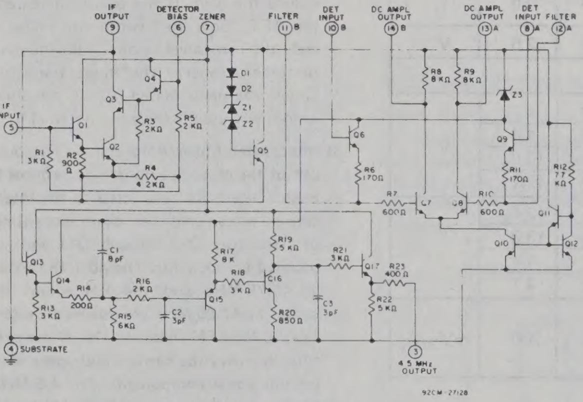


Fig. 5 – Schematic diagram of CA3139.

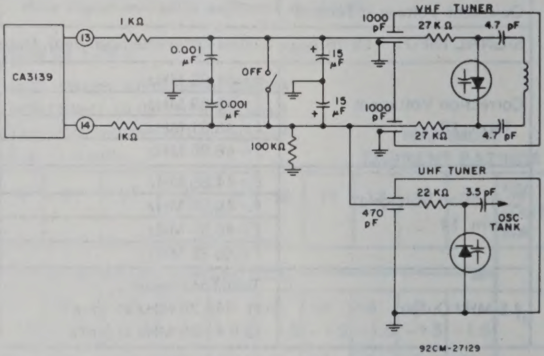


Fig. 6 – Typical tuner connection.

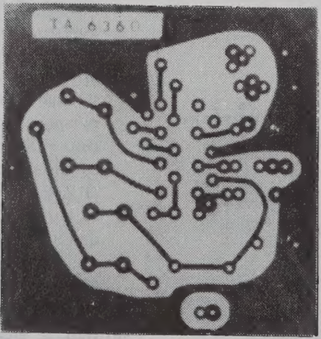


Fig. 7 – Template of CA3139Q circuit board (actual size, bottom view).

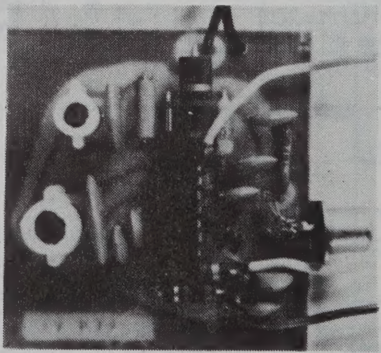


Fig. 8 – CA3139Q circuit board with components.

TV Luminance Processor

The CA3143E is a monolithic silicon integrated circuit that performs the luminance processing functions of amplification; contrast, brightness and peaking control; blanking; and black-level clamping.

This device, when used in conjunction with the CA3126Q chroma processor and the CA3137E chroma demodulator, will provide a luminance/chrominance system having excellent tracking of controls. The CA3143E is supplied in a 14-lead dual-in-line plastic package.

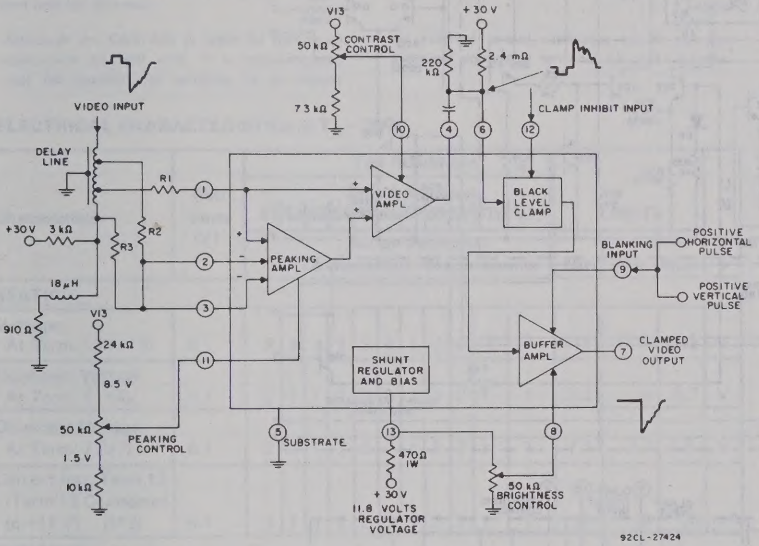
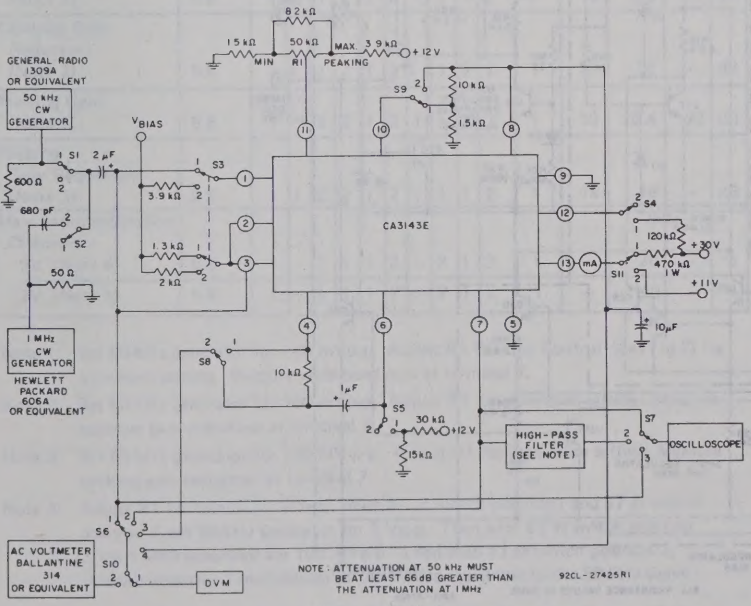


Fig.1 – Functional block diagram.



NOTE: ATTENUATION AT 50 kHz MUST BE AT LEAST 66 dB GREATER THAN THE ATTENUATION AT 1 MHz

Fig.2 – Test circuit.

Features:

- **Black-level clamping**
- **Linear dc controls for brightness, contrast, and peaking**
- **Horizontal and vertical blanking**
- **Operates with standard or tapped delay line**

CIRCUIT DESCRIPTION

Fig. 1 is a block diagram of the CA3143E indicating the internal functions as well as external circuitry and signals. The video input signal with positive-going sync is applied to the input of the tapped delay line. Signals from fixed taps of the delay line are applied to terminals 1, 2 and 3 of the CA3143E. In referring to Fig.4, the signal from the delay line tap A is applied to the video input at terminal 1. The signals from taps B and C are summed where $V_A + V_B = V_{sum}$. The signal (V_{sum}) is then applied to the parallel connection of the peaking input terminals, 2 and 3. The video input signal is applied to a non-inverting input of the peaking amplifier while the peaking input signal (V_{sum}) is applied to an inverting input of the peaking amplifier.

Low-frequency video components are unattenuated, while high-frequency components are attenuated as a function of the delay-line tap points. The peaking amplifier is a differential amplifier, so that the output is proportional to V_1 minus V_{sum}. At low frequencies, the signal at terminals 2 and 3 is unattenuated, and the peaking amplifier produces no output at these frequencies. However, at high frequencies the signal at terminals 2 and 3 is attenuated thus, the peaking amplifier output consists of high-frequency video. The peaking control setting determines the amplitude of the peaking signal which is then fed to the video amplifier, where it is added to the video input signal and amplified. The setting of the peaking control does not substantially affect the dc quiescent voltage at terminal 4.

The low-impedance video amplifier output is at terminal 4. The signal is fed through an external coupling capacitor to terminal 6, the black-level clamp input. The action of the black-level clamp is such that it clamps to the black level rather than to the sync level. Refer to the circuit diagram in Fig.3. Consider the situation where no signal is applied to terminal 12. Terminal 6 is biased through diode D2. The signal at terminal 6 will clamp its most negative excursion (sync pulse) to the anode voltage of D2. However, if a positive pulse is applied to terminal 12 during the sync interval, the anode of D2 is forced to ground due to saturation of Q17. The clamp is thus disabled, and terminal 6 will clamp to the next lower signal level, the black level.

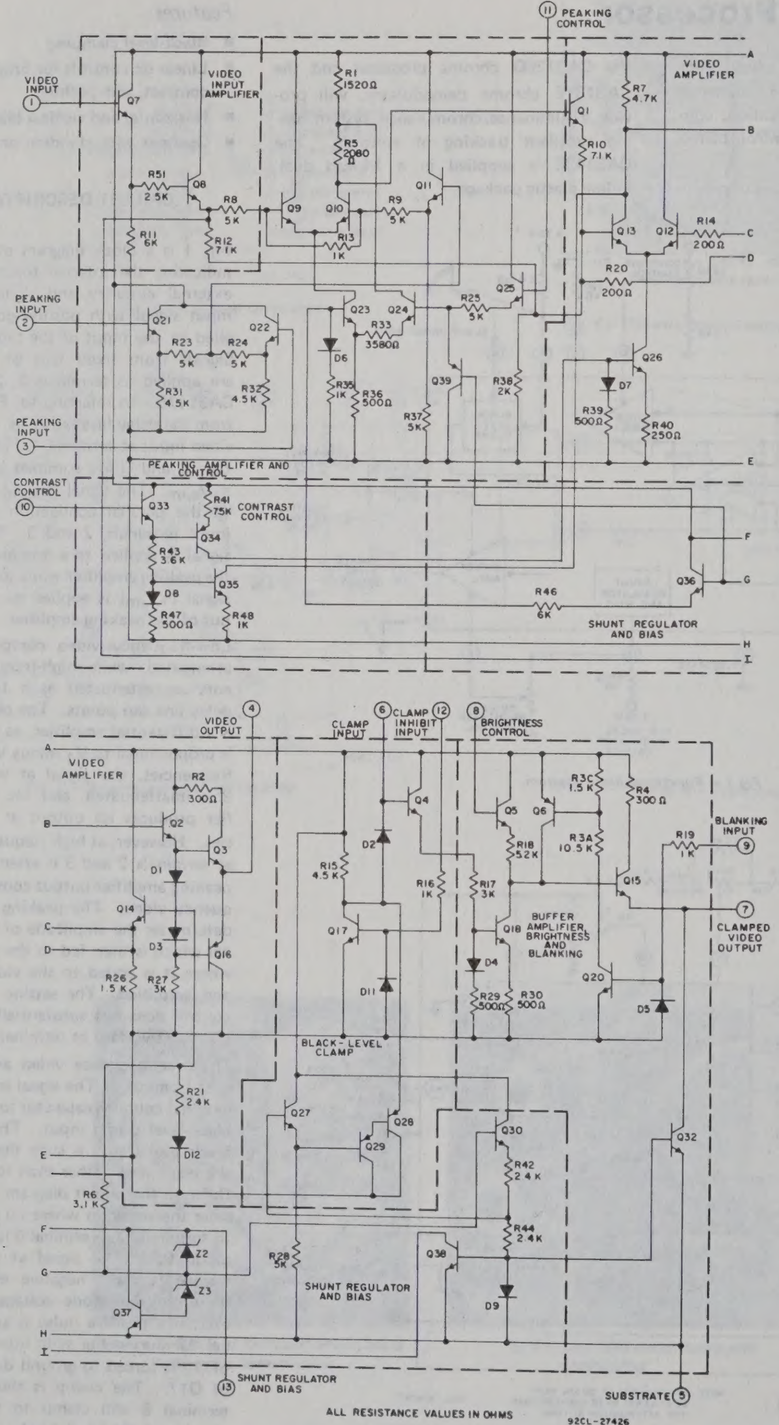


Fig. 3 – Schematic diagram of CA3143E .

MAXIMUM RATINGS, *Absolute-Maximum Values*:

DC SUPPLY CURRENT (Into Terminal 13)*	59.5 mA
DEVICE DISSIPATION:*	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly 7.9 mW/°C
AMBIENT–TEMPERATURE RANGE:	
Operating	–40 to +85°C
Storage	–65 to +150°C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

* Although the CA3143E is rated for maximum dissipation of 750 mW, it is recommended that the current into terminal 13 be limited by external circuit resistance to 39 mA for a typical voltage at terminal 13 of 11.8 volts.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Bias Volts (V)	Test Conditions Switch Numbers											LIMITS			UNITS
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11				
		Switch Positions For Characteristics Measurements											Min.	Typ.	Max.	
STATIC																
Voltage: At Term. 13 (V13)	6.1	2	1	1	2	2	4	1	2	2	1	1	11	11.8	13.2	V
Quiescent Voltage At Term. 4 (V4)	6.1	2	1	1	2	2	3	1	2	2	1	1	3.3	4	5.7	V
Quiescent Voltage At Term. 7 (V7)	6.1	2	1	1	2	2	2	1	2	2	1	1	7.1	7.7	8.3	V
Current into Term.13 (Term.13 Connected to +11 V) (I13)	6.1	2	1	1	2	2	3	1	2	2	1	2	10	19	30	mA
DYNAMIC																
Wide-Band Gain (Note 1)	5.8	1	1	1	2	1	2	1	1	1	2	1	6	8.3	11	dB
Contrast Gain Reduction (Note 2)	5.8	1	1	1	2	1	2	1	1	2	2	1	27	30	–	dB
Peaking Gain (Note 1)	5.8	1	1	2	2	1	2	1	1	1	2	1	15	18.4	22	dB
Peaking Gain Reduction (Note 3)	5.8	1	1	2	2	1	2	1	1	1	2	1	16	18	–	dB
Max. Intermodulation Distortion: 2V (Note 4)	5.8	1	–	1	1	1	2	–	2	1	2	1	–	20	–	%
3V (Note 5)	5.8	1	–	1	1	1	2	–	2	1	2	1	–	40	–	%

Note 1: Set 50-kHz generator for 100 mVp-p. Adjust R1 Peaking Control (See Fig.2) for minimum setting. Measure wide-band gain at terminal 7.

Note 2: Set 50-kHz generator for 100 mVp-p. Adjust R1 for minimum setting. Measure contrast gain reduction at terminal 7.

Note 3: Set 50-kHz generator for 100 mV-p-p. Adjust R1 for maximum setting. Measure peaking gain reduction at terminal 7.

Note 4: Adjust R1 for minimum setting. With S2 at switch position1 and S7 at switch position 3, set 50-kHz generator for 2 Vp-p. Then with S2 at switch position 2, set 1 MHz generator for 100 mVp-p. Then with S7 at switch position 2, measure downward modulation of the 1-MHz signal due to the 50-kHz signal.

Note 5: Repeat step 4 except that the 50-kHz generator must be set at 3 Vp-p.

The clamped video signal at terminal 6 is amplified and inverted at terminal 7. Blanking is accomplished by applying horizontal and vertical sync pulses to terminal 9. The pulses turn ON p-n-p transistor Q6 which shorts the base of transistor Q15 to the terminal 13 supply voltage. The brightness control function is accomplished by varying the voltage on terminal 8. The gain of the inverter stage remains constant, but the dc reference voltage follows the terminal 8 voltage. The contrast control function is accomplished by varying the voltage of terminal 10. Increasing the voltage on terminal 10 lowers the gain of the video amplifier. This reduction in gain does not substantially affect the dc quiescent voltage at terminal 4.

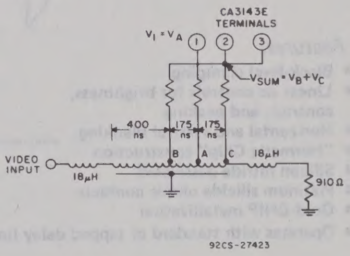
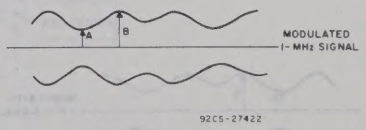


Fig.4 – Tapped delay line.



A = Amplitude of 50 kHz signal at deepest trough

B = Peak amplitude of 50 kHz signal

$$\text{Downward Modulation} = \frac{B-A}{B}$$

CA3144G

TV Luminance Processor

The CA3144G is a monolithic silicon integrated circuit that performs the luminance processing functions of amplification; contrast, brightness and peaking control; blanking; and black-level clamping.

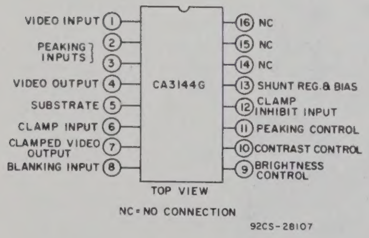
This device, when used in conjunction with the CA3126Q chroma processor and the CA3137E chroma demodulator, will provide a luminance/chrominance system having excellent tracking of controls. The CA3144G is supplied in a 16-lead hermetic Gold-CHIP dual-in-line plastic package ("G" suffix).

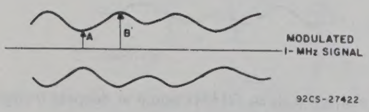
The semiconductor junctions in this device are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

Features:

- **Black-level clamping**
- **Linear dc controls for brightness, contrast, and peaking**
- **Horizontal and vertical blanking**
- **"Hermetic Chip" construction**
- **Silicon nitride passivated**
- **Platinum silicide ohmic contacts**
- **Gold-CHIP metallization**
- **Operates with standard or tapped delay line**

TERMINAL ASSIGNMENT





A = Amplitude of 50-kHz signal at deepest trough
B = Peak amplitude of 50-kHz signal

$$\text{Downward Modulation} = \frac{B-A}{B}$$

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY CURRENT (Into Terminal 13)*	57 mA
DEVICE DISSIPATION: *	
Up to $T_A = 55°C$	750 mW
Above $T_A = 55°C$	derate linearly 7.9 mW/°C
AMBIENT-TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

* Although the CA3144G is rated for maximum dissipation of 750 mW, it is recommended that the current into terminal 13 be limited by external circuit resistance to 39 mA for a typical voltage at terminal 13 of 12.3 volts.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Characteristic	Bias Volts (V)	Test Conditions											LIMITS			UNITS
		Switch Numbers														
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11				
		Switch Positions For Characteristics Measurements											Min.	Typ.	Max.	
STATIC																
Voltage: At Term. 13 (V13)	6.5	2	1	1	2	2	4	1	2	2	1	1	11	12.3	13.2	V
Quiescent Voltage At Term. 4 (V4)	6.5	2	1	1	2	2	3	1	2	2	1	1	3.3	4	5.7	V
Quiescent Voltage At Term. 7 (V7)	6.5	2	1	1	2	2	2	1	2	2	1	1	7.1	7.7	8.3	V
Current into Term.13 (Term.13 Connected to +11 V) (I13)	6.5	2	1	1	2	2	3	1	2	2	1	2	10	18	30	mA
DYNAMIC																
Wide-Band Gain (Note 1)	7.3	1	1	1	2	1	2	1	1	1	2	1	1	3	5	dB
Contrast Gain Reduction (Note 2)	7.3	1	1	1	2	1	2	1	1	2	2	1	27	30	–	dB
Peaking Gain (Note 1)	7.3	1	1	2	2	1	2	1	1	1	2	1	9	13	17	dB
Peaking Gain Reduction (Note 3)	7.3	1	1	2	2	1	2	1	1	1	2	1	16	18	–	dB
Max. Intermodulation Distortion:																
3.8 V (Note 4)	7.3	1	–	1	1	1	2	–	2	1	2	1	–	20	–	%
5 V (Note 5)	7.3	1	–	1	1	1	2	–	2	1	2	1	–	40	–	%

Note 1:
Set 50-kHz generator for 200 mV_{rms}. Adjust R1 peaking control for minimum setting (see Fig. 2). Measure wide-band gain at terminal 7.

Note 2:
Set 50-kHz generator for 200 mV_{rms}. Adjust R1 for minimum setting. Measure contrast gain reduction at terminal 7.

Note 3:
Set 50-kHz generator for 200 mV_{rms}. Adjust R1 for maximum setting. Measure peaking gain reduction at terminal 7.

Note 4:
Adjust R1 for minimum setting. With S2 at switch position 1 and S7 at switch position 3, set 50-kHz generator for 3.8 V_{p-p}. Then with S2 at switch position 2, set 1-MHz generator for 200 mV_{rms}. Then with S7 at switch position 2, measure downward modulation of the 1-MHz signal due to the 50-kHz signal.

Note 5:
Repeat step 4 except that the 50-kHz generator must be set at 5 V_{p-p}.

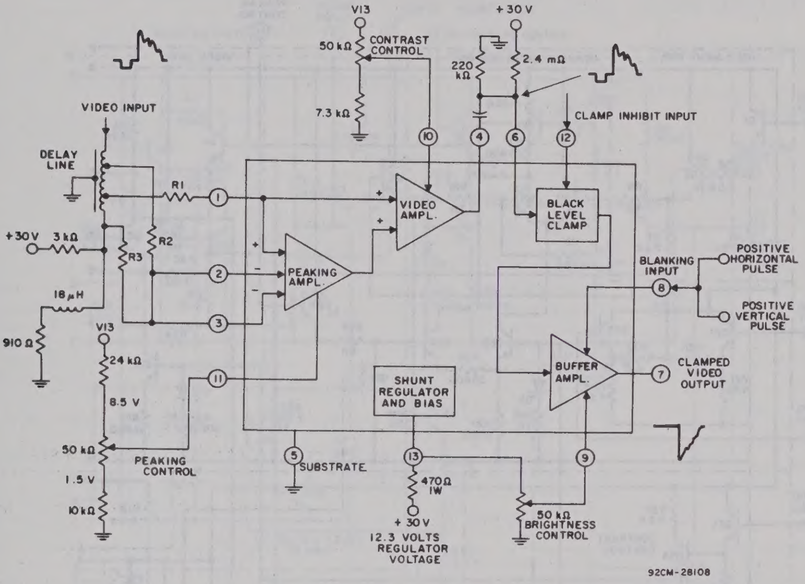
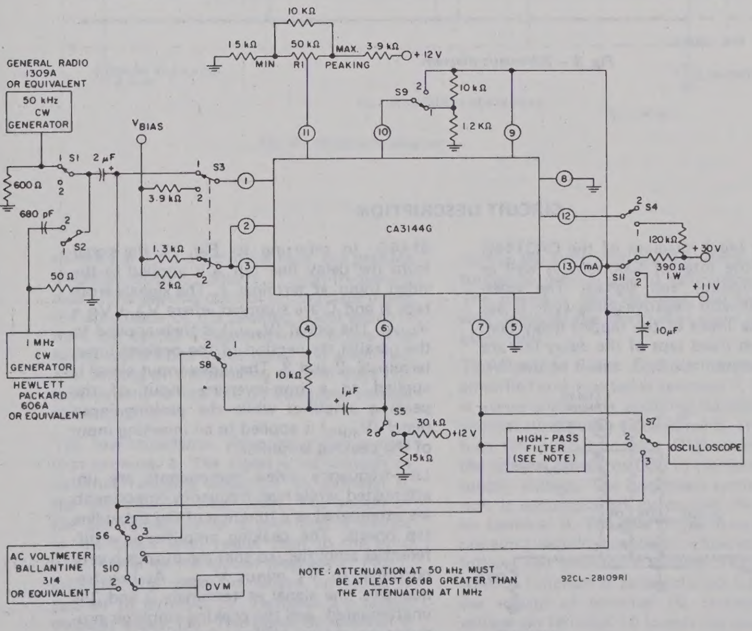


Fig. 1 — Functional block diagram.



NOTE: ATTENUATION AT 50 kHz MUST BE AT LEAST 66 dB GREATER THAN THE ATTENUATION AT 1 MHz

Fig. 2— Test circuit.

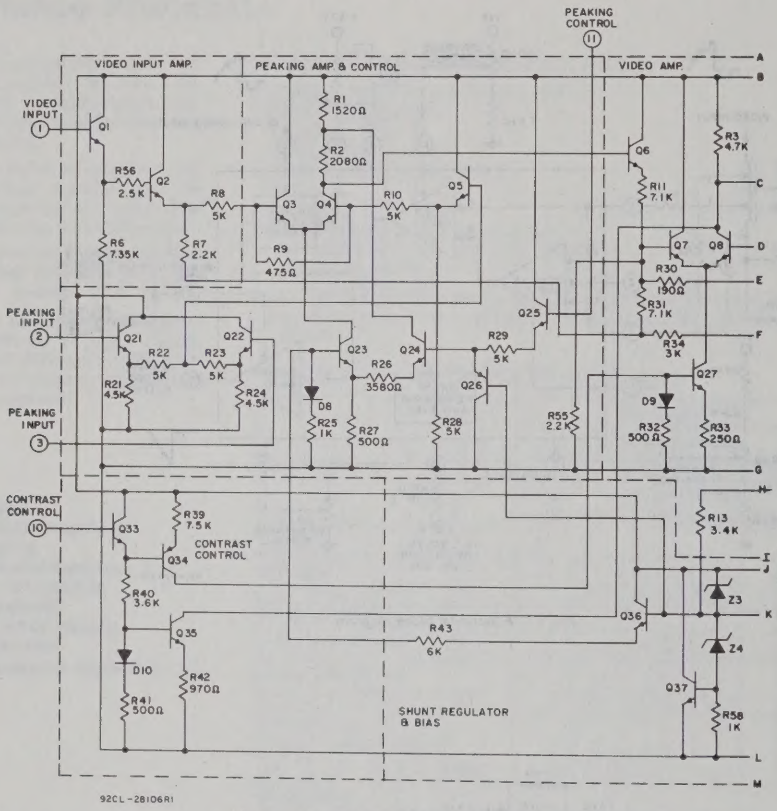


Fig. 3 – Schematic diagram

CIRCUIT DESCRIPTION

Fig. 1 is a block diagram of the CA3144G indicating the internal functions as well as external circuitry and signals. The video input signal with negative-going sync is applied to the input of the tapped delay line. Signals from fixed taps of the delay line are applied to terminals 1, 2, and 3 of the CA3144G. In referring to Fig. 4, the signal from the delay line tap A is applied to the video input at terminal 1. The signals from taps B and C are summed where $V_A + V_B = V_{sum}$. The signal (V_{sum}) is then applied to the parallel connection of the peaking input terminals, 2 and 3. The video input signal is applied to a non-inverting input of the peaking amplifier while the peaking input signal (V_{sum}) is applied to an inverting input of the peaking amplifier.

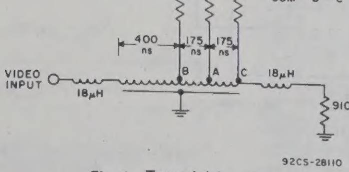


Fig. 4– Tapped delay line.

Low-frequency video components are unattenuated, while high-frequency components are attenuated as a function of the delay-line tap points. The peaking amplifier is a differential amplifier, so that the output is proportional to V_1 minus V_{sum}. At low frequencies, the signal at terminals 2 and 3 is unattenuated, and the peaking amplifier produces no output at these frequencies. However, at high frequencies the signal at ter-

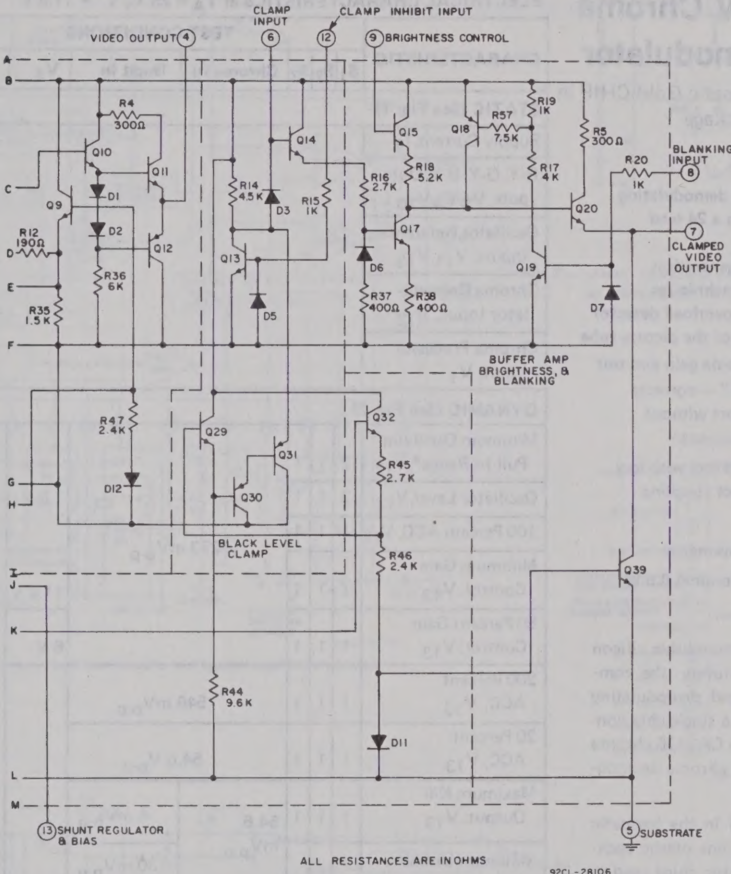


Fig. 3— Schematic diagram

minals 2 and 3 is attenuated thus, the peaking amplifier output consists of high-frequency video. The peaking control setting determines the amplitude of the peaking signal which is then fed to the video amplifier, where it is added to the video input signal and amplified. The setting of the peaking control does not substantially affect the dc quiescent voltage at terminal 4.

The low-impedance video amplifier output is at terminal 4. The signal is fed through an external coupling capacitor to terminal 6, the black-level clamp input. The action of the black-level clamp is such that it clamps to the black level rather than to the sync level. Refer to the circuit diagram in Fig. 1. Consider the situation where no signal is applied to terminal 12. Terminal 6 is biased through diode D3. The signal at terminal 6 will clamp its most negative excursion (sync pulse) to the anode voltage of D3. However, if a positive pulse is applied to terminal 12 during the sync interval, the anode of D3 is forced to ground due to saturation of Q13. The clamp is thus disabled, and terminal 6 will clamp to the next lower signal level, the black level.

The clamped video signal at terminal 6 is amplified and inverted at terminal 7. Blanking is accomplished by applying horizontal and vertical sync pulses to terminal 8. The pulses turn ON p-n-p transistor Q18 which shorts the base of transistor Q20 to the terminal 13 supply voltage. The brightness control function is accomplished by varying the voltage on terminal 9. The gain of the inverter stage remains constant, but the dc reference voltage follows the terminal 8 voltage. The contrast control function is accomplished by varying the voltage of terminal 10. Increasing the voltage on terminal 10 lowers the gain of the video amplifier. This reduction in gain does not substantially affect the dc quiescent voltage at terminal 4.

CA3151G

Single Chip TV Chroma Processor/Demodulator

"G" Suffix Type – Hermetic Gold-CHIP in Dual-In-Line Plastic Package

System Features:

- **All chroma processing and demodulating circuitry on a single chip in a 24-lead plastic package**
- **Phase-locked subcarrier regeneration utilizing sample-and-hold techniques**
- **Supplementary ACC with overload detector to prevent over saturation of the picture tube**
- **Linear dc controls for chroma gain and tint**
- **Dynamic "flesh correction" – corrects purple and green flesh colors without affecting primary colors**
- **Balanced chroma demodulators with low output impedance for direct coupling**
- **Internal rf filtering**
- **Requires few external components**
- **Low system dissipation—nominal 0.5 W**

The RCA-CA3151G is a monolithic silicon integrated circuit that performs the complete chroma processor and demodulating functions for color TV. The single chip contains all the features of the CA3126 chroma processor and the CA3137 chroma demodulator.

The CA3151G is supplied in the hermetic Gold-CHIP 24-lead dual-in-line plastic package (G suffix). The transistor chips used in the hermetic Gold-CHIP plastic packages are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
Between Terms. 18 and 7 . . . . . 13.2 V
DEVICE DISSIPATION:
Up to T_A = 55°C . . . . 825 mW
Above T_A = 55°C . . . Derate linearly at 8.7 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating . . . . −40 to +85°C
Storage . . . . −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

Preliminary Data

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 11.6 V

CHARACTERISTIC	TEST CONDITIONS							TYPICAL VALUE	UNITS
	S_1	S_2	S_3	Chroma In	Burst In	V_4	V_{17}		
STATIC (See Fig. 1)									
Supply Current, I_T								42	mA
R-Y, G-Y, B-Y, Outputs, V_8, V_9, V_{10}								5.3	Vdc
Oscillator Reference Inputs, V_{11}, V_{12}								3.7	
Chroma Demodulator Input, V_{13}								2.9	
Chroma Processor Input, V_1								2.2	
DYNAMIC (See Fig. 2)									
Minimum Oscillator Pull-In Range*, V_{12}	2	1	1	273 mV_{p-p}		1.5 V	7 V	±300	Hz
Oscillator Level, V_{12}	2	1	1					0.6	V_{p-p}
100 Percent ACC, V_{13}	1	1	1					1	
Minimum Gain Control, V_{13}	1	1	1			11.6 V		20	mV_{p-p}
50 Percent Gain Control, V_{13}	1	1	1			6 V		50	% of 100% ACC Value
200 Percent ACC, V_{13}	1	1	1	546 mV_{p-p}		1.5 V		100	
20 Percent ACC, V_{13}	1	1	1	54.6 V_{p-p}				100	
Maximum Kill Output, V_{13}	1	1	1	54.6 mV_{p-p}	4 mV_{p-p}			20	mV_{p-p}
Minimum Unkill Output, V_{13}	1	1	1		30 mV_{p-p}			400	
Overload Detector (OLD), V_{13}	1	1	2	546 mV_{p-p}	273 mV_{p-p}			1	V_{p-p}
R-Y Sensitivity, V_{10} E_g = 282 mV_{p-p}, 3.53 MHz	1	2	1	0				0.8	
R-Y Ratio B-Y/R-Y, V_8**	1	2	1					120	%
G-Y Ratio G-Y/R-Y, V_9**	1	2	1					33	
Max. R-Y Output, V_{10} E_g = 2 V_{p-p}, 3.53 MHz	1	2	1					3	V_{p-p}
Minimum Tint Control Range, $\phi 13$	1	1	1	273 mV_{p-p}			0 V to 11.6 V	80	Degrees

* Tune C_2 to 3,579,845 Hz with S_1 in position 2. Put S_1 in position 1, and check for pull in. Repeat for frequency tuned to 3,579,245 Hz. For other tests, frequency tuned to 3,579,545 ± 10 Hz.

** All input levels up to 2 V_{p-p}.

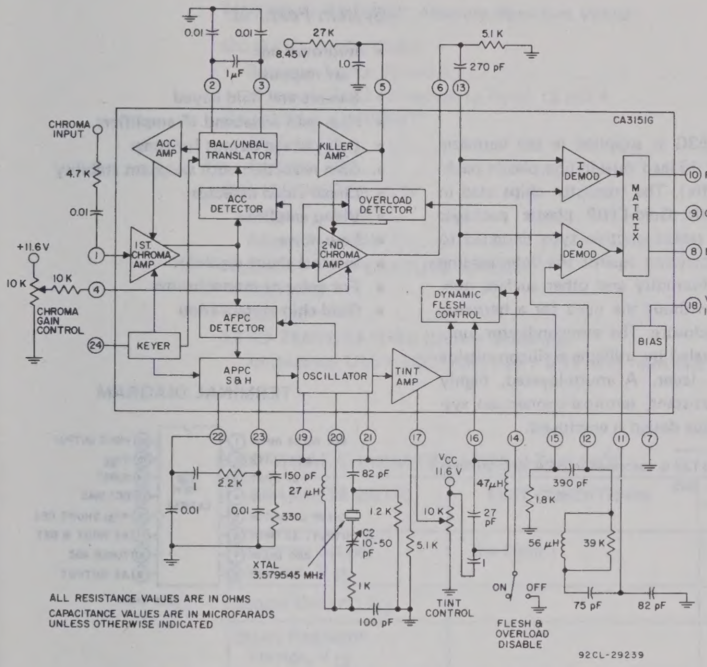


Fig. 1 – Functional diagram, static test circuit, and typical application circuit.

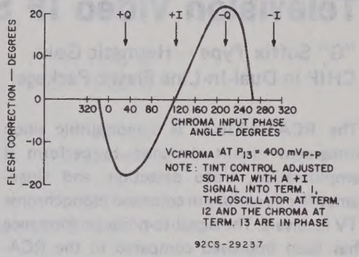
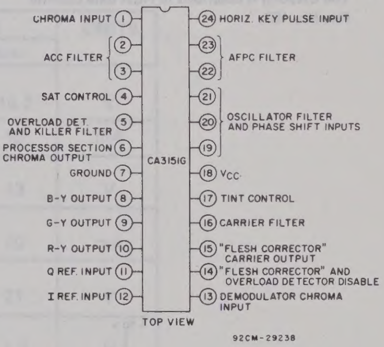


Fig. 2 – "Flesh" correction of oscillator phase angle as a function of chroma input phase angle.

TERMINAL DIAGRAM


CHROMA INPUT 1
ACC FILTER 2 3
SAT CONTROL 4
OVERLOAD DET. AND KILLER FILTER 5
PROCESSOR SECTION CHROMA OUTPUT 6
GROUND 7
B-Y OUTPUT 8
G-Y OUTPUT 9
R-Y OUTPUT 10
Q REF. INPUT 11
I REF. INPUT 12
24 HORIZ. KEY PULSE INPUT
23 22 AFPC FILTER
21 20 19 OSCILLATOR FILTER AND PHASE SHIFT INPUTS
18 VCC
17 TINT CONTROL
16 CARRIER FILTER
15 "FLESH CORRECTOR" CARRIER OUTPUT
14 "FLESH CORRECTOR" AND OVERLOAD DETECTOR DISABLE
13 DEMODULATOR CHROMA INPUT
CA3151G
TOP VIEW
92CM-29238

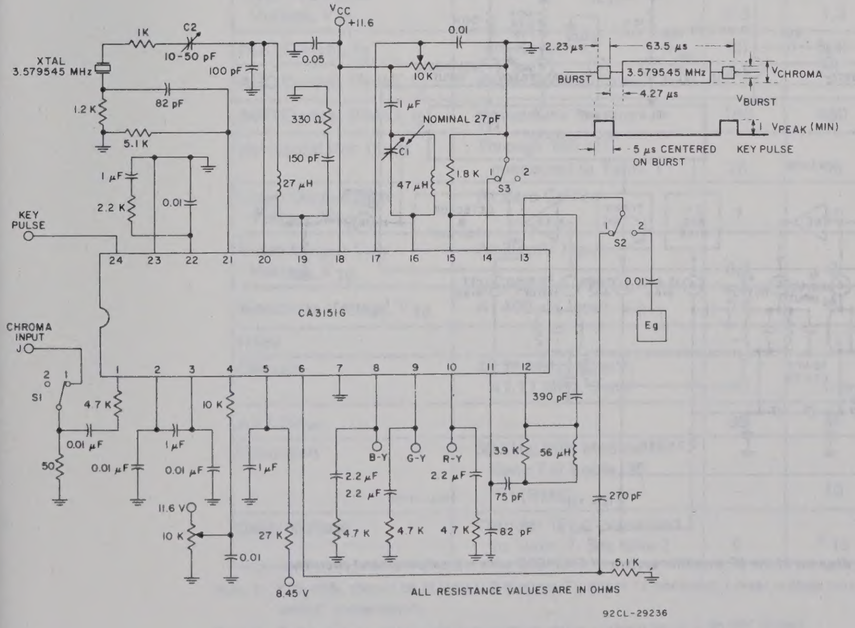


Fig. 3 – Dynamic test circuit.

CA3153G

Television Video IF System

"G" Suffix Type -- Hermetic Gold-CHIP in Dual-In-Line Plastic Package

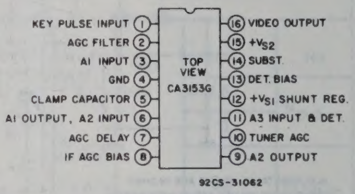
The RCA-CA3153G is a monolithic silion integrated circuit designed to perform if amplification, video detection, and video-amplifier functions in color and monochrome TV receivers. The signal-to-noise performance has been improved compared to the RCA-CA3068*. The AGC performance has also been improved through the use of a sample and hold keyed system. The RCA-CA3153G is designed to interface with the RCA-CA3139# Automatic Fine Tuning (aft) circuit, and intercarrier amplifier.

The CA3153G is supplied in the hermetic Gold-CHIP 16-lead dual-in-line plastic package (G suffix). The transistor chips used in the hermetic Gold-CHIP plastic packages are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

System Features:

- **Improved agc**
  Fast response
  Sample and hold keyed
- **High gain wideband IF amplifiers**
- **Delayed agc output for tuner**
- **Gain reduction with excellent stability**
- **Linear video detector**
- **Video amplifier**
- **Low noise**
- **Internal shunt regulator**
- **For color or monochrome**
- **Gold-chip metalization**

TERMINAL DIAGRAM



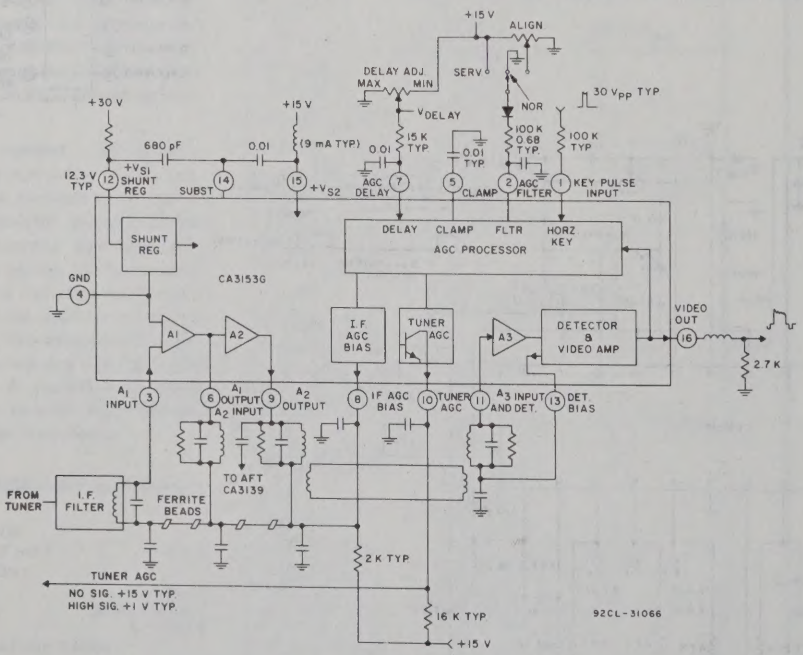


Fig. 1 – Functional block diagram of the IF amplifier-system of CA3153G with typical peripheral circuitry.

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* The CA3068 is described in RCA data bulletin File No. 467.

# The CA3139 is described in RCA data bulletin File No. 905.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
Between Terms. 15 and 4	16 V
Between 470 Ω connected to Term. 12 and 4	35 V
DC SUPPLY CURRENT:	
At Term. 15	20 mA
At Term. 12	30 mA
DEVICE DISSIPATION:	
Up to $T_A = +55^\circ C$	750 mW
Above $T_A = +55^\circ C$	Derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	–40 to +85°C
Storage	–65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Operating Supply Voltage, V_{15}	See Note 1	12	14.2	V
Supply Current, I_{15}		3	15	mA
Shunt Regulator Voltage, V_{12}		10.9	13	V
Shunt Regulator Current, I_{12}	$V_{12} = 10.5$ V	6	20	mA
Tuner AGC High Voltage, V_{10}		18.5	21	V
Tuner AGC Low Voltage, V_{10}		0.3	1.3	V
AGC Current, I_2	Non-Keyed	80	500	μA
AGC Current (Peak), I_2	Keyed Source Current	0.7	3	mA
AGC Current (Peak), I_2	Keyed Sink Current	150	680	μA
Horizontal Key Input	Through 100 kΩ connected to Term. 1	25	35	V
Video Output High Voltage, V_{16}	At Zero Carrier	7	10	V
Video Output Low Voltage, V_{16}	At 30 mV Input	0.9	2	V
Sensitivity Voltage, V_{16}	At 400 μV Input	0.9	5	V
Noise		–	12	$mV_{(RMS)}$
Chroma	45.75 MHz, 10 mV; 42.17 MHz, 3 mV	0.7	1.6	V (RMS)
AFT Drive		35	85	$mV_{(RMS)}$
Distortion	50 kHz, 80% Modulated, Sync TIP Equiv. 30 $mV_{(RMS)}$	–	10	%
Delay Voltage	Through 15kΩ connected to Term. 7. See note 2	0	V_{15}	V

Note 1: V_{15} MIN. should be at least 0.6 V above Terminal 12 potential. Lower voltage may cause some "white" compression.

Note 2: Zero voltage corresponds to maximum delay at signal input = 30 mV (RMS).

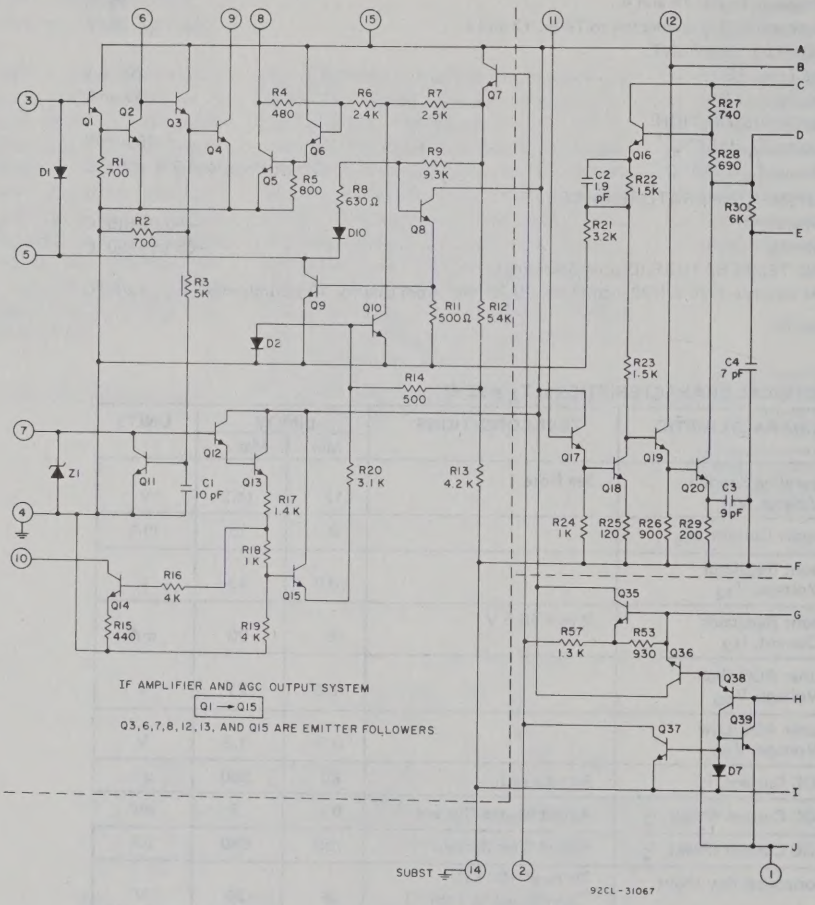


Fig. 2 – Schematic diagram for the CA31536.

AGC System (See Fig. 3)

The AGC system employs a sample-and-hold system to allow a fast-acting agc and reduce the effect of the vertical synchronizing signal on the video output stage. An override path is provided to allow a lower-gain agc system when the key pulse is not locked to the sync signal (for example, during channel selection).

The negative-going sync signal at the video output, Terminal 16, is applied to transistor Q41 through resistors R51 and R52 which act as current-limiting and filtering components. The sync signal is inverted and amplified by transistor Q41. The video portion of the signal is cutoff by the saturation voltage of Q41. When the TV system is in synchronization, the positive sync pulse at the collector of Q41 is coincident with the key input at Terminal 1, Transistor Q42 is turned off by the key pulse. Capacitor C13 is charged by the positive sync pulse through diode D9. The amplitude of the potential at C13 is proportional to the video-signal amplitude. The voltage is transfered through transistors Q40,

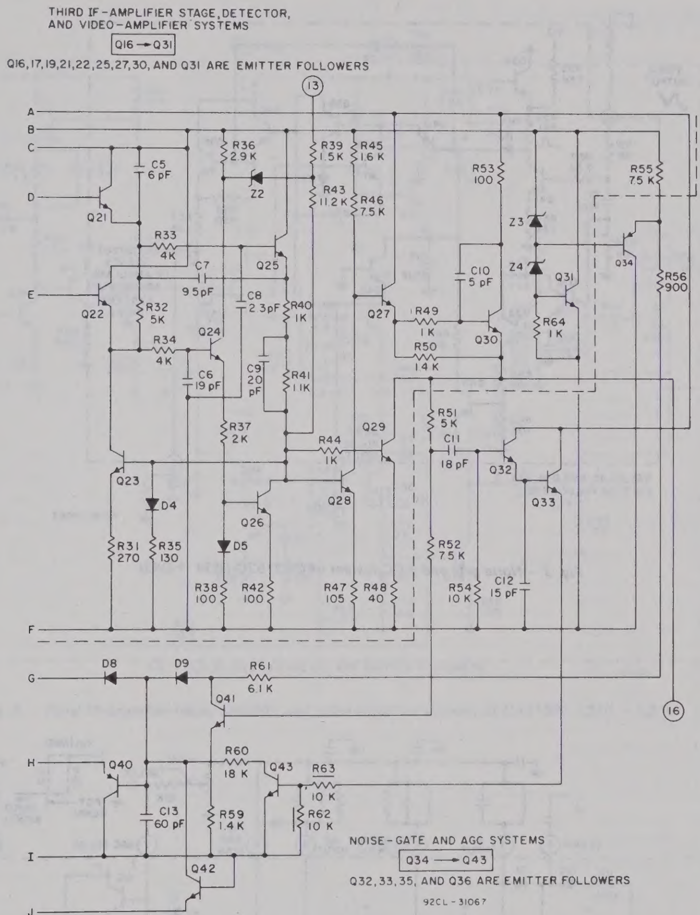


Fig. 2 – Schematic diagram for the CA3153G.

Q38, Q36, and Q35 to resistor R57 to form the charge current for the external agc filter capacitor at Terminal 2.

A constant-current discharge path for the capacitor at Terminal 2 is provided by current mirror components D7 and Q37 during the key-pulse duration. Thus the external agc filter capacitor is charged or discharged during the key-pulse interval only by the difference in current between the charge- and discharge currents. At the end of the key-pulse duration, C13 is discharged, and the charge and discharge current paths at Terminal 2 are turned off. Diode D8 provides a lower-gain agc path for turn-on during channel acquisition.

Noise-Gate System (See Fig. 3)

The circuit components, C11, R54, Q32, Q33, and Q43 perform the function of a statistical system to reduce agc gain during "spike" noise. The noise gate turns on for large amplitude fast signals and reduces the agc loop gain.

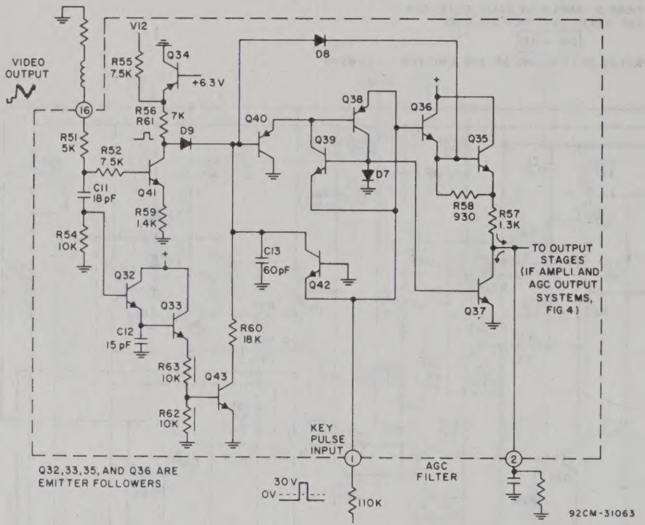


Fig. 3 – Noise-gate and AGC system of CA3153G (Q34 → Q43).

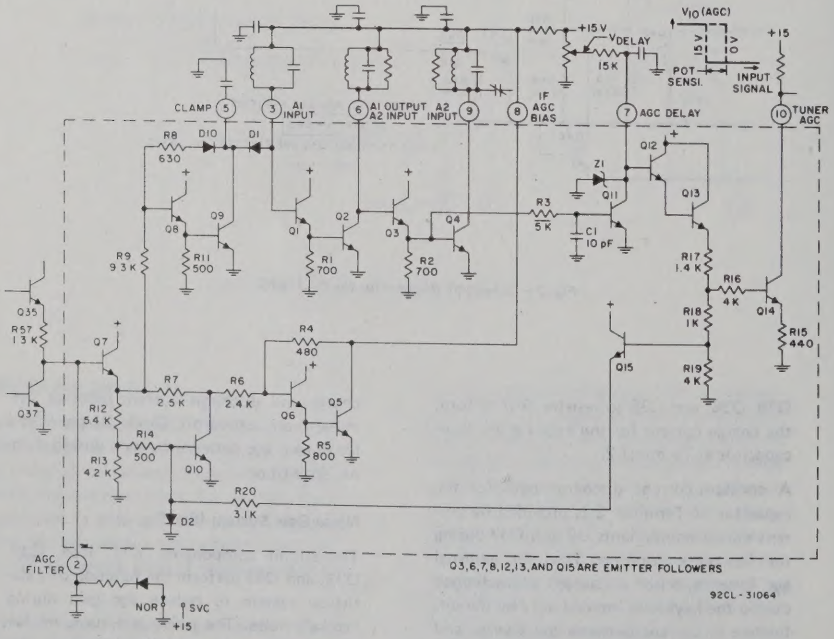


Fig. 4 – IF amplifier and AGC output system of CA3153G (Q1 → Q15).

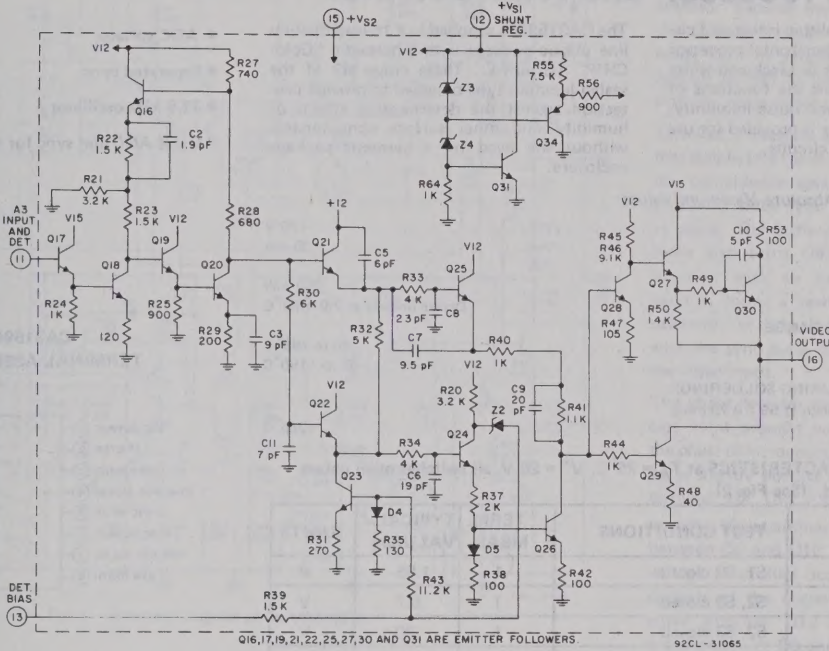


Fig. 5 – Third IF-amplifier stage, detector, and video-amplifier systems of CA3153G (Q16 → Q31).

CA3159G

Preliminary Data

Horizontal Processor and AGC Detector

The CA3159G is a monolithic integrated circuit designed for use as a horizontal processor and AGC detector in color or black-and-white TV receivers. It performs the functions of AGC, sync separation, and noise immunity, and a 31.5 kHz oscillator is provided for use with vertical-countdown circuits.

The CA3159G is supplied in a 16-lead dual-in-line plastic package with a hermetic "Gold-CHIP" (G suffix). These chips are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure.

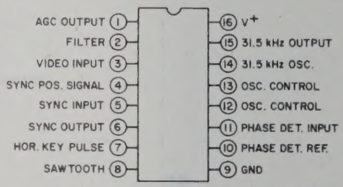
Features:

- **AGC voltage**
- **Separated sync**
- **31.5 kHz oscillator**
- **Gates AGC and sync for noise immunity**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	+30 V
DC SUPPLY CURRENT	30 mA
DEVICE DISSIPATION:	
Up to $T_A = 55^\circ C$	750 mW
Above $T_A = 55^\circ C$	Derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max.	+265°C

CA3159G TERMINAL ASSIGNMENT



92CS-31036

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, $V^+ = 28$ V, all switches open unless otherwise specified. (See Fig. 2)

CHARACTERISTIC	TEST CONDITIONS	TERM. MEAS.	TYPICAL VALUES	UNITS
AGC Voltage	S1, S9 closed	1	1.85	V
Noise Inverter[1]	S2, S9 closed	1	0.7	V
Shift Threshold[1]	S2, S3 closed	1	20	V
Sync Level	S1, S9 closed	4	18	V
Positive Pulse[2]	S5 closed	7	25	V
Positive Sawtooth[3]	S5, S6 closed	8	3	V
Sync Low	S3, S4 closed	6	1.5	V
Supply Current		16	20	mA
Free-Running Freq.[4]	S7,S8,S9 closed	15	31.5	kHz
Duty Cycle	S7,S8,S9 closed	15	48	%

1. A = 3 V, B = 1.2 V, − 1 mA to term. I
2. C = 0.2 mA
3. C = 0.2 mA, D = 5 mA
4. Adjust LI, $V^+ = 20$ V

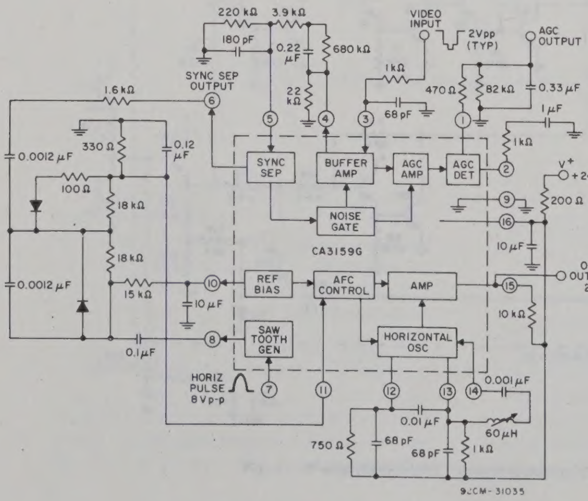


Fig. 1 – Functional block diagram of CA3159G.

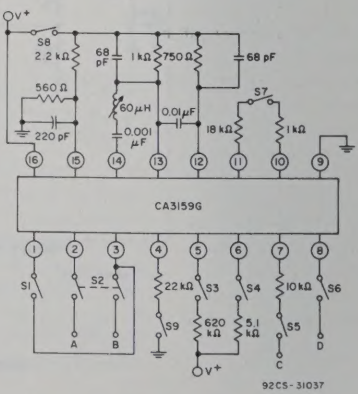


Fig. 2 – DC test circuit.

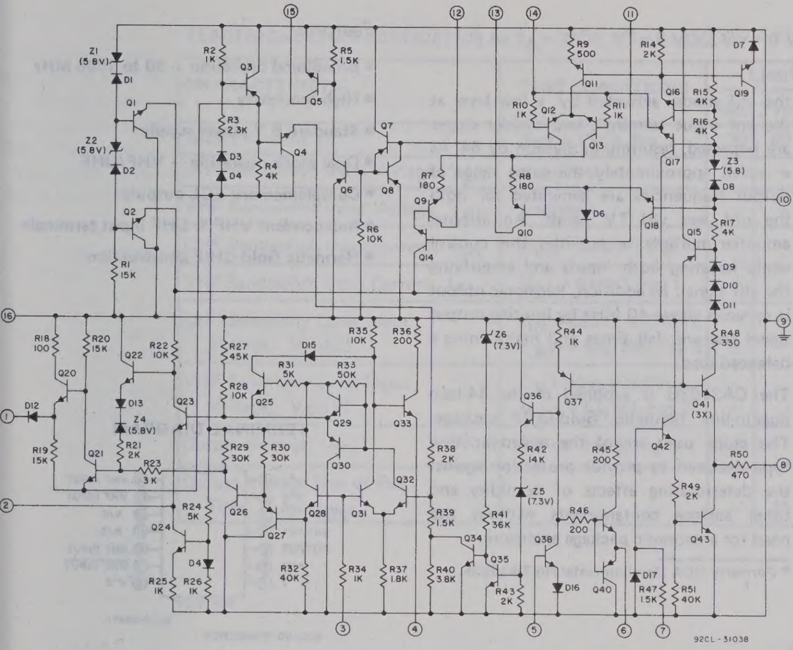


Fig. 3 – Schematic diagram of the CA3159G.

Circuit Description

The negative sync video input at terminal 3 is the detected video if. This video signal is buffered and V_{be} compensated by emitter-followers Q28, Q27, and Q26. The buffered video signal is applied between the base of Q21 and a temperature-stable 2-V reference. Q21 is normally in saturation, and the negative sync pulse imparts a positive swing to the base of Q20. Q20 is used as a peak rectifier driving a capacitor at terminal 1. The voltage at terminal 1 is the AGC control voltage that sets the if gain such that the sync pulses drop to just below the 2 V level, driving Q21 out of saturation.

The above description is for a normal video signal; the presence of noise pulses more negative than the sync tip level would lower the gain to that level, thus disturbing the picture. A gated noise-inversion threshold is provide at the base of Q32 to compensate for these noise pulses. The threshold is about 1.5 V during trace time, but is reduced to about 1 V during coincidence of the sync and flyback pulses. When the video signal is more negative than the noise threshold, Q32 conducts and pulls the base and emitter of Q30 low. Without noise, Q23 conducts 0.5 mA with its collector at 7 V, which holds Q22 in cutoff. Q29 has an emitter load provided by an external 1 kΩ resistor and a series capacitor: when its base is switched low, its collector switches high. The resulting flow of current in Q23 overrides the normal negative-going pulse in the direct signal path and holds Q21 in saturation.

The video input to terminal 3 also operates the sync channel, beginning with Q31. Because Q32 is normally cut off, Q31 acts as an amplifer with a moderate gain to its collector, and a positive sync signal appears at terminal 4. If the noise pulse is more negative than the noise threshold at the base of Q32, the base of Q30 is pulled down as discussed above. In addition to operating the AGC noise inverter, the Q30 current passes through Q25 to the amplifier load resistor, R35, and cancels the potentially positive pulse at that point.

The positive sync signal at terminal 4 is coupled through an RC network to terminal 5 for sync separation. In essence, the network permits Q38 to clamp the positive peaks, so the most positive part of the signal is amplified by Q38 while the rest is beyond cutoff. The separated sync, a negative pulse at the collector of Q38, follows two paths. First, the sync operates an output driver to terminal 6, which drives the outboard diode phase detector. Second, the negative pulse cuts off the current through Q36, which otherwise holds Q35 in saturation, thus enabling a current in R41 to turn Q34 on and thereby shift the noise threshold voltage.

Terminal 7 receives a positive flyback pulse that supplies R41 with the signal to complete the coincidence gate that alters the noise threshold when sync and flyback pulses are in phase. The buffered and clipped flyback pulse also turns Q43 on, which, in conjunction with an external integrating capacitor, forms a sawtooth waveform. This sawtooth (at flyback rate) is phase compared with the sync pulse that was separated from the video input.

The phase detector works against an internal bias point brought out to terminal 10, and the phase detector output applied to terminal 11 is slightly positive or negative relative to terminal 10. This voltage differential with terminal 10 determines the division of current between Q9 and Q10, which are part of the voltage controlled oscillator. The oscillator consists of the current source Q11, differential amplifier Q12 and Q13, and differential amplifier Q9 and Q10. The frequency is determined primarily by a series LC circuit connected between terminals 13 and 14 (terminals 12 and 13 have resistor loads to the positive supply). If the entire oscillator current passes through Q10 to terminal 13, the oscillator operates at the frequency at which the phase shift in the LC circuit is zero. If the current is sent through Q9 to terminal 12, however, it must go through an external capacitor between terminals 12 and 13 and then through the original LC circuit and the circuit is tuned differently. Intermediate proportions of current division will produce intermediate oscillator frequencies. The oscillator current output from Q12 provides base drive for the 31.5 kHz output at terminal 15.

CA3163G

Preliminary Data

VHF/UHF Prescaler

The RCA-CA3163G* is an integrated-circuit prescaler intended for use in TV frequency synthesis tuning systems over an input frequency range of 90 to 1000 MHz. It performs division by 256 in the uhf mode and division by 64 in the vhf mode.

The mode of operation can be selected by means of the bandswitch and the separate uhf and vhf input terminals provided. The output is a complementary emitter-coupled stage with controlled slew rate for harmonic suppression.

All input terminals should be ac coupled to the appropriate input signal source. Because of high sensitivity, unbuffered coupling from the local oscillator is possible in most cases. In the uhf mode, which is activated by applying a high level to the bandswitch input terminal, all eight divider stages are operative, resulting in division by 256. In the vhf mode, activated by a low level at the vhf input terminal, two divider stages are bypassed, resulting in division by 64. As a result, approximately the same range of output frequencies are generated for both the uhf and vhf TV bands. An internal amplifier/multiplexer provides this control while isolating both inputs and amplifying the vhf signal. In addition, harmonic output is reduced above 40 MHz by limiting output signal rise and fall times and maintaining a balanced load.

The CA3163G is supplied in the 14-lead dual-in-line hermetic Gold-CHIP package. The chips used are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure.

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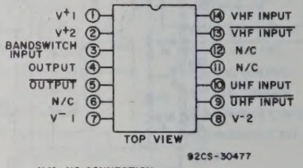
* Formerly RCA Developmental No.TA10535.

Features:

- **Broadband operation – 90 to 1000 MHz**
- **High sensitivity**
- **Standard 5 V power supply**
- **Dual mode operation – VHF/UHF**
- **Complementary ECL outputs**
- **Independent VHF & UHF input terminals**
- **Hermetic Gold-CHIP construction**

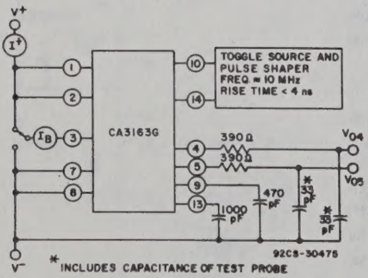
TERMINAL DIAGRAM



N/C = NO CONNECTION

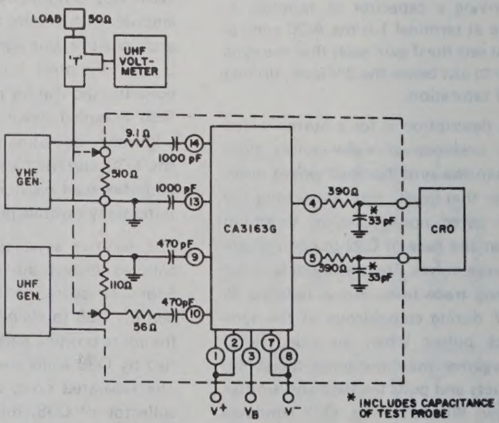
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	5.5	V
DC BANDSWITCH VOLTAGE	20	V
RMS INPUT VOLTAGE	0.5	V
DEVICE DISSIPATION:		
UP TO T_A = 70°C	600	mW
ABOVE T_A = 70°C	derate linearly at 7.5	mW/°C
AMBIENT TEMPERATURE RANGE:		
OPERATING	0 to 70	°C
STORAGE	−55 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):		
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265	°C



*INCLUDES CAPACITANCE OF TEST PROBE

Fig. 1 – DC characteristics test circuit.



* INCLUDES CAPACITANCE OF TEST PROBE

Fig. 2 – AC characteristics test circuit.

ELECTRICAL CHARACTERISTICS At T_A = 25°C, V^+ = 5 VDC, V^- = 0 VDC; see Figs. 1 & 2

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current, I^+	Terms. (1+2), Fig. 1	30	60	90	mA
UHF Bandswitch Input Voltage, V_{BH}	High level	2.4	–		V
VHF Bandswitch Input Voltage, V_{BL}	Low level		–	0.8	V
UHF Bandswitch Input Current, I_{BH}	V_{BH} = 20 VDC, Fig. 1	–	–	0.5	mA
VHF Bandswitch Input Current, I_{BL}	V_{BL} = 0 VDC, Fig. 1	–	–	–1	mA
UHF Sensitivity Level Input Voltage, $V_{IN}(U)$	f_{IN} = 450 to 950 MHz, $f_{OUT} = f_{IN}/256$, Fig. 2	–	–	80	mVRMS
VHF Sensitivity Level Input Voltage, $V_{IN}(V)$	f_{IN} = 90 to 275 MHz, $f_{OUT} = f_{IN}/64$, Fig. 2	–	–	40	mVRMS
Output Voltage, V_O	Terms, 4 or 5, Fig. 2	0.65	1	–	$V_{p\text{-}p}$
Output Voltage Rise of Fall Time, t_r,t_f		–	70	–	ns

CA3166E **Preliminary Data**

Operational Amplifier Bandswitch

BiMOS input operational amplifier, frequency band-select switch, and AFT mode switch

For Frequency-Synthesizer Television Tuning Systems

The RCA-CA3166E incorporates bipolar, PMOS, and CMOS processes on a single monolithic chip to provide three functional blocks for use in frequency-synthesizer type TV tuners. Included are an input operational amplifier, a band-select switch, and an AFT mode switch.

The operational amplifier features internal bias and phase compensation, high-impedance PMOS input transistors, diode clipper input limiting, output short-circuit protection, and static charge protection. The operational amplifier is used to amplify an error signal that is proportional to the detected phase difference between the desired channel frequency and an internally generated reference signal.

The band-select switch has two logic inputs, a control voltage input, and three outputs (UHF, VHF Low, VHF High) with a drive capability of 90 mA each, for controlling the tuner varactor diodes.

The AFT mode switch is a CMOS transmission gate with static charge protection and an enable logic input for selecting the "AFT ON" or "AFT DEFEAT" mode.

The CA3166E is supplied in the 14-lead dual-in-line plastic package.

Features:

- **Three independent functions — input operational amplifier, AFT mode switch, and band-select switc**
- **Input operational amplifier has internal biasing circuitry and high-impedance PMOS input transisto**
- **Internal diode clipper limiting at operational amplif inputs and short-circuit protection at the outputs**
- **Static charge protection for both PMOS and CMOS circuit components**
  - **AFT mode switch utilizes CMOS transmission gate and enable logic inputs control AFT mode**
  - **Logic-controlled band-select switch**
  - **Three band-select-switch outputs, each with 90-mA drive capability (typ.) at input voltage up to 28 V dc**
  - **High voltage-rating for wide dynamic control range of error signals and switch functions**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, V^+	+29.5 to +35 V
DIFFERENTIAL INPUT VOLTAGE	±1.5 V
DC SUPPLY CURRENT I^+	20 mA
BAND-SELECT SWITCH INPUT VOLTAGE RANGE, V_{BS}	0 to +28 V
DEVICE DISSIPATION:	
Up to +70°C	600 mW
Above +70°C	Derate linearly at 11.1 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +70°C
Storage	−55 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

Bandswitch Truth Table

LOGIC INPUTS		OUTPUTS		
A	B	UHF	VHF LOW	VHF HIGH
0	0	0	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

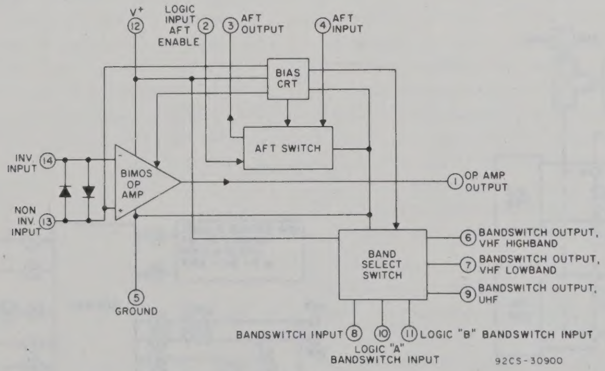
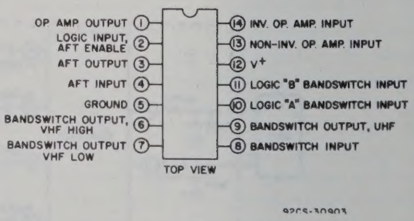


Fig. 1 — CA3166E Block diagram.

CA3166E TERMINAL ASSIGNMENT


OP AMP OUTPUT ①
LOGIC INPUT, AFT ENABLE ②
AFT OUTPUT ③
AFT INPUT ④
GROUND ⑤
BANDSWITCH OUTPUT, VHF HIGH ⑥
BANDSWITCH OUTPUT VHF LOW ⑦
⑭ INV. OP. AMP. INPUT
⑬ NON-INV. OP. AMP. INPUT
⑫ V+
⑪ LOGIC "B" BANDSWITCH INPUT
⑩ LOGIC "A" BANDSWITCH INPUT
⑨ BANDSWITCH OUTPUT, UHF
⑧ BANDSWITCH INPUT
TOP VIEW
92CS-30903

Operational Amplifier (See Fig. 2)
Electrical Characteristics at T_A = 25°C, $V^{\pm}$ = 32.5 V, V_{BS} = 18 V, Terms 4 & 5 grounded

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES	UNITS
Input Bias Voltage, V_{13}	I_{13} = 4 mA, Feedback = 1 MΩ	2.5	V_{DC}
Input Bias Voltage, V_{13}	I_{13} = 6 mA, Feedback = 1 MΩ	2.6	V_{DC}
Input Bias Voltage, V_{14}	I_{14} = 4 mA, Feedback = 1 MΩ	3.3	V_{DC}
Diode Voltage (term. 14 to term. 13)	I_{14} = 4 mA, Term. 13 = Reference	0.8	V_{DC}
Diode Voltage (term. 13 to term. 14)	I_{13} = 4 mA, Term. 14 = Reference	0.8	V_{DC}
Output Voltage Low, V_{OL}	I_{14} = 4 mA, Resistance between Terms. 1 and 12 = 10 kΩ	0.2	V_{DC}
Output Voltage High, V_{OH}	V_{14} = 0 V, I_{13} = 4 mA, Resistance between Terms. 1 and 12 = 10 kΩ	28	V_{DC}
Input Offset Voltage, V_{IO}	V_{13} = 0 V, Term. 1 connected to Term. 14	10	mV
Supply Current, I^+	V_4 = 1 V, Feedback (Terms. 1 to 14) = 1 MΩ	14	mA
Output Sink Current, I_{OL}	I_{14} = 4 mA, V_1 = 32.5 V	25	mA
Output Source Current, I_{OH}	I_{13} = 4 mA, V_1 = V_{14} = 0V	–15	mA
Input Bias Current, I_{IB} (term. 14)	V_{13} = 0 V, Term. 1 connected to Term. 14	0.5	nA
Common-Mode Rejection Ration, CMRR		65	dB
Power Supply Rejection Ratio, PSRR		75	dB
Open-Loop Voltage Gain, A_{OL}		80	dB

Band-Select Switch (See Fig. 3)
Electrical Characteristics at T_A = 25°C, V^+ = 32.5 V, V_{BS} = 18 V, Terms. 4 & 5 grounded
Terms. 6, 7, 9 = 100 kΩ to ground

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES	UNITS
Logic Inputs "A" & "B" Sink Current		100	μA
Logic Inputs "A" & "B" Source Current	I_9 = –90 mA, V_{10} = V_{11} = 2.4 V	–5	μA
Output Leakage Current, Terms. 6, 7, 9		2	μA
Output Saturation Voltage:			
Term. 9	I_9 = –90 mA, V_{10} = V_{11} = 2.4 V	0.6	V
Term. 9	I_9 = –60 mA, V_{10} = V_{11} = 24 V	0.3	V
Term. 7	I_7 = –90 mA, V_{10} = 0 V, V_{11} = 24 V	0.6	V
Term. 7	I_7 = –60 mA, V_{10} = 0 V, V_{11} = 2.4 V	0.3	V
Term. 6	I_6 = –90 mA, V_{10} = 2.4 V, V_{11} = 0 V	0.6	V
Term. 6	I_6 = –60 mA, V_{10} = 24 V, V_{11} = 0 V	0.3	V

AFT Mode Switch

Electrical Characteristics at $T_A = 25°C$, $V^+ = 32.5$ V, $V_{BS} = 18$ V, Terms. 5, 10, 11 grounded

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES	UNITS
Logic Input Current Low	$V_2 = 0$ V, $R_{TERM.\,3} = 10$ MΩ, $V_4 = 13.5$ V	−100	µA
Logic Input Current High	$V_2 = 2.4$ V, $R_{TERMS.\,3} = 1$ kΩ, $V_4 = 1$ V	2	µA
Input Current	$V_2 = 0$ V, $R_{TERM.\,3} = 10$ MΩ, $V_4 = 13.5$ V	2	µA
Output Leakage Current	$V_2 = 0.6$ V, $V_3 = 8$ V, $V_4 = 0$ V	1	nA
Output Sink Current	$V_2 = 2.4$ V, $V_3 = 1.8$, $V_4 = 0$ V	2	mA
Output Offset Voltage	$V_2 = 2.4$ V, $V_4 = 3$ V	0.1	V
Output Voltage, "ON"	$V_2 = 2.4$ V, $R_{TERM.\,3} = 1$ kΩ, $V_4 = 1$ V	0.8	V
Output Voltage, "ON"	$V_2 = 2.4$ V, $R_{TERM.\,3} = 1$ kΩ, $V_4 = 13.5$ V	10	V

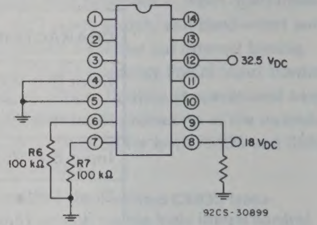
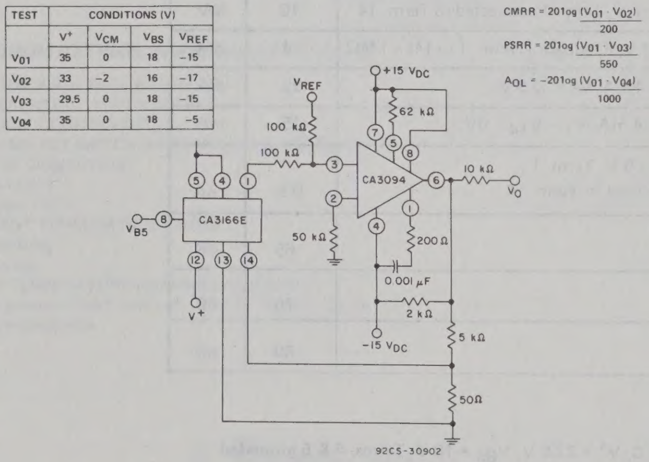


Fig. 3 – Bandswitch test circuit.



TEST	CONDITIONS (V)			
	V^+	V_{CM}	V_{BS}	V_{REF}
V_{01}	35	0	18	−15
V_{02}	33	−2	16	−17
V_{03}	29.5	0	18	−15
V_{04}	35	0	18	−5

$$\text{CMRR} = 20\log\frac{(V_{01}\cdot V_{02})}{200}$$

$$\text{PSRR} = 20\log\frac{(V_{01}\cdot V_{03})}{550}$$

$$A_{OL} = -20\log\frac{(V_{01}\cdot V_{04})}{1000}$$

Fig. 2 – Operational amplifier test circuit for CMRR, PSRR, and A_{OL}.

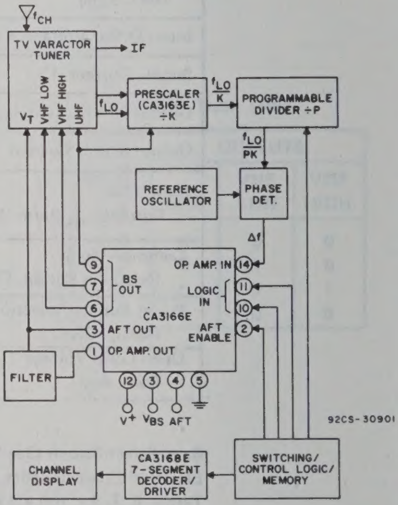


Fig. 4 – Block diagram of a typical digital tuning system.

Turner Operation

Fig. 4 shows a typical digital TV tuning system employing the CA3166E. This system consists of a phase-locked loop (PLL) and a programmable divider to generate a tuner local-oscillator frequency that is an integral multiple of a reference-oscillator frequency. The output of the local oscillator is connected to a prescaler (CA3163) which divides the frequency to values that can be processed by a programmable divider. The amount of division is established by the control logic and depends on the desired channel to be viewed. This signal and a reference signal are combined in a phase detector to produce an error signal proportional to the frequency separation. The error signal is then amplified by the CA3166E and filtered to provide a dc voltage to the varactors of the tuner voltage-controlled oscillator (VCO). The VCO frequency is thus corrected to reduce its difference with the reference.

Logic-control signals are applied to terminals 10 and 11 (band-select switch) of the CA3166E, and the proper varactor circuits for UHF, low-band VHF, or high-band VHF are selected. The truth table for the selection logic is shown on page 3.

An analog switch for AFT operation is included in the CA3166E for automatic correction of frequency transmission errors.

Preliminary Data

CA3168E

2-Digit BCD-to-7-Segment Decoder/Driver

For Common-Anode LED Displays

The RCA-CA3168E is a monolithic integrated circuit intended for 2-digit display such as "numbers" for TV and "CB" channel selection, and other 0-99 numerical or counting for consumer or industrial indicator applications. It consists of two independent BCD-to-7-segment decoder/drivers. Two sets of BCD inputs are buffered with p-n-p differential amplifier stages internally referenced to 1.7 V. Each of the eight input terminals draws less than 15 μA and is provided with an internal protection circuit.

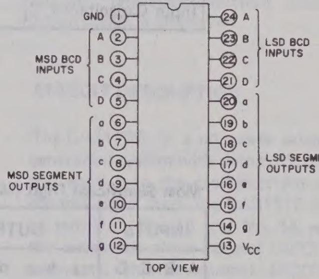
Decoding is accomplished with I^2L ROM's. The fourteen output terminals are buffered with Darlington pairs driving common-emitter output transistors. Each output is capable of sinking 25 mA for an LED common-anode display device. The supply-voltage range (V_{CC}) is intended to be 4.5 V to 6 V. The output voltage (V_O) must not exceed 12 V, which provides for a wide range of common-anode voltage sources.

The CA3168E is supplied in the 24-lead dual-in-line plastic package.

Features:

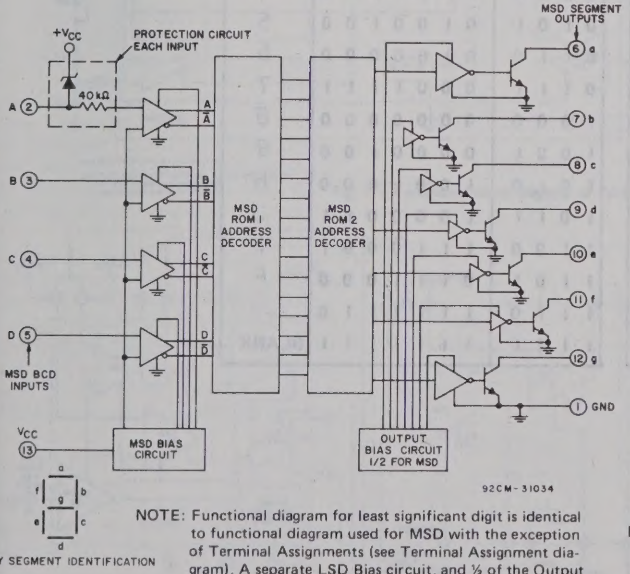
- Separate BCD inputs and segment outputs for each digit
- Input loading less than 15 μA
- I^2L logic with buffered inputs and outputs
- Internal input overrange protection circuit
- 5-V supply operation
- Internal biasing circuits
- Output drive capability of 25 mA per segment
- Open collector outputs drive indicators directly

CA3168E
TERMINAL ASSIGNMENT



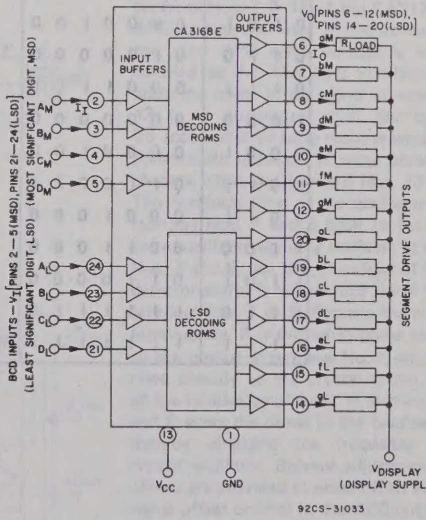
MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY-VOLTAGE, V_{CC}	6 V
INPUT-VOLTAGE (MIN./MAX.)	$-0.3/V_{CC}$ V
INPUT CURRENT (PROTECTION CIRCUIT)	±10 mA
UTPUT VOLTAGE, V_O	12 V
UTPUT SEGMENT CURRENT, $I_{DISPLAY}$	25 mA
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +70°C
Storage	−55 to +150°C
OWER DISSIPATION:	
Up to +70°C	400 mW
Above +70°C	derate linearly at 8.7 mW/°C
EAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C


$+V_{CC}$
PROTECTION CIRCUIT EACH INPUT
40 kΩ
A ②
B ③
C ④
D ⑤
MSD BCD INPUTS
V_{CC} ⑬
MSD BIAS CIRCUIT
MSD ROM 1 ADDRESS DECODER
MSD ROM 2 ADDRESS DECODER
OUTPUT BIAS CIRCUIT 1/2 FOR MSD
MSD SEGMENT OUTPUTS
⑥ a
⑦ b
⑧ c
⑨ d
⑩ e
⑪ f
⑫ g
① GND
92CM-31034
a
b
c
d
e
f
g
LAY SEGMENT IDENTIFICATION

NOTE: Functional diagram for least significant digit is identical to functional diagram used for MSD with the exception of Terminal Assignments (see Terminal Assignment diagram). A separate LSD Bias circuit, and ½ of the Output Bias Circuit is used for LSD.

Fig. 1 – Functional diagram for Most Significant Digit (MSD).



NOTE: See truth table for test sequence of input/output logic tests and Minimum $R_{LOAD} = \dfrac{V_{DISPLAY} - V_{OL}}{\text{Max. } I_{DISPLAY}}$ For each of the 14 segment drive output terminals. (LED is not used in test circuit)

Fig. 2 – Test circuit.

TYPICAL ELECTRICAL CHARACTERISTICS at V_{CC} = 5 V, V_1 = GND, $V_{DISP.}$ = 12 V, and T_A = 25°C, See Fig. 2
Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Voltage High, V_{IH}		2.4	5	V_{CC}	V
Input Voltage Low, V_{IL}		0	–	0.6	V
Input Current High, I_{IH}	All BCD Inputs = 5 V	–	–	15	μA
Input Current Low, I_{IL}	All BCD inputs = 0 V	−10	–	–	μA
On-State Output Voltage, V_{OL}	$I_{O(Sink)}$ = 25 mA	–	–	1	V
Off-State Output Current, I_{OH}		–	5	50	μA
Power Supply Drain Current, I_{CC}	V_{CC} = 6 V	–	17	25	mA
Input Capacitance, C_I		–	5	–	pF

TRUTH TABLES

Most Significant Digit (MSD)

INPUTS	OUTPUTS	DISPLAY
A B C D	a b c d e f g	
0 0 0 0	0 0 0 0 0 0 1	0
0 0 0 1	1 0 0 1 1 1 1	1
0 0 1 0	0 0 1 0 0 1 0	2
0 0 1 1	0 0 0 0 1 1 0	3
0 1 0 0	1 0 0 1 1 0 0	4
0 1 0 1	0 1 0 0 1 0 0	5
0 1 1 0	0 1 0 0 0 0 0	6
0 1 1 1	0 0 0 1 1 1 1	7
1 0 0 0	0 0 0 0 0 0 0	8
1 0 0 1	0 0 0 0 1 0 0	9
1 0 1 0	0 1 1 0 0 0 1	C
1 0 1 1	0 0 0 1 0 0 0	A
1 1 0 0	0 0 1 1 0 0 0	P
1 1 0 1	0 1 1 0 0 0 0	E
1 1 1 0	1 1 1 1 1 1 0	–
1 1 1 1	1 1 1 1 1 1 1	BLANK

Least Significant Digit (LSD)

INPUTS	OUTPUTS	DISPLAY
A B C D	a b c d e f g	
0 0 0 0	0 0 0 0 0 0 1	0
0 0 0 1	1 0 0 1 1 1 1	1
0 0 1 0	0 0 1 0 0 1 0	2
0 0 1 1	0 0 0 0 1 1 0	3
0 1 0 0	1 0 0 1 1 0 0	4
0 1 0 1	0 1 0 0 1 0 0	5
0 1 1 0	0 1 0 0 0 0 0	6
0 1 1 1	0 0 0 1 1 1 1	7
1 0 0 0	0 0 0 0 0 0 0	8
1 0 0 1	0 0 0 0 1 0 0	9
1 0 1 0	1 0 0 1 0 0 0	H
1 0 1 1	1 0 0 0 0 1 1	J
1 1 0 0	1 1 1 0 0 0 1	L
1 1 0 1	0 1 1 1 0 0 0	F
1 1 1 0	1 1 1 1 1 1 0	–
1 1 1 1	1 1 1 1 1 1 1	BLANK

TV Chroma System

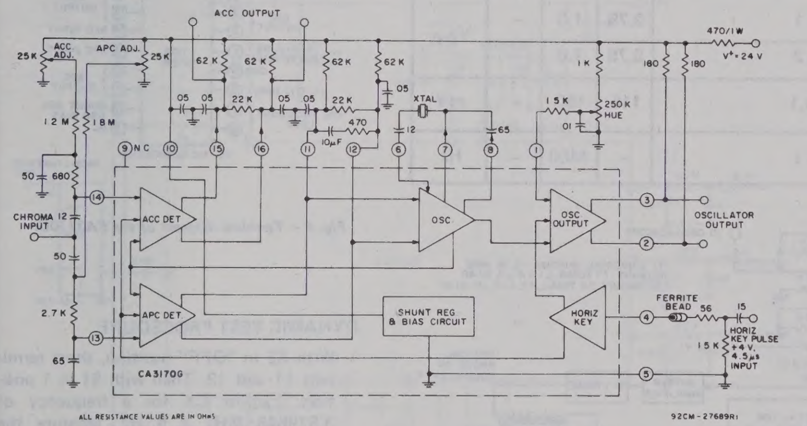
"G" Suffix Type-Hermetic Gold-CHIP in Dual-In-Line Plastic Package

The RCA-CA3170G is a monolithic silicon integrated circuit that performs the functions of subcarrier regeneration, ACC and APC detection, and tint control in color television receivers. It is designed to function compatibly with the CA3121E TV Chroma Amplifier/Demodulator in a 2-package chroma system.

The CA3170G is a TV Chroma System of advanced design that incorporates all the features of the CA3070E but with the added advantage of the modified Hue Control Characteristic. With the CA3170G, the designer can provide a front panel hue control that functions linearly over its entire range, a particularly desirable consumer feature.

MAXIMUM RATINGS, *Absolute-Maximum:*

DEVICE DISSIPATION:*
Up to $T_A = 55^\circ C$ . . . . 750 mW
Above $T_A = 55^\circ C$ . . . . derate linearly 7.9 mW/°C
AMBIENT–TEMPERATURE RANGE:
Operating . . . . −40 to +85°C
Storage . . . . −65 to +150°C
LEAD TEMPERATURE (During soldering):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm)
from case for 10 s max. . . . . +265°C



ALL RESISTANCE VALUES ARE IN OHMS
UNLESS OTHERWISE INDICATED ALL CAPACITANCE VALUES LESS THAN 1.0 ARE IN MICROFARADS
1.0 OR GREATER ARE IN PICOFARADS

Fig. 1 — Functional block diagram of CA3170G.

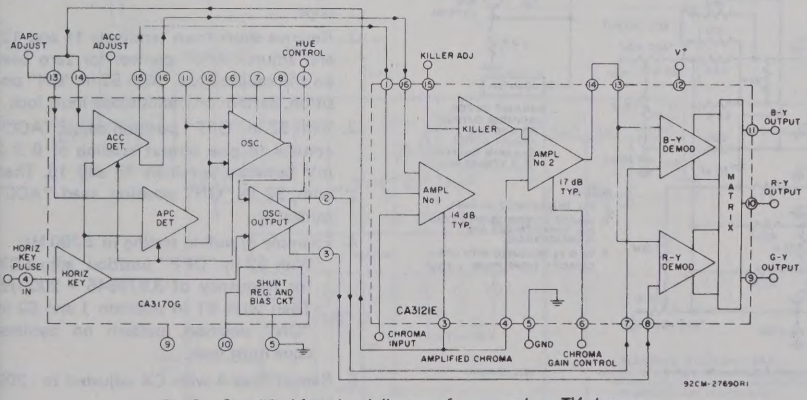


Fig. 2 — Simplified functional diagram of a two-package TV chroma system utilizing the CA3170G and CA3121E.

Features:

- **Voltage-controlled oscillator**
- **Keyed APC and ACC detectors**
- **DC hue control**
- **Shunt regulator**

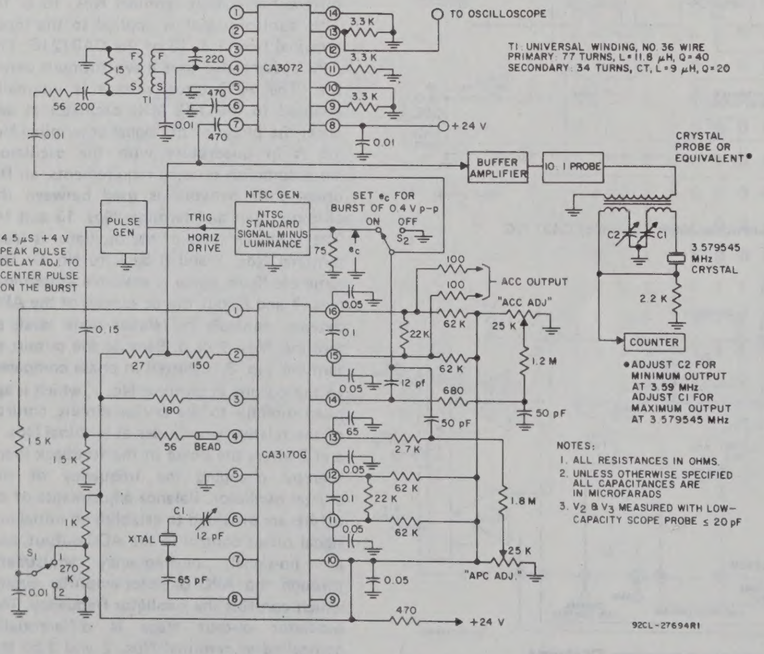
The CA3170G is supplied in the 16-lead dual-in-line plastic package with a hermetic Gold-CHIP (G suffix). The chips used in the hermetic Gold-CHIP plastic packages are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multilayered, highly corrosion-resistant, terminal-connection system of unique design is employed.

CIRCUIT DESCRIPTION

The CA3170G is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3121E is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval. The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 16 of the CA3121E. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator. To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue

ELECTRICAL CHARACTERISTCS, at T_A = 25°C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SPECIAL TEST CONDITIONS		LIMITS CA3170G MIN.	LIMITS CA3170G TYP.	LIMITS CA3170G MAX.	UNITS
Static Characteristics						
Voltage: Hue Control, V_1	See Fig.7					V
Oscillator Input, V_6		S_1 CLOSED S_3 OFF; S_2, S_4, S_5 OPEN See Fig. 8	–	2.6	–	
APC Input, V_{13}			–	5.4	–	
Regulator, V_{10}	V^+ = 21 V		11	12.3	13.5	
Regulator Change, V_{10}	V^+ = 27 V		-0.2	–	+0.2	
Horizontal Key Input, V_4	I_4 = -10 µA		5	–	–	
Currents: Oscillator Output, I_2	S_1, S_2, S_4, S_5 CLOSED, S_3 in position 2, See Fig. 8		–	5.8	–	mA
APC Output, I_{11}, I_{12}	S_1, S_5 OPEN, S_2, S_4 CLOSED, S_3 in position 1, See Fig. 8		–	1.45	–	
ACC Output, I_{15}, I_{16}			–	1.45	–	
Dynamic Characteristics (See Figure 6)						
Oscillator Outputs: Terminal No. 2, V_2	S_1 in position 1		0.75	1.0	–	V_{p-p}
Terminal No. 3, V_3	S_1 in position 2		0.75	1.0	–	
ACC Detected Output V_{16} - V_{15}	S_1 in position 1		115	150	–	mV
Oscillator Pull-In Range	S_1 in position 1		–	±400	–	Hz



T1: UNIVERSAL WINDING, NO. 36 WIRE
PRIMARY: 77 TURNS, L = 11.8 µH, Q = 40
SECONDARY: 34 TURNS, CT, L = 9 µH, Q = 20

*ADJUST C2 FOR MINIMUM OUTPUT AT 3.59 MHz
ADJUST C1 FOR MAXIMUM OUTPUT AT 3.579545 MHz

NOTES:
1. ALL RESISTANCES IN OHMS.
2. UNLESS OTHERWISE SPECIFIED ALL CAPACITANCES ARE IN MICROFARADS
3. V_2 & V_3 MEASURED WITH LOW-CAPACITY SCOPE PROBE ≤ 20 pF

Fig. 5 – Dynamic characteristics test circuit.

phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3170G includes a shunt regulator to establish a 12-volt dc supply.

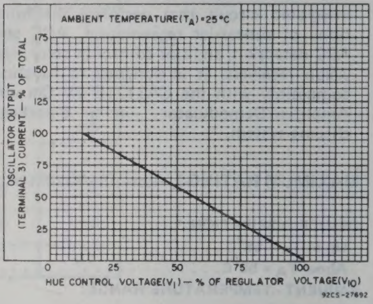


Fig. 3 – Typical hue control characteristic.

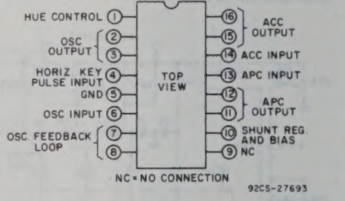


Fig. 4 – Terminal diagram of the CA3170G.

DYNAMIC TEST PROCEDURE

1. With S2 in "OFF" position, short terminals 11 and 12. Then with S1 in 1 position, adjust CX for a frequency of 3.579545 MHz ± 5 Hz. Measure the frequency using the frequency counter or by zero beat indication on the oscilloscope.
2. Remove short from terminals 11 and 12, and adjust "APC" control for zero beat on the oscilloscope. With S2 in "ON" position, pattern on oscilloscope must lock.
3. With S2 in "OFF" position adjust "ACC" control to give output reading of 0 ± 2 mV between terminals 15 and 16. Then with S2 in "ON" position, read "ACC" output.
4. Example of pull-in testing to ± 200 Hz:
   With S2 in "OFF" position, adjust CX for frequency of 3.579545 + 200 Hz. Then with S1 in position 1 and S2 in "ON" position, pattern on oscilloscope must lock.
5. Repeat Step 4 with CX adjusted to - 200 Hz.

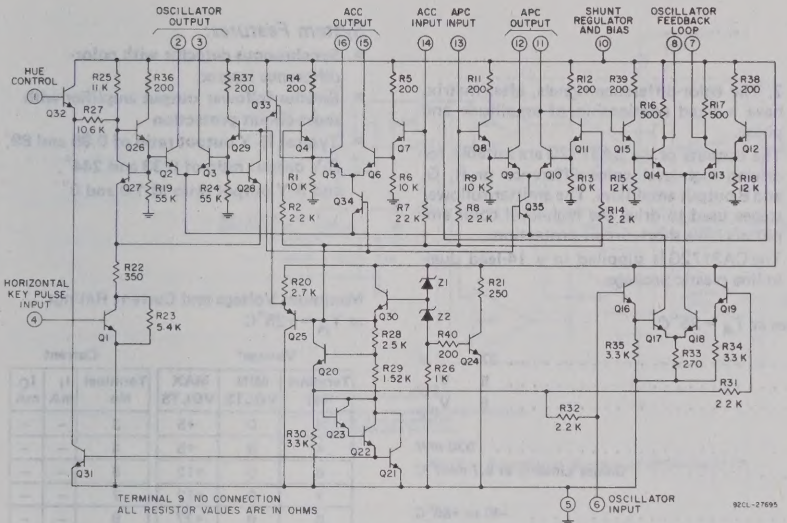


Fig. 6 – Schematic diagram of the CA3170G.

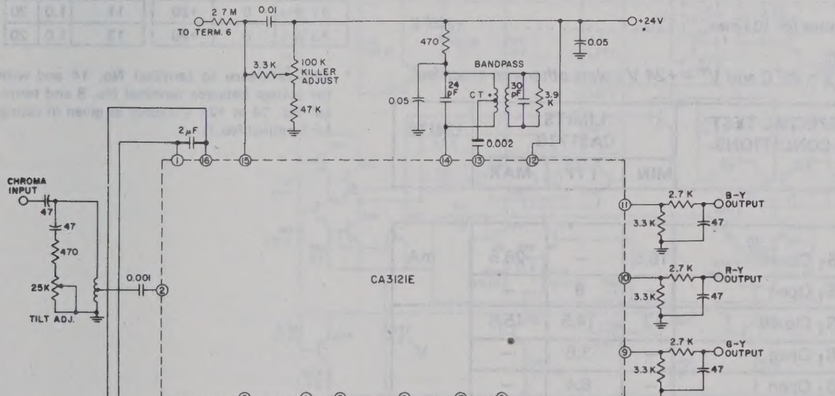

TO TERM. 6
+24V
KILLER ADJUST
BANDPASS
CHROMA INPUT
TILT ADJ.
CA3121E
B-Y OUTPUT
R-Y OUTPUT
G-Y OUTPUT
CHROMA GAIN CONT.
APC ADJ
ACC ADJ
CA3170G
FERRITE BEAD
HUE
HORIZ. KEY PULSE +4V, 4.5 μs INPUT
RESISTANCE VALUES ARE IN OHMS.
UNLESS OTHERWISE INDICATED, ALL CAPACITANCE VALUES LESS THAN 1 ARE IN MICROFARADS, 1 OR GREATER ARE IN PICOFARADS.
92CL-27688R1

Fig. 7 – Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3121E and CA3170G.

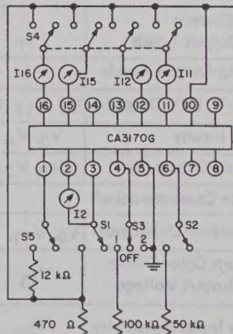


Fig. 8 – Static characteristics test circuit

CA3172G

TV Chroma Demodulator

The RCA-CA3172G is a monolithic silicon integrated circuit intended for use as a chroma demodulator in TV applications. It is operated from a 24-volt supply.

The device has synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color-difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4, while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color-difference signals, after matrix, have a fixed relationship of amplitude and phase.

The outputs of the CA3172G are suitable for driving high-level color-difference or R, G, and B output amplifiers. The emitter-follower stages used to drive the high-level color amplifiers have short-circuit protection.

The CA3172G is supplied in a 14-lead dual-in-line plastic package.

System Features:

- **Synchronous detector with color-difference matrix**
- **Emitter-follower output amplifier with short-circuit protection**
- **Typical R-Y output ratio of 0.95 and 89°, G-Y output ratio of 0.33 and 244°, and B-Y output ratio of 1.0 and 0°**

MAXIMUM RATINGS, ***Absolute Maximum-Values at T_A = 25°C***

DC SUPPLY VOLTAGE (Terminal 8 to Terminal 14)	27 V
REFERENCE INPUT VOLTAGE	5 V_{p-p}
CHROMA INPUT VOLTAGE	5 V_{p-p}
DEVICE DISSIPATION:	
Up to T_A = +70°C	530 mW
Above T_A = +70°C	Derate Linearly at 6.7 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/32 in. (3.17 mm) from seating plane for 10 s max.	+265°C

Maximum Voltage and Current Ratings at T_A = +25°C

Voltage*			Current		
Terminal No.	MIN VOLTS	MAX VOLTS	Terminal No.	I_I mA	I_O mA
3	0	+5	3	–	–
4	0	+5	4	–	–
6	0	+12	6	–	–
7	0	+12	7	–	–
8	0	+27	8	–	–
9	0	+20	9	1.0	20
11	0	+20	11	1.0	20
13	0	+20	13	1.0	20

* With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C and V^+ = +24 V unless otherwise specified*

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3172G			UNITS
			MIN.	TYP.	MAX.	
Static Characteristics[a]						
Supply Current With Output Loads	I_T	S_1 Closed	16.5	–	28.5	mA
With No Output Loads		S_1 Open	–	9	–	
G-Y, R-Y, B-Y Outputs	V_9 V_{11}, V_{13}	S_1 Closed	13	14.5	15.5	V
Chroma Inputs	V_3, V_4	S_1 Open	–	3.6	–	
Reference Subcarrier	V_6, V_7	S_1 Open	–	6.4	–	
Dynamic Characteristics[b]						
Demodulator Unbalance	V_9, V_{11}, V_{13}	$V_3 = V_4 = 0$	–	–	0.6	V_{p-p}
Maximum Color Difference Output Voltage	V_{13}	$V_3 = V_4 = 0.35\ V_{p-p}$	5	–	–	V_{p-p}
Chroma Input Sensitivity	V_3	Adjust e_c for 5.0 V_{p-p} @ term No. 13 (B-Y)	–	0.2	0.35	
R-Y Output Ratio	V_{11}		–	0.95	–	
G-Y Output Ratio	V_9		–	0.32	–	
V_{DC} Difference Between any two Output Terminals	$\|V_9\| - \|V_{11}\|$ $\|V_9\| - \|V_{13}\|$ $\|V_{11}\| - \|V_{13}\|$	$e_c = 0$	–	–	0.6	V
Input Impedance Reference Subcarrier	$R_i6, 7$ $C_i6, 7$		– –	1.7 6	– –	kΩ pF
Input Impedance at Chroma Inputs	$R_i3, 4$ $C_i3, 4$		– –	0.95 6	– –	kΩ pF
Output Resistance	R_o9, R_o11, R_o13		–	180	–	Ω

[a] Test circuit Fig. 3

[b] Test circuit Fig. 4

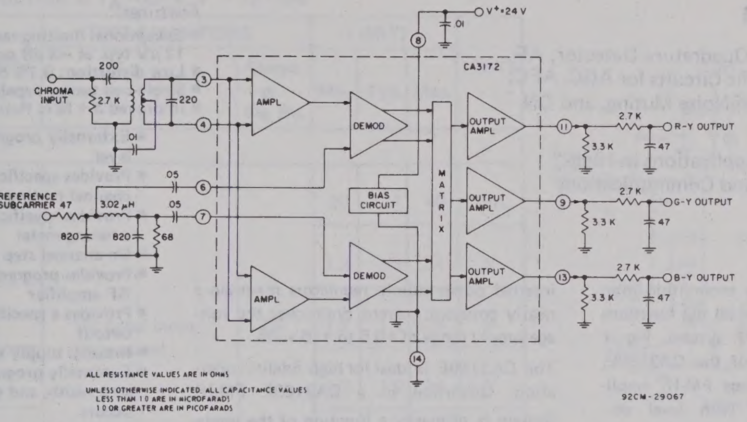


Fig. 1 – Functional diagram of RCA-CA3172.

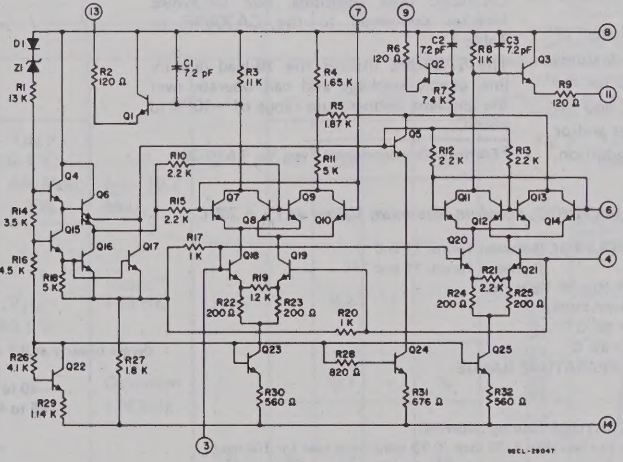


Fig. 2 – Schematic diagram for CA3172.

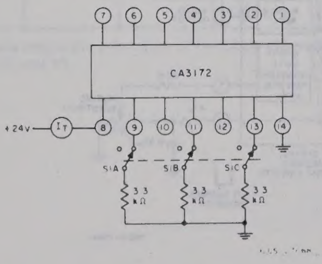


Fig. 3 – Static characteristics test circuit.

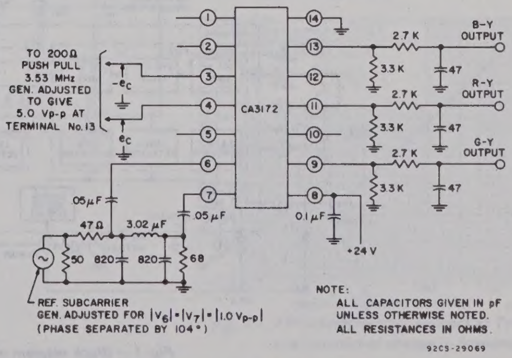

TO 200Ω PUSH PULL 3.53 MHz GEN. ADJUSTED TO GIVE 5.0 Vp-p AT TERMINAL No. 13
-ec
ec
CA3172
.05 µF
47 Ω
3.02 µF
50
820
820
68
.05 µF
0.1 µF
+24 V
2.7 K
3.3 K
47
B-Y OUTPUT
R-Y OUTPUT
G-Y OUTPUT
REF. SUBCARRIER GEN. ADJUSTED FOR |V6|=|V7|=|1.0 Vp-p| (PHASE SEPARATED BY 104°)
NOTE: ALL CAPACITORS GIVEN IN pF UNLESS OTHERWISE NOTED. ALL RESISTANCES IN OHMS.
92CS-29069

Fig. 4 – Dynamic characteristics test circuit.

CA3189E

FM IF System

Includes IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Tuning Meter, Deviation-Noise Muting, and ON Channel Detector

For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers

Features:

- **Exceptional limiting sensitivity: 12 μV typ. at −3 dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **Improved S + N/N Ratio**
- **Externally programmable recovered audio level**
- **Provides specific signal for control of inter-channel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **On channel step for search control**
- **Provides programmable AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible audio output**
- **Internal supply-voltage regulators**
- **Externally programmable "on" channel step width, and deviation at which muting occurs**

The RCA-CA3189E* is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 shows a block diagram of the CA3189E, which includes a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power-supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3189E is ideal for high-fidelity operation. Distortion in a CA3189E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3189E has all the features of the CA3089E plus additions. See CA3189E features compared to the CA3089E in Table I.

The CA3189E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

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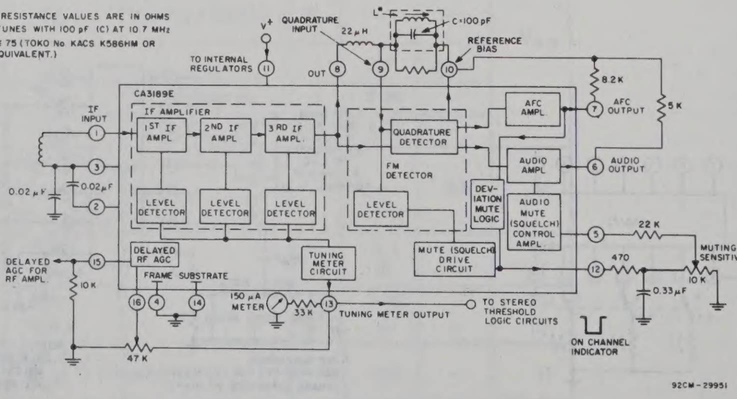
* Formerly Developmental Type No. TA10038.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$:*

DC SUPPLY VOLTAGE (between Terms. 11 and 4)	16 V
(between Terms. 11 and 14)	16 V
DC CURRENT (Out of Term. 15)	2 mA
DEVICE DISSIPATION:	
Up to $T_A = 85^\circ C$	640 mW
Above $T_A = 85^\circ C$	derate linearly at 9.9 mW/°C
AMBIENT-TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During soldering):	
At distance not less than 1/32 inch (0.79 mm) from case for 10s max.	+265°C



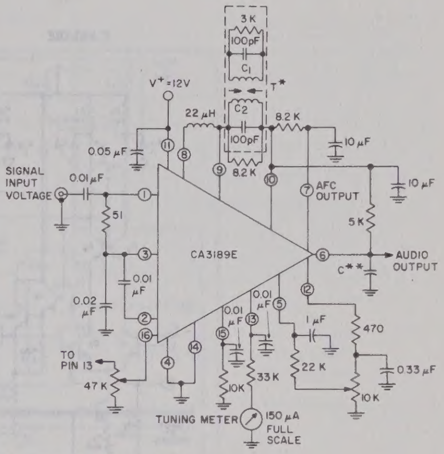
ALL RESISTANCE VALUES ARE IN OHMS
* L TUNES WITH 100 pF (C) AT 10.7 MHz
$Q_O \cong 75$ (TOKO No. KACS K586HM OR EQUIVALENT.)

Fig. 1 — Block diagram of the CA3189E.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V^+ = 12 Volts

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
				Circuit or Fig. No.	Min.	Typ.	Max.	
Static (DC) Characteristics								
Quiescent Circuit Current	I_{11}	No signal input, Non muted		2,6	20	31	40	mA
DC Voltages: Terminal 1 (IF Input)	V_1				1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2				1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3				1.2	1.9	2.4	V
Terminal 15 (RF AGC)	V_{15}				7.5	9.5	11	V
Terminal 10 (DC Reference)	V_{10}				5	5.6	6	V
Dynamic Characteristics								
Input Limiting Voltage (−3 dB point)	V_I(lim)		f_O = 10.7 MHz,	2,6	–	12	25	μV
AM Rejection (Term. 6)	AMR	V_{IN} = 0.1 V, AM Mod. = 30%			45	55	–	dB
Recovered AF Voltage (Term. 6)	V_O(AF)				325	500	650	mV
Total Harmonic Distortion:* Single Tuned (Term. 6)	THD	V_{IN} = 0.1 V	$f_{mod.}$ = 400 Hz, Deviation ±75 kHz	6	–	0.5	1	%
Double Tuned (Term. 6)	THD			2	–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)	S + N/N			2,6	65	72	–	dB
Deviation Mute Frequency	$f_{DEV.}$		$f_{mod.}$ = 0	4,6,7	–	±40	–	kHz
RF AGC Threshold	V_{16}			2,6	–	1.25	–	V
On Channel Step	V_{12}	V_{IN} = 0.1 V	$f_{DEV.}$ < ±40 kHz	6	–	0	–	V
			$f_{DEV.}$ > ±40 kHz		–	5.6	–	

*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.



ALL RESISTANCE VALUES ARE IN OHMS

*T: PRI. – Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20t OF 34e ON 7/32" DIA. FORM

SEC. – Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20t OF 34e ON 7/32" DIA. FORM

kQ (PER CENT OF CRITICAL COUPLING) ≅ 70% (ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV

ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT "E" TYPE SLUGS, SPACING 4 mm

**C = 0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)
= 0.015 μF FOR 75 μs DEEMPHASIS (USA)

92CM-29954

Fig. 2 – Test circuit for CA3189E using a double-tuned detector coil.

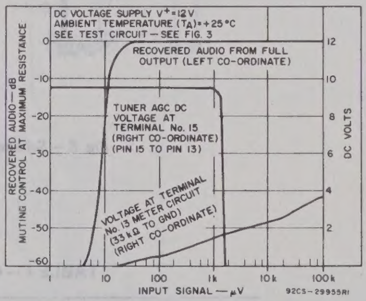


Fig. 3 – Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

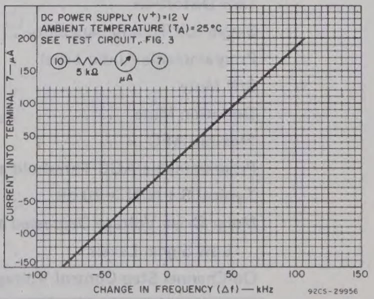


Fig. 4 – AFC characteristics (current at Term. 7 as a function of change in frequency).

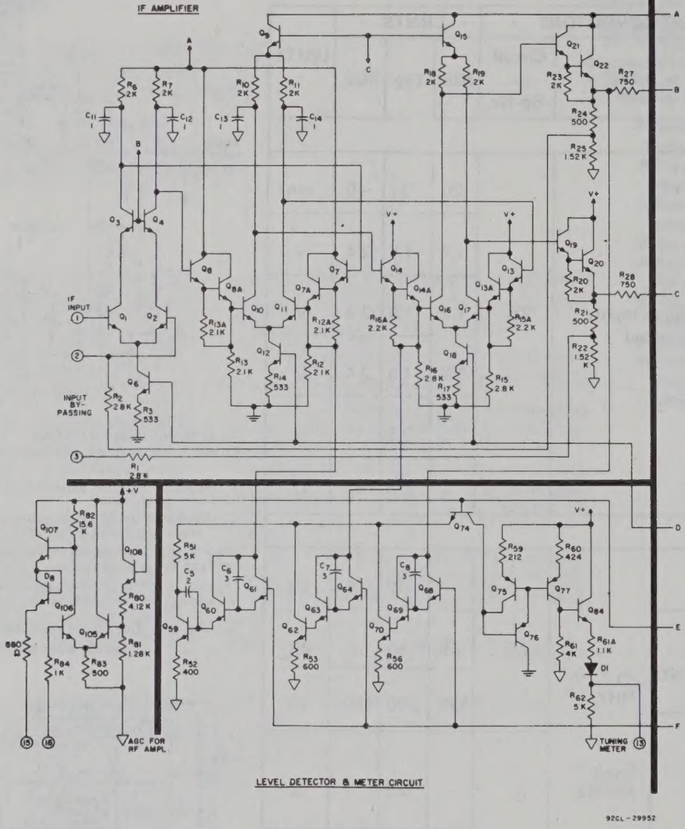
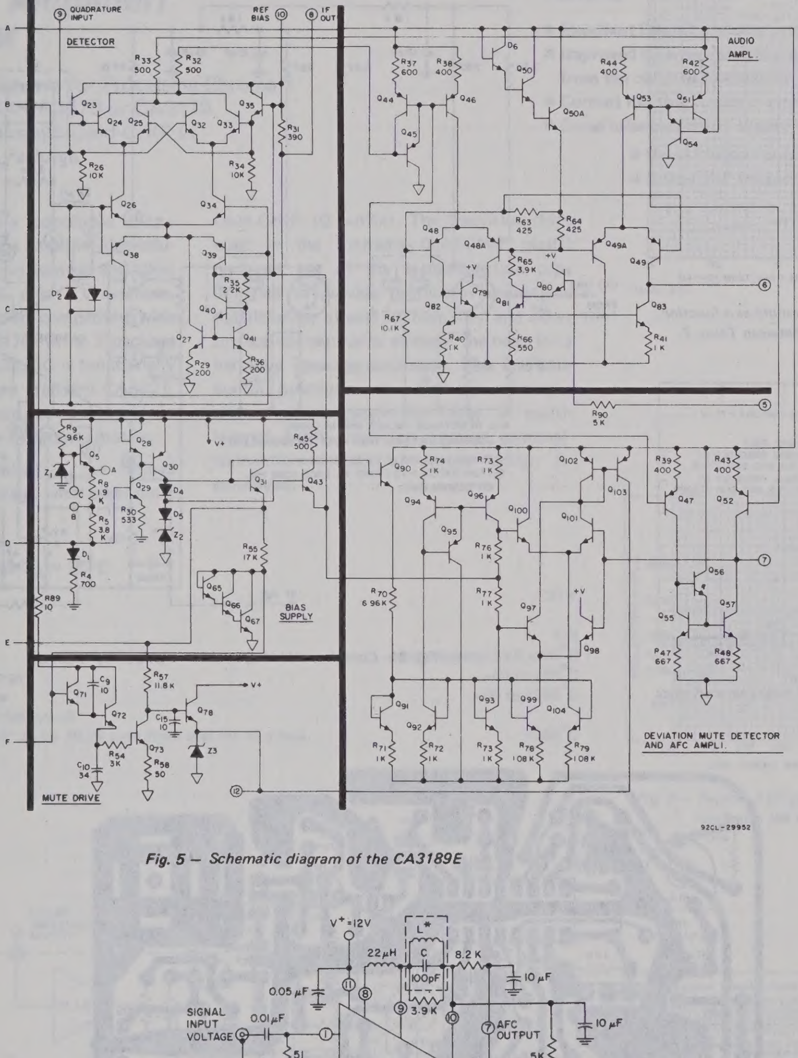


Fig. 5 – Schematic diagram of the CA3189E

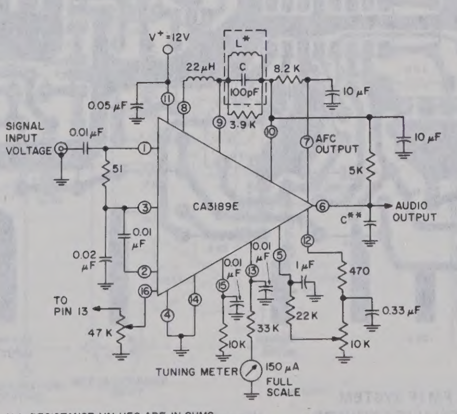
TABLE I – CA3189E Features Compared to CA3089E

FEATURES	CA3189E	CA3089E
Low Limiting Sensitivity (12 μV typ.)	Yes	Yes
Low Distortion	Yes	Yes
Single-coil Tuning Capability	Yes	Yes
Programmable Audio Level	Yes	No
S/N Mute	Yes	Yes
Deviation Mute	Yes	No
Flexible AFC	Yes	Yes
Programmable AGC Threshold and Voltage	Yes	No
Typical S + N/N > 70 dB	Yes	No
Meter Drive Voltage Depressed at Very- Low Signal Levels	Yes	No
On-Channel Step Control Voltage	Yes	No



92CL-29952

Fig. 5 – Schematic diagram of the CA3189E



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O(UNLOADED)≈75 (TOKO No. KACS K586HM OR EQUIVALENT)
**C=0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)
=0.015 μF FOR 75 μs DEEMPHASIS (USA)

92CM-29953

Fig. 6 – Test circuit for CA3189E using a single-tuned detector coil.

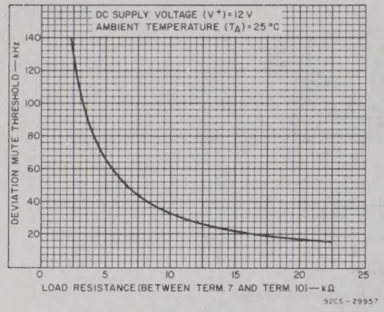


Fig. 7 — Deviation mute threshold as a function of load resistance (between Term. 7 and Term. 10).

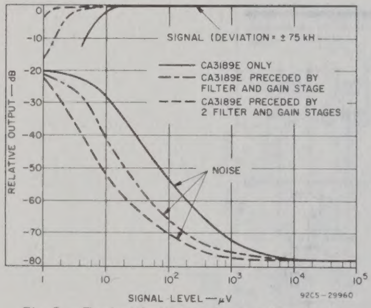


Fig. 8 — Typical limiting and noise characteristics.

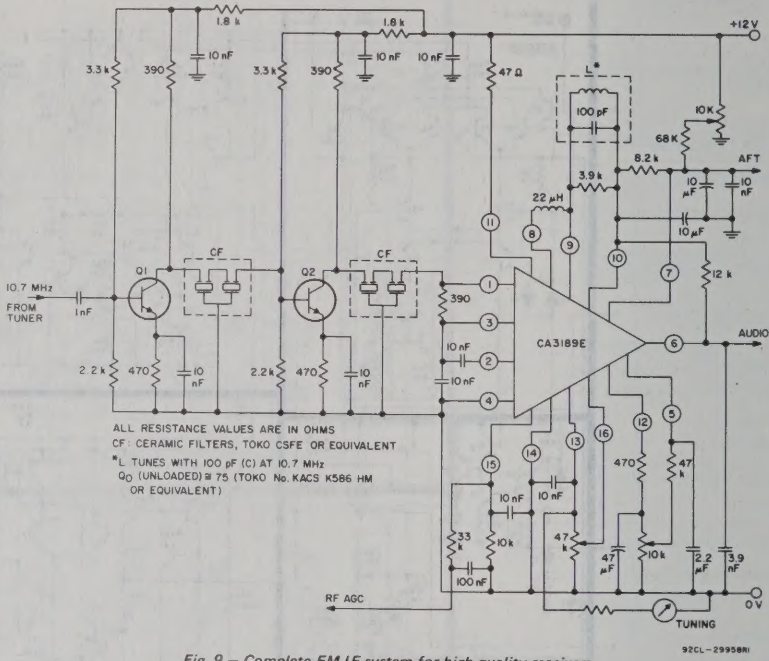
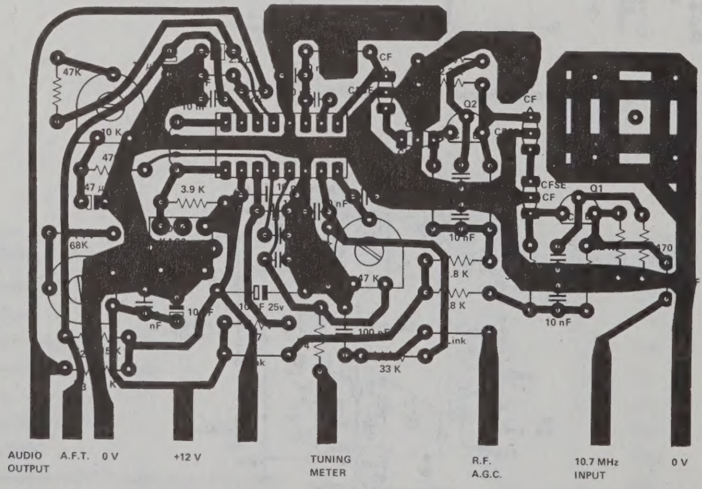


Fig. 9 — Complete FM IF system for high-quality receivers.



COMPLETE FM IF SYSTEM FOR HIGH-QUALITY TUNERS

The circuit, Fig. 9, provides a complete FM IF system for a high-quality receiver. Either one or two stages of amplification and bandpass filtering may be desired, depending on the receiver requirements. Figure 8 shows typical limiting and noise characteristics for each circuit configuration which can be compared to the CA3189E alone.

Fig. 10 — Printed circuit-board and component layout for circuit shown in Fig. 9.

TV Chroma Amplifier/ Demodulator

Provides Complete System for Processing Chroma
When Used with RCA-CA3070 or CA3170
"G" Suffix Type-Hermetic Gold-CHIP in
Dual-In-Line Plastic Package

Features:

- **Excellent linearity in dc chroma gain-controlled circuit**
- **Improved filtering resulting in reduced 7.2-MHz output from the color demodulators**
- **Current limiting for short-circuit protection**
- **Good tolerance to B+ supply variations**
- **Good temperature coefficient stability**
- **Gold-CHIP for increased reliability**

The RCA-CA3221G is a monolithic silicon integrated circuit chroma amplifier/demodulator with ACC, saturation control, and killer control for use in NTSC color TV receivers. It is designed to function compatibly with the CA3070 or CA3170 in a 2-package chroma system. The CA3221G is functionally identical to the industry standard CA3121, but has a modified saturation control as well as a modified color difference matrix.

The CA3221G is supplied in the 16-lead dual-in-line plastic package with a hermetic Gold-CHIP (G suffix). The transistor chips used in the hermetic Gold-CHIP plastic packages are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

MAXIMUM RATINGS at $T_A = 25°C$

Supply Voltage	30 V
Device Dissipation:	
Up to $T_A = 55°C$	1 W
Above $T_A = 55°C$	derate linearly 10.5 mW/°C
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (During Soldering)	
At distance 1/16" ±1/32" (1.59 ±0.79 mm) from case for 10 s max.	+265°C

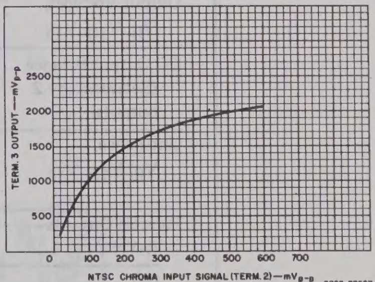


Fig. 2 – Typical ACC plot for the CA3221G when used with the CA3070.

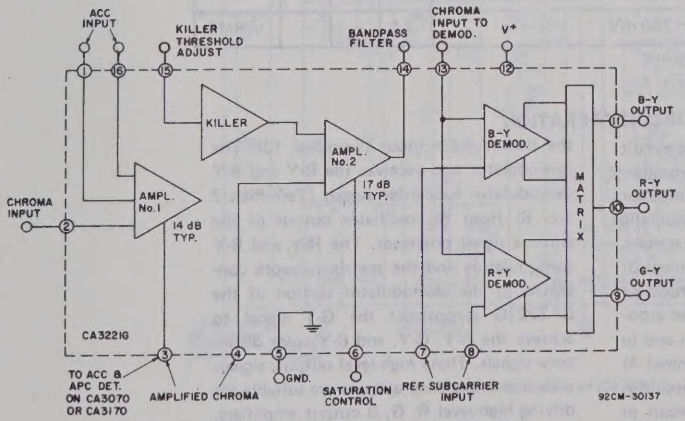


Fig. 1 – Functional block diagram of the CA3221G.

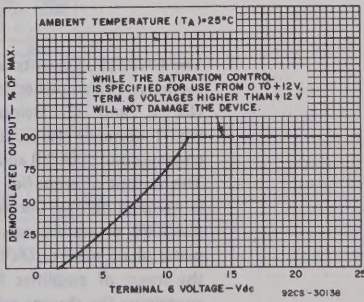


Fig. 3 – Saturation control characteristic.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and Referenced to Test Circuit (Fig.7)

CHARACTERISTIC, TERMINAL MEASURED, AND SYMBOL	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current, I_T	–	–	40	50	mA
Input Sensitivity, V_2	Vary Eg; set V_{11} for 2 V RMS S3 = 1	4	12	20	mV RMS
Second-Stage Sensitivity, V_4	Vary Eg; set V_{11} for 2 V RMS S3 = 1	30	53	75	mV RMS
Output Voltage (Killer off)	Switch Positions: S1=2, S2=2, S3=1 Adjust killer potentiometer until output drops	–	–	70	mV RMS
Saturation Control Characteristics: * V_{11} 50% Gain	Vary Eg; set V_{11} for 2 V RMS with S3 = 1. Set S3 = 2 measure V_{11}	0.71	0.95	1.16	V RMS
0% Gain	Same as above, S3 = 3	–	–	20	mV RMS
Demodulator Characteristics: Output Voltages, V_9, V_{10}, V_{11}	–	13.5	14.5	15.5	V
DC Output Balance (Between any 2 outputs)	–	–0.6	–	+0.6	V
Unbalance, V_9, V_{10}, V_{11}	Eg=0; Switch Position: S1=1, S2=1, S3= 1	–	–	0.8	Vp-p
Relative Outputs— R-Y, V_{10}	Vary Eg; set V_{11} for 2 V RMS, S3 = 1	1.75	1.85	1.95	V RMS
G-Y, V_9		0.6	0.7	0.8	V RMS
Relative Phase — R-Y, V_{10}	Vary Eg; set V_{11} for 2 V RMS; read phase of V_{10} and V_9	–	90	–	degrees
G-Y, V_9	with V_{11} as reference	–	244	–	degrees
Max. Output Voltage, V_{11}	Eg = 750 mV	2.8	–	–	V RMS

*See Fig. 3 for saturation control characteristic.

CIRCUIT OPERATION

The CA3221G consists of three basic circuit sections: (1) amplifier No. 1, (2) amplifier No. 2, and (3) demodulator. Amplifier No. 1 contains the circuitry for automatic chroma control (ACC) and color-killer sensing. The output of amplifier No. 1 (Terminal 3) is coupled to the Chroma Signal Processor (CA3070 or equivalent) for ACC and automatic phase control (APC) operation and to the input of amplifier No. 2 (Terminal 4) containing the chroma gain control circuitry. The signal from the color-killer circuit in amplifier No. 1 acts upon amplifier No. 2 to greatly reduce its gain under weak signal conditions.

The output from amplifier No. 2 (Terminal 14) is applied, through a Bandpass Filter, to the demodulator input (Terminal 13). The demodulator also receives the R-Y and B-Y demodulator subcarrier signals (Terminals 7 and 8) from the oscillator output of the chroma signal processor. The R-Y and B-Y demodulators and the matrix network contained in the demodulator section of the CA3221G reconstruct the G-Y signal to achieve the R-Y, G-Y, and B-Y color difference signals. These high-level outputs signals with low impedance outputs are suitable for driving high-level R, G, B output amplifiers. Internal capacitors are included on each output to filter out unwanted harmonics. For additional operating information and signal waveforms, refer to Television Chroma System (utilizing RCA-CA3070, CA3071, CA3072), File No. 468.

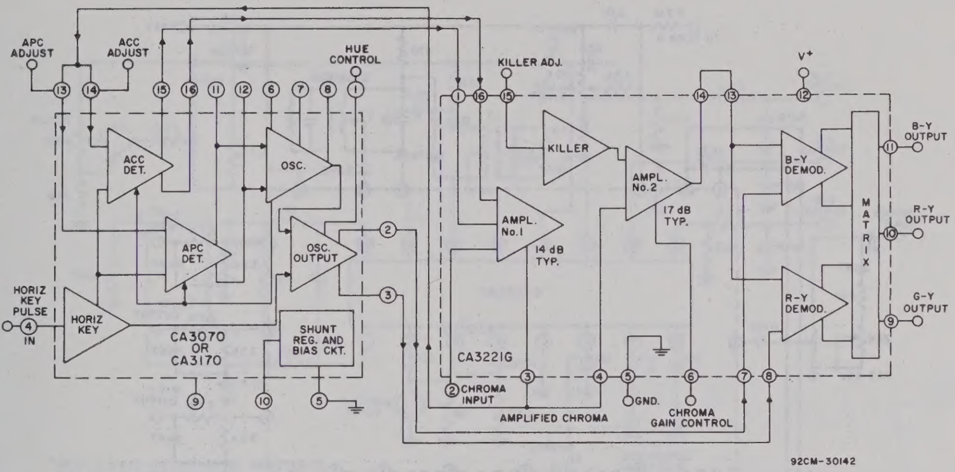


Fig. 4 – Simplified functional diagram of a two-package TV chroma system utilizing the CA3221G and CA3070 or CA3170.

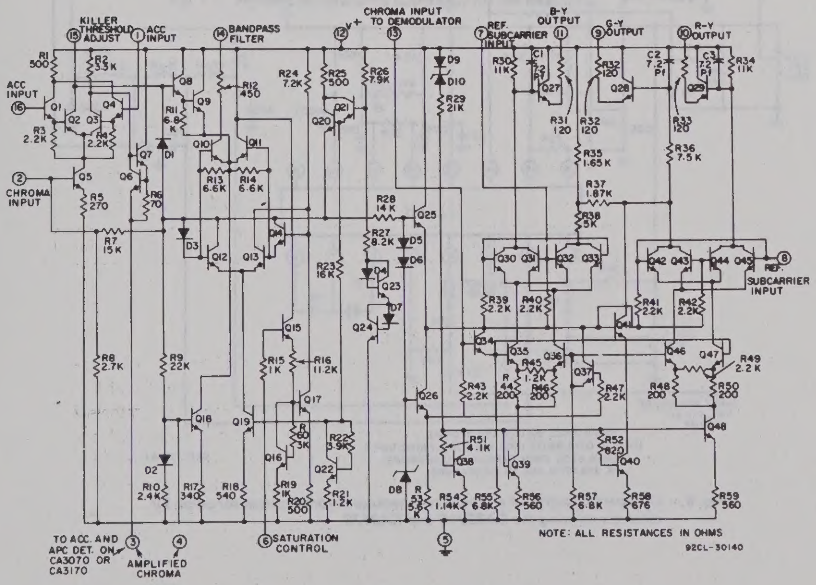
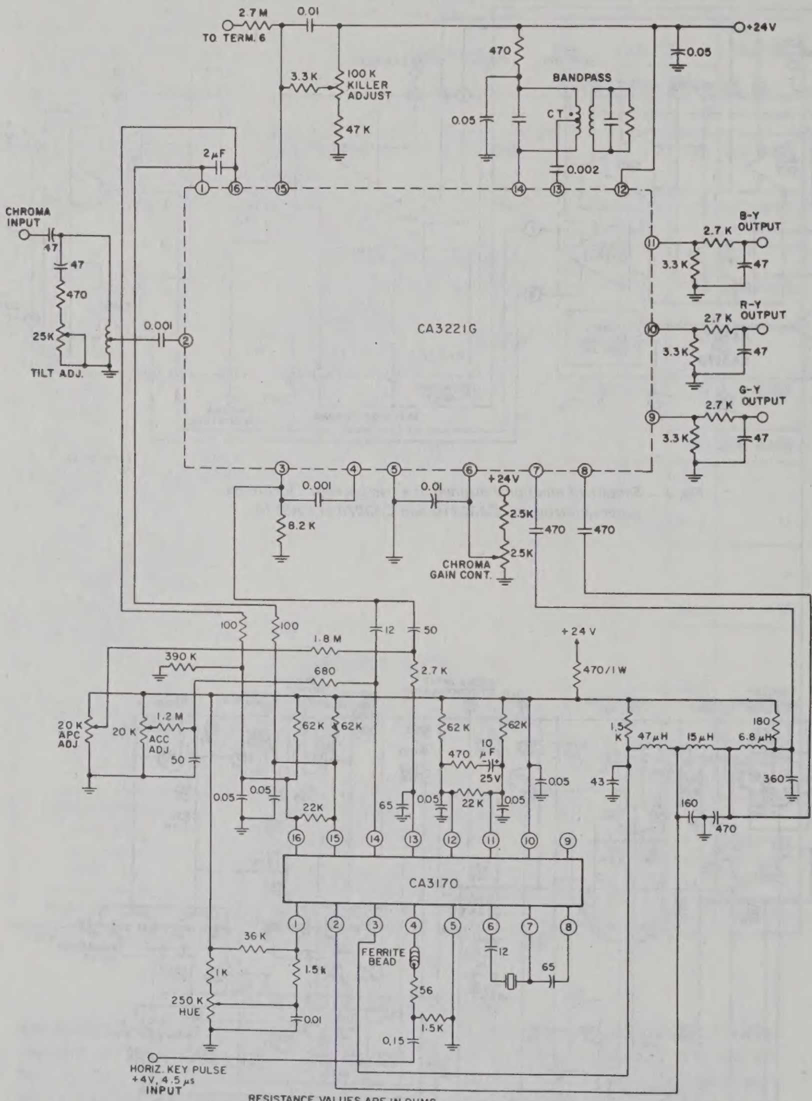


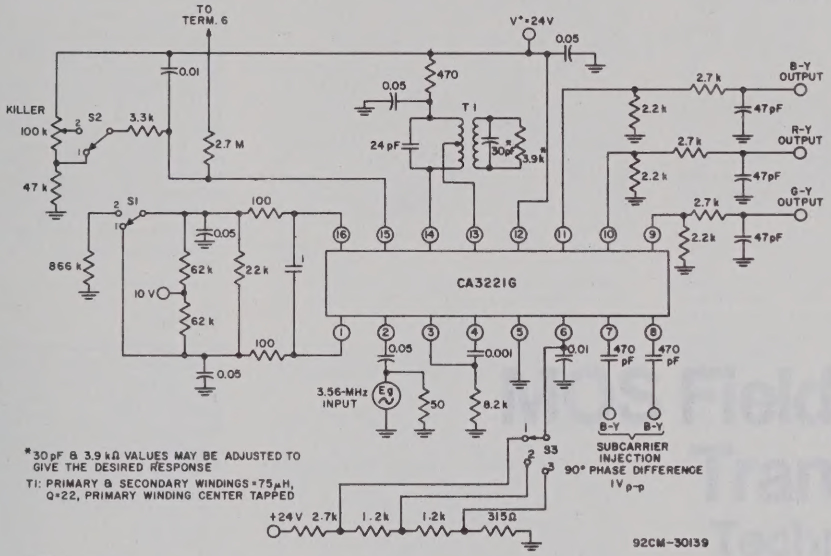
Fig. 5 – Schematic diagram of CA3221G.



RESISTANCE VALUES ARE IN OHMS.
UNLESS OTHERWISE INDICATED, ALL CAPACITANCE
VALUES LESS THAN 1 ARE IN MICROFARADS,
1 OR GREATER ARE IN PICOFARADS.

92CL-30141

Fig. 6 – Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3221G and CA3170.



*30 pF & 3.9 kΩ VALUES MAY BE ADJUSTED TO GIVE THE DESIRED RESPONSE

T1: PRIMARY & SECONDARY WINDINGS = 75 μH, Q=22, PRIMARY WINDING CENTER TAPPED

NOTE:
2.2-kΩ LOADS ONLY FOR TEST PURPOSE, 3.3-kΩ LOADS RECOMMENDED FOR APPLICATIONS.
RESISTANCE VALUES ARE IN OHMS.
CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE INDICATED.

Fig. 7 — Typical characteristics test circuit for the CA3221G.

MOS Field-Effect Transistors

Technical Data

3N128, 3N143

Silicon MOS Transistors N-Channel Depletion Types

For Amplifier, Mixer, & Oscillator Applications in Military &
Industrial VHF Communications Equipment Operating up to 250 MHz

RCA-3N128 and 3N143 are N-channel depletion-type silicon insulated-gate field-effect transistors utilizing the MOS* construction. The 3N128 is intended primarily for VHF amplifier service in military and industrial applications. It also is extremely well suited for use in dc and low-frequency amplifier applications requiring a transistor having high power gain, very high input impedance, and low gate leakage.

The 3N143 is designed for use as a VHF mixer and oscillator. Because of their improved transfer characteristic and increased dynamic range the 3N128 and 3N143 provide substantially better cross-modulation performance in linear amplifier applications than conventional (bipolar) transistors and are free from diode-current loading common to junction type FET's. These transistors are hermetically sealed in JEDEC TO-72 metal packages.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25° C:*

*DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
*DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:		
Continuous dc	+1, -8	V
Peak ac	±15	V
*DRAIN CURRENT, I_D	50	mA
*TRANSISTOR DISSIPATION, P_T:		
At Ambient up to 25°C	330	mW
Temperatures above 25°	Derate 2.2	mW/°C
*AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
*LEAD TEMPERATURE (During soldering): At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265	°C

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*In accordance with Jedec Registration Data Format JS9-RDF11B.

Performance Features

- Large dynamic range
- Greatly reduces spurious responses in rceiver front ends
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability
- Superior crossmodulation capability

Device Features

- Low noise figure (3N128) – 3.5 dB typ. at 200 MHz
- High VHF amplifier gain (3N128) – 16 dB typ. at 200 MHz
- Low input capacitance – 5.5 pF typ.
- High transconductance – 7500 μmho typ.
- High input resistance – 10^{14} Ω typ.
- High conversion gain (3N143, mixer) – 13.5 dB typ. at 200 MHz

Applications

- VHF amplifiers, mixers, converters and if-amplifiers in communication receivers.
- High-impedance timing circuits
- Detectors, oscillators, frequency multipliers, phase splitters, pulse stretchers and current limiters
- Electrometer amplifiers
- Voltage-controlled attenuators
- High impedance differential amplifiers

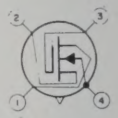
ELECTRICAL CHARACTERISTICS: *(At T_A = 25° C)*

Measured with Substrate Connected to Source Unless Otherwise Specified.

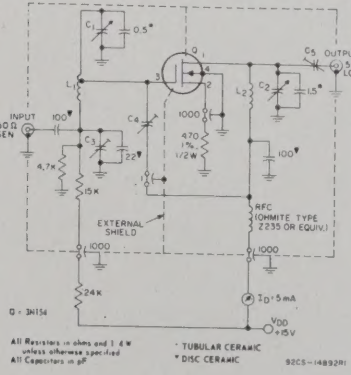
	CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS 3N128 MIN.	3N128 TYP.	3N128 MAX.	3N143 MIN.	3N143 TYP.	3N143 MAX.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = –8 V T_A = 25°C	–	0.1	50	–	0.1	1000	pA
			V_{DS} = 0, V_{GS} = –8 V T_A = 125°C	–	–	5	–	–	200	nA
*	Zero-Bias Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	25	5	15	30	mA
*	Drain-to-Source Cutoff Current	$I_D(off)$	V_{DS} = 20 V, V_{GS} = –8 V	–	–	50	–	–	50	μA
*	Gate-to-Source Cutoff Voltage	$V_{GS}(off)$	V_{DS} = 15 V, I_D = 50 μA	–0.5	–3	–8	–0.5	–3	–8	V
*	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5,000	7,500	12,000	5,000	7,500	12,000	μmho
*	Drain-to-Source Channel Resistance	$r_{DS}(on)$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	–	200	–	–	200	–	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance▲	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.15	0.25	0.35	0.12	0.25	0.38	pF
*	Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	–	5.5	7	–	5.5	7	pF
			Common-Source Configuration							
*	Input Admittance	Y_{is}	f = 200 MHz	–	0.4 + J7.3	–	–	–	–	mmho
*	Forward Transfer Admittance	Y_{ss}	V_{os} = 15 Volts	–	7 – J2	–	–	–	–	mmho
*	Output Admittance	Y_{os}	I_D = 5 mA	–	0.28 + J1.8	–	–	–	–	mmho
*	Maximum Available Power Gain	MAG	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz		21	–	–	–	–	dB
*	Insertion Power Gain (Fixed Neutralization) See Fig. 1	G_{PS}		13.5	16	–	–	–	–	dB
	Power Gain (Conversion (See Fig. 3)	$G_{PS}(c)$	V_{DS} = 15 V, I_D = 1 mA, f_{in} = 200 MHz f_{out} = 30 MHz	–	–	–	10	13.5	–	dB
	Noise Figure (See Fig. 1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	–	3.5	5	–	–	–	–

*In accordance with **JEDEC** Registration Data Format JS9-RDF-11B.
▲Three-Terminal Measurement: Source Returned to Guard Terminal.

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case



C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig. 1 - Test circuit used to measure 200-MHz maximum usable power gain and noise figure for 3N128

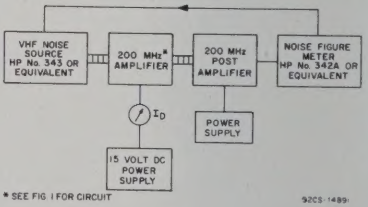
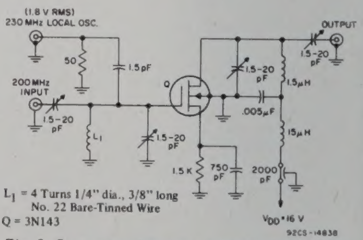


Fig. 2 - Noise figure measurement setup for 3N128



L_1 = 4 Turns 1/4" dia., 3/8" long No. 22 Bare-Tinned Wire
Q = 3N143

Fig. 3 - Conversion power gain test circuit for 3N143

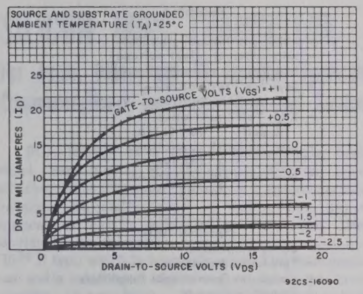


Fig. 4 - Drain current vs. drain-to-source voltage

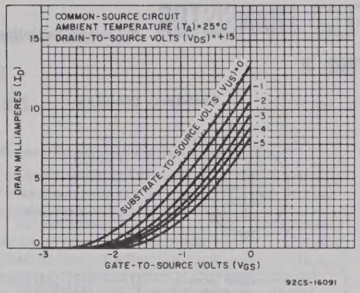


Fig. 5 - Drain current vs. gate-to-source voltage (V_{GS})

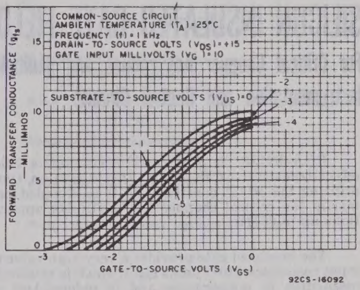


Fig. 6 - Forward transconductance vs. gate bias voltage

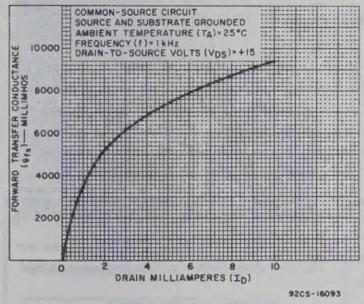


Fig. 7 - Forward transconductance vs. drain current

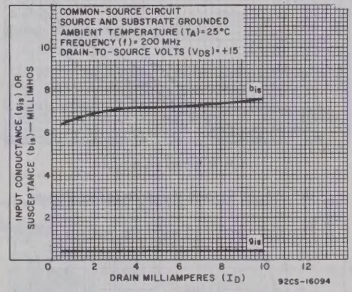


Fig. 8 - Input admittance vs. drain current

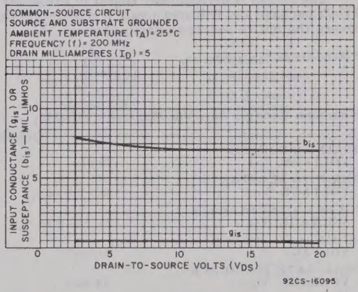


Fig. 9 - Input admittance vs. drain-to-source voltage

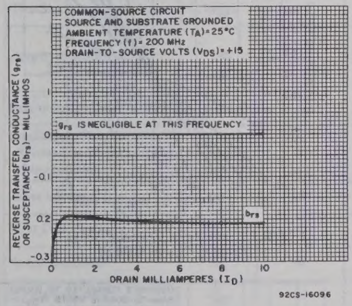


Fig. 10 - Reverse transadmittance vs. drain current

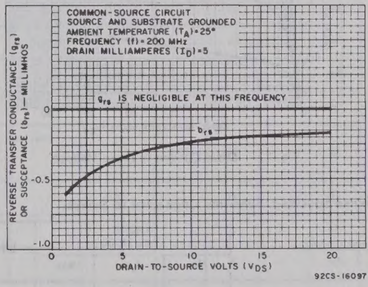


Fig. 11 - Reverse transadmittance vs. drain-to-source voltage

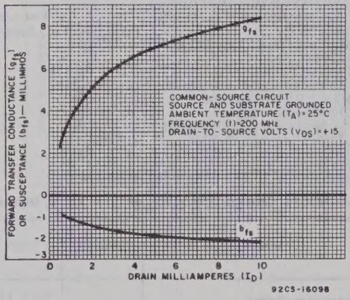


Fig. 12 - Forward transadmittance vs. drain current

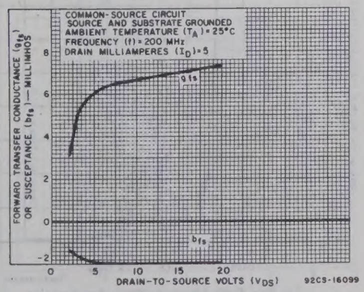


Fig. 13 - Forward transadmittance vs. drain-to-source voltage

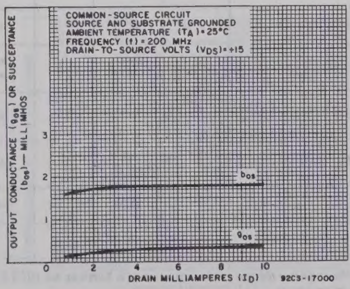


Fig. 14 - Output admittance vs. drain current

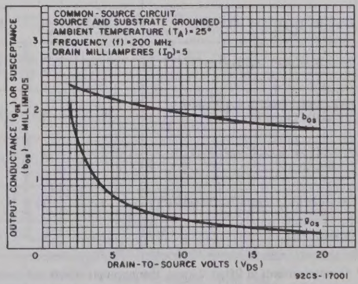


Fig. 15 - Output admittance vs. drain-to-source voltage

SILICON INSULATED-GATE FIELD-EFFECT TRANSISTOR

N-Channel Depletion Type

For Critical Chopper Applications and Multiplex Service in Instrumentation and Control Circuits

RCA-3N138 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60MHz.

The insulated gate provides a very high value of input resistance (10^{14} ohms typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N138 also features extremely low feedthrough capacitance (0.18pF typ.) and zero inherent offset voltage.

The 3N138 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

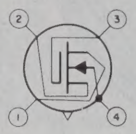
* Metal-Oxide-Semiconductor.

Maximum Ratings, Absolute-Maximum Values:

(Substrate connected to source unless otherwise specified)

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	±35 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, −0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, −0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	±10 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max.	V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS: V_{GS}, V_{GD}, V_{GB}, non-repetitive	±45 max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10)	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330 max.	mW
above 25°C	Derate linearly at 2.2 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +150	°C
Operating	−65 to +125	°C
LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32" to seating surface for 10 seconds max.	265 max.	°C

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

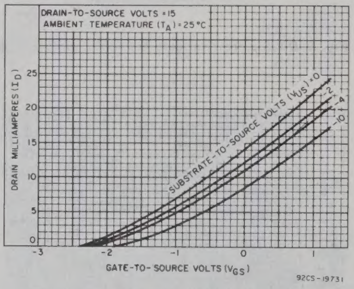


Fig. 1 — Drain Current vs Gate-to-Source Voltage

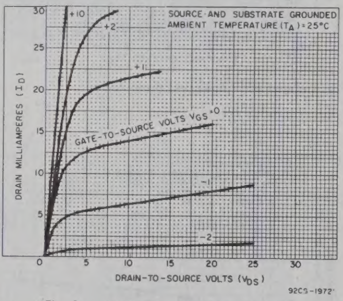


Fig. 2 — Drain Current vs Drain Voltage

Features

- excellent thermal stability
- zero inherent offset voltage
- low leakage current: 10 pA max.
- low "on" resistance —
  r_{DS}(on) = 240Ω typ. (V_{GS} = 0V)
- high "off" resistance —
  R_{DS}(off) = 10^{10}Ω typ.
- low feedback capacitance —
  C_{rss} = 0.18pF typ.
- low input capacitance —
  C_{iss} = 3pF typ.

Applications

- Servo Amplifiers
- Telemetry Amplifiers
- Computer Operational Amplifiers
- Sampling Circuits
- Electrometer Amplifiers

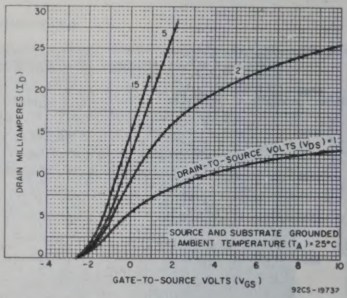


Fig. 3 — Drain Current vs Gate-to-Source Voltage

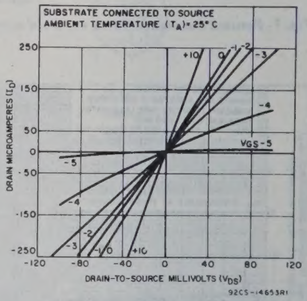


Fig. 4 — Low-Level Drain Current vs Drain-to-Source Voltage

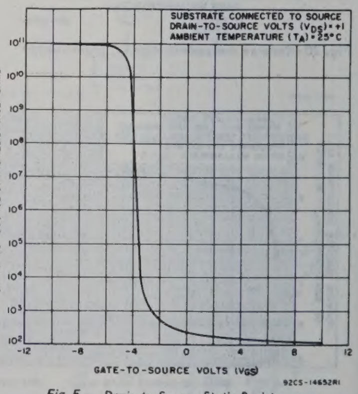


Fig. 5 — Drain-to-Source Static Resistance vs Gate-to-Source Voltage

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N138			UNITS
			Min.	Typ.	Max.	
Gate-Leakage Current	I_{GSS}	V_{GS} = ±10, V_{DS} = 0, T_A = 25°C V_{GS} = ±10, V_{DS} = 0, T_A = 125°C	— —	0.1 20	10 200	pA pA
Drain-to-Source "ON" Resistance	r_{DS}(on)	V_{GS} = 0, V_{DS} = 0, f = 1 KHz, T_A = 25°C V_{GS} = +10, V_{DS} = 0, f = 1 KHz, T_A = 25°C V_{GS} = 0, V_{DS} = 0, f = 1 KHz, T_A = 125°C	— — —	240 135 350	350 — —	Ω Ω Ω
Drain-to-Source "OFF" Resistance	R_{DS}(off)	V_{GS} = −10, V_{DS} = +1	2 × 10^8	10^{10}	—	Ω
Drain-to-Source Cutoff Current	I_D(off)	V_{GS} = −10, V_{DS} = +1, T_A = 25°C V_{GS} = −10, V_{DS} = +1, T_A = 125°C	— —	0.01 0.01	5 0.5	nA μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	V_{GS} = −10, V_{DS} = 0, f = 1 MHz	—	0.25	0.4	pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	V_{GS} = −10, V_{DS} = 0, f = 1 MHz	—	3	5	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	V_{DS} = 12, I_D = 5 mA	—	6000	—	μmho
Offset Voltage	V_O	V_{GS} = ±10, V_{DS} = 0	—	0*	—	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more: There errors may be minimized by the use of solder having a low thermal e.m.f. such as Leeds & Northrup No.107-1.0.1, or equivalent.

3N139

SILICON MOS TRANSISTOR N-Channel Depletion Type

For Audio, Video, and RF Amplifier Applications in Communications, Instrumentation and Control Circuits

RCA 3N139 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is a general purpose transistor especially suited for audio, video, and rf applications, and for wide-band amplifier designs. The insulated gate provides a very high input resistance (10^{14} Ω typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N139 also has a high transconductance, a low value of input capacitance (3 pF typ.), and a very low feedback capacitance (0.19 pF typ.).

The 3N139 is hermetically sealed in the standard 4-lead JEDEC TO-72 package.

Maximum Ratings, *Absolute-Maximum Values:*

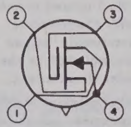
DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . .	+35 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, -0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, -0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS} .	±10 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max.	V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS; V_{GS}, V_{GD}, V_{GB}, non-repetitive	±42 max.	V
DRAIN CURRENT, I_D	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
above 25°C	Derate linearly at 2.2	mW/°C
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distance not closer than 1/32 inch to seating surface for 10 seconds max. . .	265 max.	°C

* Metal-Oxide-Semiconductor

FEATURES

- **high input resistance $R_{GS} = 10^{14}$ Ω typ.**
- **low input capacitance $C_{iss} = 3$ pF typ.**
- **low feed back capacitance $C_{rss} = 0.2$ pF typ.**
- **low gate leakage current $I_{GSS} = 0.1$ nA typ.**
- **high drain-to-source voltage: +35 max. V**

TERMINAL ARRANGEMENT



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

ELECTRICAL CHARACTERISTICS, at T_A = 25° C Unless Otherwise Specified. Bulk (Substrate) Connected to Source

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS			UNITS
		FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC GATE-TO-SOURCE VOLTAGE V_{GS}	DC DRAIN CURRENT I_D				
		MHz	V	V	mA	Min.	Typ.	Max.	
Drain-to-Source Cutoff Current	I_D(OFF)		15	−8		—	—	50	μA
Zero-Bias Drain Current*	I_{DSS}		15	0		5	15	25	mA
Gate Reverse Current	I_{GSS}	T_A = 25°C	0	±10		—	—	1	nA
		T_A = 100°C	0	±10		—	—	100	nA
Gate-to-Source Cutoff Voltage	V_{GS}(OFF)		15		0.05	−2	−4	−6	V
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15		5	0.05	0.2	0.4	pF
Input Resistance	r_{is}	100	15		5		12	—	kΩ
Input Capacitance	C_{iss}	100	15		5	—	3	10	pF
Output Resistance	r_{os}	100	15		5		6	—	kΩ
Output Capacitance	C_{css}	100	15		5	—	1.4	—	pF
Forward Transconductance	g_{fs}	1 kHz	15		5		5	—	mmho

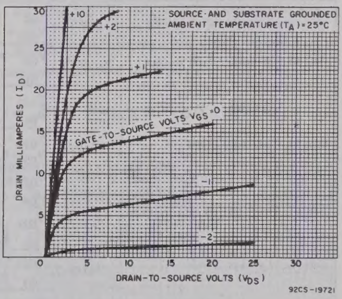


Fig. 1 – Drain Current vs Drain Voltage

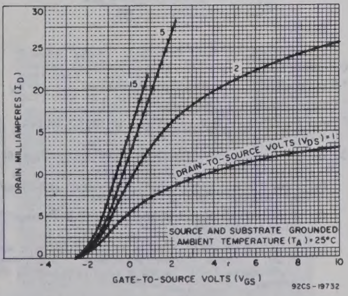


Fig. 2 – Drain Current vs Gate-to-Source Voltage

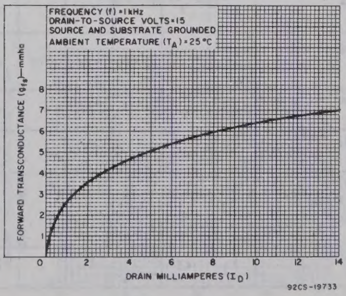


Fig. 3 – 1 KHz forward transconductance vs drain current

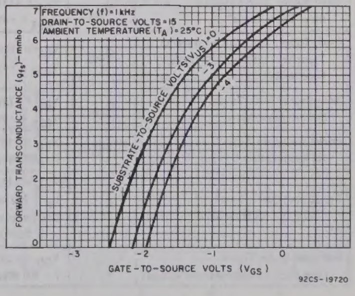


Fig. 4 – 1 KHz forward transconductance vs gate-to-source voltage

3N140, 3N141

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS N-Channel Depletion Types

For Amplifier and Mixer Applications Up to 300 MHz

RCA-3N140 and 3N141* are n-channel silicon, depletion type, dual insulated-gate, field-effect transistors utilizing the MOS** construction. They have exceptional characteristics for rf-amplifier and mixer applications at frequencies up to 300 MHz. These transistors feature a series arrangement of two separate channels, each channel having an independent control gate.

The 3N140, used in a common-source configuration in which gate No.2 is ac grounded, reduces oscillator-feedthrough to the antenna thereby minimizing oscillator radiation. The 3N141 provides excellent isolation between the oscillator and rf signals because each of the two signal frequencies being mixed has its own control element.

The mixing function performed by the 3N141 is unique in that the signal applied to gate No.2 is used to modulate the input-gate (gate No.1) transfer characteristic. This technique is superior to conventional "square law" mixing, which can only be accomplished in the non-linear region of the device transfer characteristic.

The use of the 3N141 as described provides high useful conversion gains at all vhf frequencies, and the reduction in spurious responses is substantial and easily obtainable in simple circuits.

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} . .	0 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-8 to +1	V
Peak ac	-8 to +20	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-8 to 40% of V_{DS}	V
Peak ac	-8 to +20	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
DRAIN CURRENT, I_D		
(Pulsed): Pulse duration ≤ 20 ms, duty factor ≤ 0.15	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	400	mW
At ambient temperatures above 25°C	derate linearly at 2.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds max. .	265	°C

The 3N140 and 3N141 are hermetically sealed in metal JEDEC TO-72 packages.

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* Formerly Dev. Nos. TA2644 and TA7274, respectively.

** Metal-Oxide-Semiconductor.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C Unless Otherwise Specified. Common-Source Circuit.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS
			TYPE 3N140 RF AMPLIFIER			TYPE 3N141 MIXER			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Gate No.1-to-Source Cutoff Voltage	$V_{G1S}(off)$	V_{DS} = +16V, I_D = 200 μA V_{G2S} = +4V	-	-2	-4	-	-2	-4	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S}(off)$	V_{DS} = +16V, I_D = 200 μA V_{G1S} = 0	-	-2	-4	-	-2	-4	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G1S} = +1V, V_{G2S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G1S} = -20V, V_{G2S} = 0 V_{DS} = 0, T_A = 125°C	-	-	0.2	-	–	0.2	μA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	–	-	1	nA
		V_{G2S} = +1V V_{DS} = 0, V_{G1S} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G2S} = -20V, V_{G1S} = 0 V_{DS} = 0, T_A = 125°C	-	-	0.2	-	-	0.2	μA
Zero-Bias Drain Current	I_{DSS}*	V_{DD} = +14V, V_{G1S} = 0, V_{G2S} = +4	5	18	30	5	18	30	mA
Forward Transconductance (Gate No.1 to Drain)	g_{fs}	V_{DD} = +14V, I_D = 10 mA V_{G2S} = +4V, f = 1 kHz	6000	10000	18000	6000	10000	18000	μmho
Cutoff Forward Transconductance (Gate No.1 to Drain)	$g_{fs}(off)$	V_{DD} = +14V, V_{G1S} = -0.5V V_{G2S} = -2V, f = 1 kHz	-	-	100	-	-	-	μmho
Small-Signal, Short-Circuit Input Capacitance♦	C_{iss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	3	5.5	7	3	5.5	7	pF
Small-Signal, Short-Circuit Reverse Transfer Capacitance (Drain to Gate No.1)▲	C_{rss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	0.01	0.02	0.03	0.01	0.02	0.03	pF
Small-Signal Short-Circuit Output Capacitance	C_{oss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	-	2.2	-	-	2.2	-	pF
Power Gain (See Fig.1 for Measurement Circuit)	G_{ps}	V_{DD} = +15V, R_S = 270Ω f = 200 MHz, R_G = 50Ω	16	18	-	-	-	-	dB
Conversion Power Gain (See Fig.2 for Measurement Circuit)	G_{psc}	V_{DD} = +15V, R_S = 120Ω, f_{IN} = 200 MHz, f_{OUT} = 30 MHz Oscillator injection voltage● = 2.5 V (rms)	-	-	-	13	17	-	dB
Measured Noise Figure (See Fig.1 for Measurement Circuit)	NF	V_{DD} = +15V, R_S = 270Ω f = 200 MHz, R_G = 50Ω	-	3.5	4.5	-	-	-	dB

* Pusle test: Pulse duration ≤ 20 ms, duty factor ≤ 0.15.

♦ Capacitance between Gate No.1 and all other terminals.

▲ Three-Terminal Measurement with Gate No.2 and Source Returned to Guard Terminal.

● Measured from gate No.2 to source.

APPLICATIONS

- RF amplifier and mixer in military and industrial communications equipment
- aircraft and marine vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

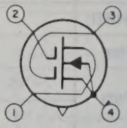
PERFORMANCE FEATURES

- wide dynamic range permits large-signal handling before overload
- dual-gate permits simplified agc circuitry
- virtually no agc power required
- greatly reduces spurious responses in fm receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability
- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's

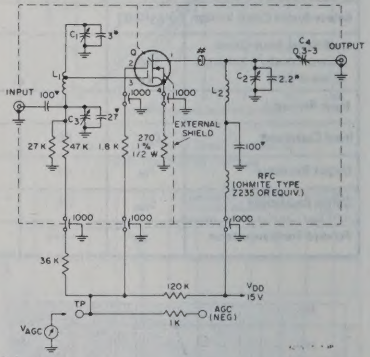
DEVICE FEATURES

- low gate leakage currents - -
  I_{G1SS} & I_{G2SS} = 1 nA max. at T_A = 25°C
- high forward transconductance - -
  g_{fs} = 6000 μmho min.
- high unneutralized RF power gain - -
  G_{ps} = 16 dB min. at 200 MHz
- low VHF noise figure - - 4.5 dB max. at 200 MHz

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE AND CASE



Q = 3N140.

▼ Disc ceramic. All resistors in ohms

* Tubular ceramic. All capacitors in pF

# Ferrite bead (1/2 used); Indiana General No.H1742C-(A-147), F-1157-1-H

C_1, C_2: 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

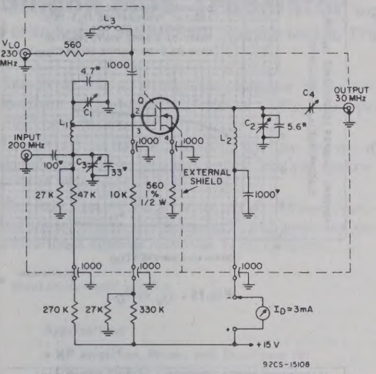
C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200 MHz power gain and noise figure test circuit for type 3N140.



Q = 3N141.

▼Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1, C_2: 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Ohmite Z-144 RF choke or equivalent.

L_3: J.W. Miller Co. #4580 0.1 μH RF choke or equivalent.

Note: If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

Fig.2 - Conversion power gain test circuit for type 3N141.

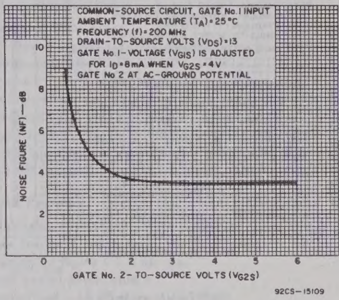


Fig.3 - NF vs V_{G2S}.

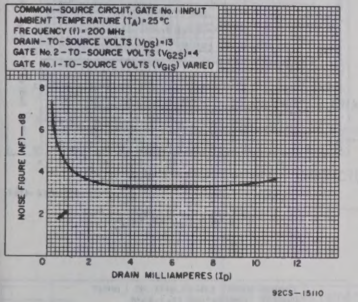


Fig.4 - NF vs I_D.

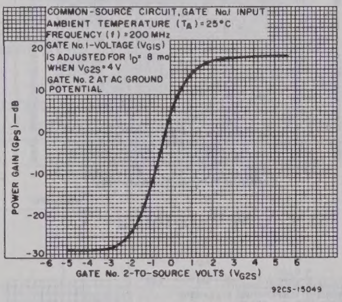


Fig.5 - G_{PS} vs V_{G2S} (For 3N140).

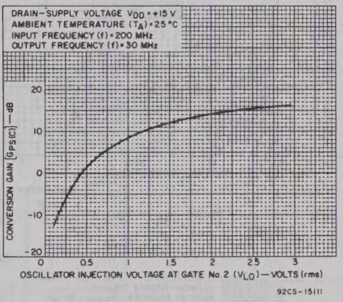


Fig.6 - $G_{PS(C)}$ vs V_{LO} (For 3N141).

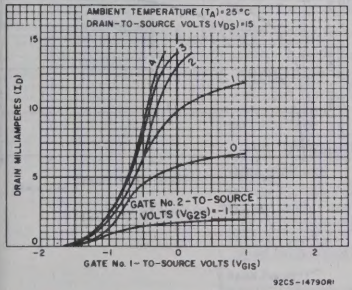


Fig.7 - I_D vs V_{G1S}.

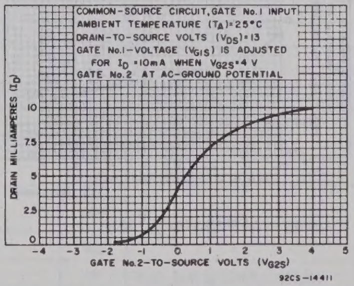


Fig.8 - I_D vs V_{G2S}.

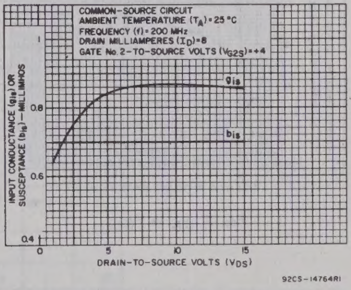


Fig.9 - y_{is} vs V_{DS}.

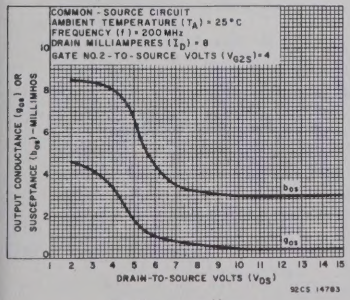


Fig.10 - y_{os} vs V_{DS}.

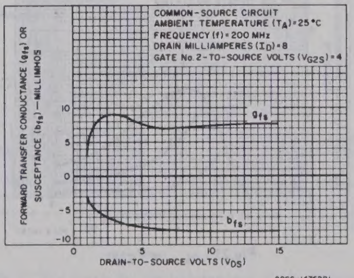


Fig.11 - y_{fs} vs V_{DS}.

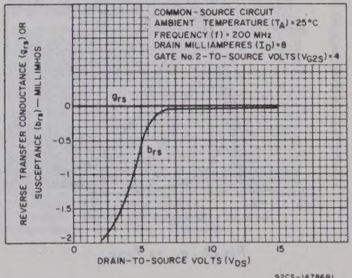
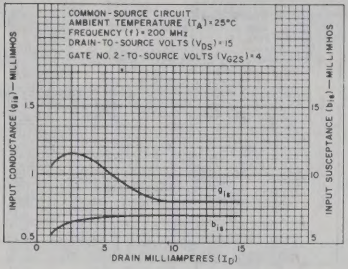
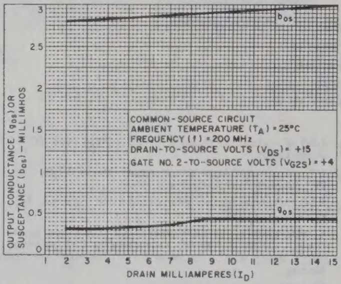


Fig.12 - y_{rs} vs V_{DS}.



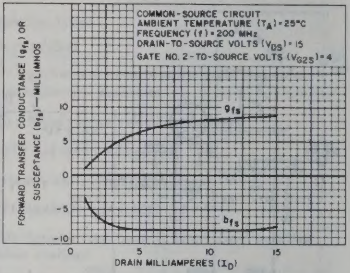
92CS-14771RI

Fig.13 - y_{is} vs I_D.



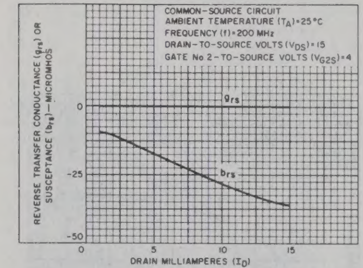
92CS 14776

Fig.14 - y_{os} vs I_D.



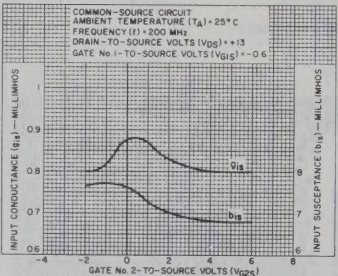
92CS-14763RI

Fig.15 - y_{fs} vs I_D.



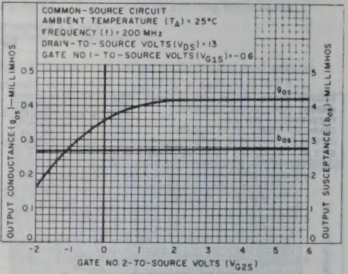
92CS-14773RI

Fig.16 - y_{rs} vs I_D.



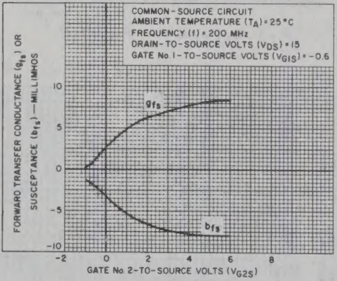
92CS-14765

Fig.17 - y_{is} vs V_{G2S}.



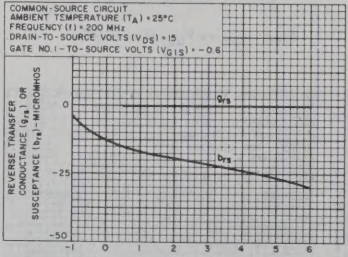
92CS 14767

Fig.18 - y_{os} vs V_{G2S}.



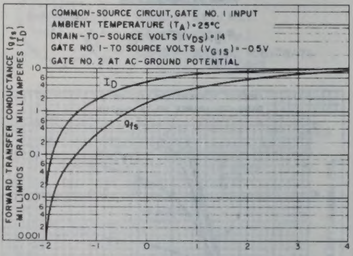
92CS-14775RI

Fig.19 - y_{fs} vs V_{G2S}.



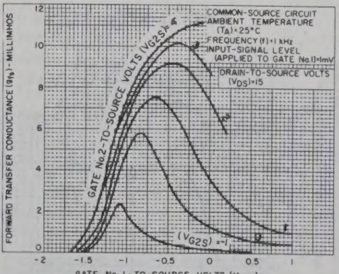
92CS-14759RI

Fig.20 - y_{rs} vs V_{G2S}.



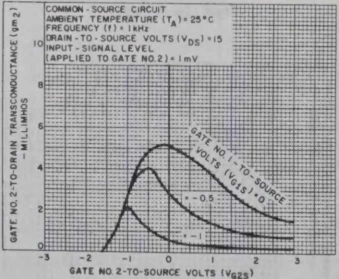
92CS 14749RI

Fig.21 - g_{fs} and I_D vs V_{G2S}.



92CS-14721

Fig.22 - g_{fs} vs V_{G1S}.



92CS 14787

Fig.23 - g_{fs2} vs V_{G2S}.

3N142

Silicon MOS Transistor N-Channel Depletion Type

For Industrial and Military Applications to 175 MHz

The 3N142 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type utilizing the MOS[■] construction.

The 3N142 is intended primarily for use as the rf amplifier in FM receivers and general amplifier applications at frequencies up to 175 MHz.

The wide dynamic range of the 3N142 reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

[■] Metal-Oxide-Semiconductor

Applications

- **RF amplifier, Mixer, and Oscillator in:**
  - **CB and Mobile Communication Receivers**
  - **Aircraft and Marine Receivers**
  - **CATV and MATV Equipment**
- **Industrial Control Circuits**
- **Variable Attenuators**
- **Current Limiters**
- **Instrumentation Equipment**
- **High-Impedance Timing Circuits**

Maximum Ratings, Absolute-Maximum Values at $T_A = 25°C$

*DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-20	V
*DRAIN-TO-GATE VOLTAGE, V_{DG}	-20	V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:		
Continuous	+1 to −8	V
Peak ac	±15	V
*DRAIN CURRENT, I_D	50	mA
*TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	Derate at 2.2mW/°C	
*AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +175	°C
Operating	−65 to +175	°C
*LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32" from seating surface for 10 seconds max.	265	°C

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* In accordance with JEDEC Registration Data Format JS-9 RDF11-B

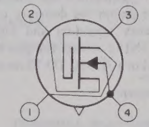
Performance Features

- Large dynamic range
- Enhanced signal-handling capability for low cross-modulation
- Dual-polarity gate permits positive and negative swing without degradation of input impedance
- Reduced spurious responses in FM receivers
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability for critical oscillator designs

Device Features

- High input resistance – 1000 megohms
- Low feedback capacitance – 0.35 pF max.
- Low noise figure – 2.5 dB typ.
- High useful power gain – neutralized – 16 dB min. at 100 MHz
- Hermetically sealed TO – 72 metal package

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

ELECTRICAL CHARACTERISTICS: (At $T_A = 25°C$)

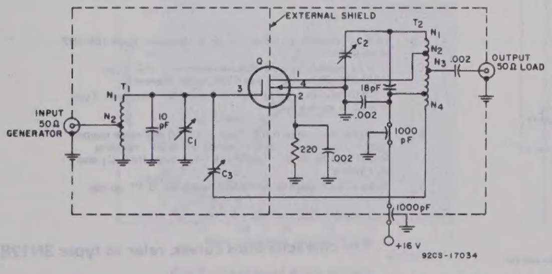
Measured with Substrate Connected to Source Unless Otherwise Specified.

CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
* Gate Leakage Current	I_{GSS}	$V_{DS} = 0$, $V_{GS} = -8$ V, $T_A = 25°C$ $V_{DS} = 0$, $V_{GS} = -8$ V, $T_A = 125°C$ $V_{DS} = 0$, $V_{GS} = +1$, $T_A = 25°C$ $V_{DS} = 0$, $V_{GS} = +1$, $T_A = 125°C$	- - - -	0.0001 - 0.0001 -	1 200 1 200	nA nA nA nA
* Zero-Bias Drain Current**	I_{DSS}	$V_{DS} = 15$ V, $V_{GS} = 0$	5	15	25	mA
* Drain-to-Source Cutoff Current	$I_{D(off)}$	$V_{DS} = 20$ V, $V_{GS} = -8$ V	-	-	50	µA
* Gate-to-Source Cutoff Voltage	$V_{GS}(off)$	$V_{DS} = 15$ V, $I_D = 50$ µA	-0.5	-3	-8	V
* Forward Transconductance	g_{fs}	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 1 kHz	5000	7500	12,000	µmho
* Drain-to-Source Channel Resistance	$r_{DS(on)}$	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 kHz	-	200	-	Ω
* Small-Signal Short-Circuit Reverse Transfer Capacitance‡	C_{rss}	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 0.1 to 1 MHz	0.10	0.22	0.35	pF
* Small-Signal Short-Circuit Input Capacitance	C_{iss}	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 0.1 to 1 MHz	-	5.5	7	pF
* Input Admittance	Y_{is}	Common Source Configuration f = 100 MHz $V_{DS} = 15V$ $I_D = 5$ mA	-	0.155+J3.45	-	mmho
* Forward Transfer Admittance	Y_{fs}		-	7.5−J0.9	-	mmho
* Output Admittance	Y_{os}		-	0.21+J0.9	-	mmho
* Maximum Available Power Gain	MAG	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 100 MHz	-	26	-	dB
Maximum Usable Power Gain (Fixed Neutralization)	MUG		-	17	-	dB
* Insertion Power Gain** (Fixed Neutralization)	G_{ps}		16	-	-	dB
* Noise Figure**	NF	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 100 MHz	-	2.5	4	dB

* In accordance with JEDEC Registration Data Format JS-9 RDF-11B

‡ Three-Terminal Measurement: Source Returned to Guard Terminal

**See Fig. 1



T_1 N_1 = 6 Turns#20 Tinned Copper Wire; ¼" I.D. ½" Long
$Q_o = 205$, $N_1/N_2 = 4.85$

T_2 $N_1 + N_4$ = 6¾ Turns#20 Tinned Copper Wire ¼" I.D. 9/16" Long
$Q_o = 190$ $N_1/N_2 = 1.9$ $N_1/N_3 = 12.3$ $N_1/N_4 = 8$

C_1 = 10 pF Variable Air Capacitor (Hammarlund Mac-10 or Equivalent)
C_2 = 5 pF Variable Air Capacitor (Hammarlund Mac-5 or Equivalent)
C_3 = 0.7-3 pF Piston-Type Variable Air Capacitor (Erie 535C or Equivalent)
Q = 3N142

Fig. 1 - Test Set Up for 100 MHz Insertion Power Gain and Noise Figure

For characteristics curves, refer to types 3N128 and 3N143.

3N152

Silicon MOS Transistor N-Channel Depletion Type

For Low-Noise RF Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

RCA-3N152 is an N-channel depletion-type silicon insulated gate field-effect transistor utilizing the MOS■ construction. It is intended primarily for VHF amplifier applications up to 250 MHz in military and industrial equipment.

Because of its improved transfer characteristic and exceptionally wide dynamic range, the 3N152 with the substrate in the reversed bias mode can provide substantially better cross-modulation performance in linear amplifier applications than conventional bipolar transistors. The insulated gate with its extremely low reverse (leakage) current eliminates the problem of diode-current loading of the input circuit under strong input conditions, which is common to junction-type FET's. These features in addition to low feedback capacitance permit the design of circuits providing superior high-frequency operation and high gain without neutralization. The 3N152 utilizes full-gate construction and is hermetically sealed in a JEDEC TO-72 metal package.

■ Metal-Oxide-Semiconductor.

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^oC$:*

* DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max.	V
* DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
* GATE-TO-SOURCE VOLTAGE, V_{GS}:		
* CONTINUOUS (dc)	+1, -8 max.	V
* PEAK ac	±15 max.	V
* DRAIN CURRENT, I_D	50 max.	mA
TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25^oC	330 max.	mW
At ambient temperatures above 25^oC	derate at 2.2 mW/^oC	
* AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	^oC
Operating	-65 to +175	^oC
* LEAD TEMPERATURE (During Soldering): At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265 max.	^oC

* In accordance with Jedec Registration Data Format JS-9 RDF 11-B.

Features

- Low gate leakage current — $I_{GSS} = 0.1$ pA typ.
- Low feedback capacitance — $C_{rss} = 0.25$ pF typ.
- High forward transconductance — $g_{fs} = 7500$ μmho typ.
- High vhf power gain — $G_{PS} = 16$ dB typ. at 200 MHz
- Low vhf noise figure — NF = 2.5 dB typ. at 200 MHz
- Exceptionally good cross-modulation characteristics

Performance

- Large dynamic range
- Greatly reduced spurious responses
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability
- Superior cross-modulation performance and greater dynamic range than bipolar transistors

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$

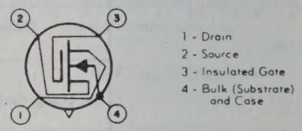
Measured with Substrate Connected to Source Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS 3N152 Min.	LIMITS 3N152 Typ.	LIMITS 3N152 Max.	UNITS
* Gate Leakage Current	I_{GSS}	$V_{DS} = 0$, $V_{GS} = -8V$, $T_A = 25^oC$		0.0001	1	nA
		$V_{DS} = 0$, $V_{GS} = -8$ V, $T_A = 125^oC$			200	nA
* Zero-Bias Drain Current	I_{DSS}	$V_{DS} = 15$ V, $V_{GS} = 0$	5	15	30	mA
Drain-to-Source Cutoff Current	$I_D(off)$	$V_{DS} = 20$ V, $V_{GS} = -8V$			50	μA
* Gate-to-Source-Cutoff Voltage	$V_{GS}(off)$	$V_{DS} = 15$ V, $I_D = 50$ μA	-0.5	-3	-8	V
* Forward Transconductance	g_{fs}	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 1 kHz	5000	7500	12,000	μmho
Drain-to-Source Channel Resistance	$r_{DS}(on)$	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 kHz		200		Ω
* Small-Signal Short-Circuit Reverse Transfer Capacitance▲	C_{rss}	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 0.1 to 1 MHz	0.15	0.25	0.35	pF
Small-Signal Short-Circuit Input Capacitance	C_{iss}	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 0.1 to 1 MHz		5.5	7	pF
Input Admittance	Y_{is}	Common Source Configuration f = 200 MHz $V_{DS} = 15$ V, $I_D = 5$ mA		0.4 + J7.3		mmho
Forward Transfer Admittance	Y_{fs}			7-J2		mmho
Output Admittance	Y_{os}			0.28 + J1.8		mmho
Power Gain Maximum Available Gain	MAG	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 200 MHz		21		dB
Insertion Power Gain (Fixed Neutralization) See Fig.1	G_{PS}		14.5	16		dB
Noise Figure (See Figs. 1 & 2)	NF	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 200 MHz		2.5	3.5	dB

▲ Three-Terminal Measurement. Source Returned to Guard Terminal.

* In accordance with JEDEC Registration Data Format JS-9 RDF-11B.

TERMINAL ARRANGEMENT



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

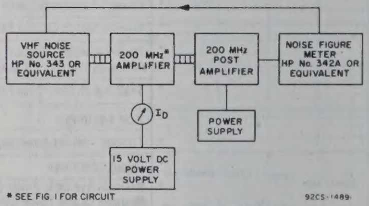
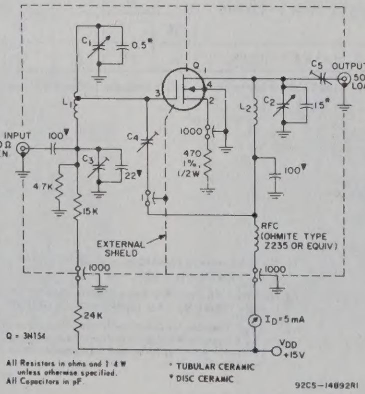


Fig. 2 - Noise figure measurement setup.



C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap

For characteristics curves, refer to types 3N128 and 3N143.

Fig. 1 - Test circuit used to measure 200-MHz maximum usable power gain and noise Figure.

SILICON INSULATED GATE FIELD-EFFECT TRANSISTOR

N-Channel Depletion Type

RCA 3N153 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60 MHz.

The insulated gate provides a very high value of input resistance (10^{10} ohms typ) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N153 also features extremely low feedback capacitance (0.34 pF typ) and virtually zero inherent offset voltage.

This transistor features a Terminal Arrangement in which the gate and source connections are interchanged to provide maximum isolation between the output (drain) and the input (gate) terminals. Although this new basing configuration does not appreciably change the measured device feedback capacitance, it permits the use of external inter-terminal shields to reduce the feedback due to external capacitances, particularly on printed circuit boards. This feature makes it possible to minimize feedthrough capacitance.

The 3N153 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

* Metal-Oxide-Semiconductor

Maximum Ratings, Absolute-Maximum Values:

(Substrate connected to source unless otherwise specified)

DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . .	+20	max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+20, -0.3	max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+20, -0.3	max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS} .	+6, -8	max.	V
PEAK GATE-TO-SOURCE VOLTAGE, v_{GS}	±14	max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor $\leq$ 0.10)	50	max.	mA
TRANSISTOR DISSIPATION, P_T:			
At ambient temperatures from -65 to +25°C	400	max.	mW
above 25°C	derate linearly at 2.67 mW/°C		
AMBIENT TEMPERATURE RANGE:			
Storage	-65 to +175		°C
Operating	-65 to +175		°C
LEAD TEMPERATURE (During soldering):			
At distance $\geq$ 1/32" to seating surface for 10 seconds max.	265	max.	°C

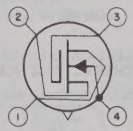
FEATURES

- excellent thermal stability
- virtually zero inherent offset voltage
- low leakage current: 50 pA max.
- low "on" resistance — $r_{DS(on)}$ = 200 Ω typ.
- high "off" resistance — $R_{DS(off)}$ = 10^{10} Ω typ.
- low feedback capacitance — C_{rss} = 0.34 pF typ.
- low input capacitance — C_{iss} = 6 pF typ.

APPLICATIONS

- Choppers
- Multiplexers
- Servo Amplifiers
- Computer Operational Amplifiers
- Sampling Circuits
- Electrometer Amplifiers

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N153			UNITS
			Min.	Typ.	Max.	
Gate-Leakage Current	I_{GSS}	V_{GS}=+6,-8V; V_{DS}=0V; T_A= 25°C V_{GS}=+6,-8V; V_{DS}=0V; T_A=125°C	- -	0.1 -	50 1	pA nA
Static Drain-to-Source "ON" Resistance	$r_{DS}(on)$	V_{GS} = 0V, V_{DS} = 0V	-	200	300	Ω
Drain-to-Source "OFF" Resistance	$R_{DS}(off)$	V_{GS} = -8V, V_{DS} = +1V	10^9	10^{10}	-	Ω
Drain-to-Source Cutoff Current	$I_D(off)$	V_{GS}=-8V, V_{DS}=+1V, T_A= 25°C V_{GS}=-8V, V_{DS}=+1V, T_A=125°C	- -	0.1 0.1	1 1	nA µA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	V_{GS}=-8V, V_{DS}=0V, f = 1 MHz V_{DS}=15V, I_D = 5 mA, f = 1 MHz	- -	0.34 0.25	0.5 0.38	pF pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz	-	6	8	pF
Small-Signal, Drain-to-Source Capacitance	C_{ds}	V_{DS} = 0V, V_{GS} = -8V, f = 1 MHz	-	-	3	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	V_{GS} = 0V, V_{DS} = +15V	-	10,000	-	µmho
Offset Voltage	V_o	V_{GS} = +6,-8V; V_{DS} = 0V	-	0*	-	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No.107-1.0.1, or equivalent.

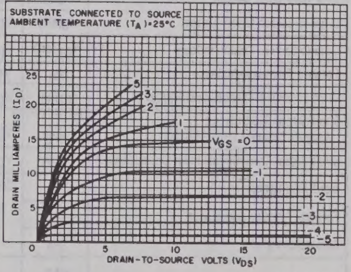


Fig.1 - Drain current vs. drain-to-source voltage.

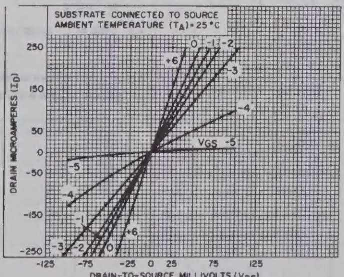


Fig.2 - Low-level drain current vs. drain-to-source voltage.

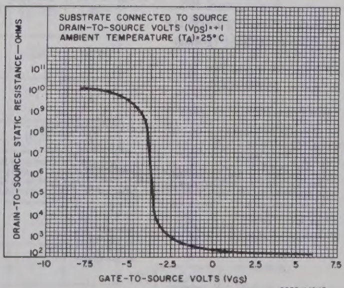


Fig.3 - Drain-to-source static resistance vs. gate-to-source voltage.

3N154

Silicon MOS Transistor N-Channel Depletion Type

For Critical Amplifier Applications in Military & Industrial
VHF Communications Equipment Operating up to 250 MHz

RCA 3N154 is an n-channel depletion-type silicon insulated-gate field-effect transistor utilizing the MOS■ construction. It is intended primarily for vhf amplifier applications up to 250 MHz in military and industrial equipment.

Because of its improved transfer characteristic and exceptionally wide dynamic range, the 3N154 can provide substantially better crossmodulation performance in linear amplifier applications than conventional bipolar transistors. The extremely low gate leakage current eliminates diode-current loading of the input circuit under strong signal conditions, a problem which is common to junction-type FET's. These features, in addition to low feedback capacitance, permit the design of circuits providing superior high-frequency operation and high gain without neutralization. The 3N154 utilizes full-gate construction and is hermetically sealed in a JEDEC TO-72 metal package.

■ Metal-Oxide-Semiconductor

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

*DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
*DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:		
* CONTINUOUS (dc)	+1, -8	V
* PEAK ac	±15	V
*DRAIN CURRENT, I_D▲	50	mA
*TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate at 2.2	mW/°C
*AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265	°C

In accordance with JEDEC Registration Data Format JS9-RDF-11B

▲ Pulsed:
Pulse duration ≤ 20 ms
Duty factor ≤ 0.15

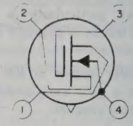
Device Feature:

- **Closely controlled I_{DSS} – 10 to 25 mA**
- **Low gate leakage current – I_{GSS} = 0.1 pA typ.**
- **Low feedback capacitance – C_{rss} = 0.25 pF typ.**
- **High forward transconductance – g_{fs} = 7500 µmho typ.**
- **High vhf power gain – G_{PS} = 16 dB typ. at 200 MHz**
- **Low vhf noise figure – NF = 3.5 dB typ. at 200 MHz**
- **Exceptionally good cross-modulation characteristics**

Performance Features

- **Large dynamic range**
- **Greatly reduced spurious responses**
- **Permits use of vacuum-tube biasing techniques**
- **Excellent thermal stability**
- **Superior cross-modulation performance and greater dynamic range than bipolar transistors**

TERMINAL DIAGRAM



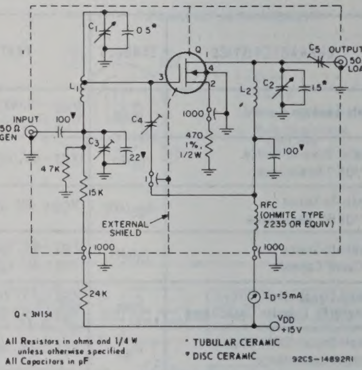
1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

ELECTRICAL CHARACTERISTICS: (At T_A = 25° C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

	CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS 3N154 Min.	LIMITS 3N154 Typ.	LIMITS 3N154 Max.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V, T_A = 25° C	-	0.0001	0.05	nA
			V_{DS} = 0, V_{GS} = -8 V, T_A = 125° C	-	-	5	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 25° C	-	0.0001	0.05	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 125° C	-	-	5	nA
*	Zero-Bias Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	10	15	25	mA
	Drain-to-Source Cutoff Current	I_D(off)	V_{DS} = 20 V, V_{GS} = -8 V	-	-	50	µA
*	Gate-to-Source Cutoff Voltage	V_{GS}(off)	V_{DS} = 15 V, I_D = 50 µA	-0.5	-3	-8	V
	Forward Transsconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	µmho
	Drain-to-Source Channel Resistance	r_{DS}(on)	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.15	0.25	0.35	pF
	Small-Signal Short-Circuit Input Capacitance ▲	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.5	7	pF
	Input Admittance	Y_{is}	Common Source Configuration f = 200 MHz, V_{DS} = 15 V, I_D = 5 mA	-	0.4 + J7.3	-	mmho
	Forward Transfer Admittance	Y_{fs}		-	7 – J2	-	mmho
	Output Admittance	Y_{os}		-	0.28 + J1.8	-	mmho
	Maximum Available Power Gain	MAG	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	21	-	dB
*	Insertion Power Gain (Fixed Neutralization) (see Fig. 1)	G_{PS}		13.5	16	-	dB
*	Noise Figure (see Figs. 1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	3.5	5	dB

* In Accordance with JEDEC Registration Data Format JS-9 RDF-11B
▲ Three-Terminal Measurement: Source Returned to Guard Terminal



C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

Q = 3N154

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig. 1 - Test circuit used to measure 200-MHz maximum usable power gain and noise figure

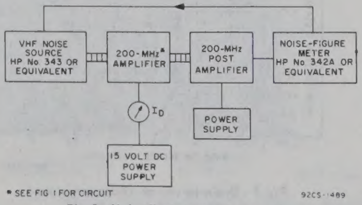


Fig. 2 - Noise figure measurement setup

For characteristics curves, refer to types 3N128 and 3N143.

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTOR

N-Channel Depletion Type

For Military and Industrial Low-Noise RF-Amplifier Applications Up to 300 MHz

The 3N159 is an n-channel silicon, depletion type, dual insulated-gate, field-effect transistor utilizing the MOS** construction. It has exceptional characteristics for rf-amplifier applications at frequencies up to 300 MHz. This transistor features a series arrangement of two separate channels, each channel having an independent control gate.

Type 3N159 has an exceptionally low-noise figure, which makes this type particularly suitable for critical vhf applications. When used in a common-source configuration in which gate No.2 is ac grounded, this device reduces oscillator feedthrough to the antenna thereby minimizing oscillator radiation.

The 3N159 is hermetically sealed in the metal JEDEC TO-72 package.

** Metal-Oxide-Semiconductor.

APPLICATIONS

- **RF amplifier in military and industrial communications equipment**
- **aircraft, marine and vehicular receivers**
- **CATV and MATV equipment**
- **telemetry and multiplex equipment**

Maximum Ratings, *Absolute-Maximum Values:* **at $T_A = 25^\circ C$**

DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . . . 0 to +20 V

GATE-No.1-TO-SOURCE VOLTAGE, V_{G1S}:
- Continuous (dc) . . . . -8 to +1 V
- Peak ac . . . . -8 to +20 V

GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:
- Continuous (dc) . . . . -8 to 40% of V_{DS} V
- Peak ac . . . . -8 to +20 V

DRAIN-TO-GATE VOLTAGE:
- V_{DG1} or V_{DG2} . . . . +20 V

DRAIN CURRENT, I_D
- Pulsed: Pulse duration $\leq$ 20 ms, duty factor $\leq$ 0.15 . . . . 50 mA

TRANSISTOR DISSIPATION, P_T:
- At ambient temperatures up to 25°C . . . . 400 mW
- At ambient temperatures above 25°C . . . . derate linearly at 2.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Storage and Operating . . . . -65 to +175 °C

LEAD TEMPERATURE (During soldering):
- At distances $\geq$ 1/32 inch from seating surface for 10 seconds max. . . . . 265 °C

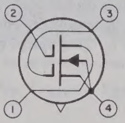
PERFORMANCE FEATURES

- **wide dynamic range permits large-signal handling before overload**
- **dual-gate permits simplified agc circuitry**
- **virtually no agc power required**
- **greatly reduces spurious responses in FM receivers**
- **permits use of vacuum-tube biasing techniques**
- **excellent thermal stability**
- **superior cross-modulation performance and greater dynamic range than bipolar or single-gate field-effect transistors**

DEVICE FEATURES

- **low gate leakage currents – –** I_{G1SS} & I_{G2SS} = 1 nA max.
- **high forward transconductance – –** g_{fs} = 7000 µmho min.
- **high unneutralized RF power gain – –** G_{ps} = 16 dB min. at 200 MHz
- **low vhf noise figure – –** NF = 3.5 dB max. at 200 MHz

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ C$ unless otherwise specified

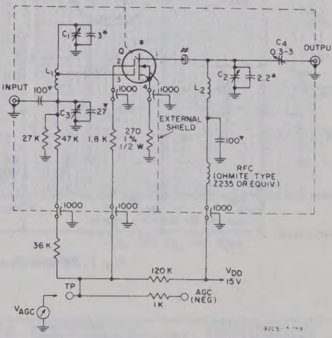
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS 3N159 Min.	LIMITS 3N159 Typ.	LIMITS 3N159 Max.	UNITS
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +16V, I_D = 200 µA V_{G2S} = +4V	-	-2	-4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +16V, I_D = 200 µA V_{G1S} = 0	-	-2	-4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G1S} = +1V, V_{G2S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G1S} = -20V, V_{G2S} = 0 V_{DS} = 0, T_A = 125°C	-	-	0.2	µA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G2S} = +1, V_{DS} = 0 V_{G1S} = 0, T_A = 25°C	-	-	1	nA
		V_{G2S} = -20V, V_{G1S} = 0 V_{DS} = 0, T_A = 125°C	-	-	0.2	µA
Zero-Bias Drain Current	I_{DSS}*	V_{DD} = +14V, V_{G1S} = 0 V_{G2S} = +4V	5	18	30	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DD} = +14V, I_D = 10 mA V_{G2S} = +4V, f = 1 kHz	7000	10,000	18,000	µmho
Cutoff Forward Transconductance (Gate-No.1-to-Drain)	$g_{fs(off)}$	V_{DD} = +14V, V_{G1S} = -0.5V V_{G2S} = -2V, f = 1 kHz	-	-	100	µmho
Small-Signal, Short-Circuit Input Capacitance▲	C_{iss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	3	5.5	7	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1)♦	C_{rss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	0.01	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	-	2.2	-	pF
Maximum Usable Power Gain (See Fig.1 for Measurement Circuit)	MUG	V_{DD} = +15V, R_S = 270Ω R_G = 50Ω, f = 200 MHz	16	18	22	dB
Measured Noise Figure (See Fig.1 for Measurement Circuit)	NF	V_{DD} = +15V, R_S = 270Ω f = 200 MHz, R_G = 50Ω	-	2.5	3.5	dB

* Pulse Test: Pulse duration $\leq$ 20 ms, duty factor $\leq$ 0.15.

▲ Capacitance between Gate No.1 and all other terminals.

♦ Three-Terminal Measurement with Gate No.2 and Source Returned to Guard Terminal.

For characteristics curves refer to types 3N140, 3N141.



■ Tubular ceramic

▼ Disc ceramic

# Ferrite bead (1/2 used); Indiana General No. H 1742C-(A-147) or F1157-1-H or equivalent.

‡ VHF plug in socket Jettron CD72-148 and CD72149 (part No.7977-1) or equivalent.

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200-MHz power gain and noise-figure test circuit for type 3N159.

3N187

Silicon Dual Insulated-Gate Field-Effect Transistor

N-Channel Depletion Type

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 300 MHz

Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance – g_{fs} = 12,000 μmho (typ.)
- High unneutralized RF power gain – G_{ps} = 18 dB(typ.) at 200 MHz
- Low VHF noise figure – 3.5 dB(typ.) at 200 MHz

RCA-3N187 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS▲ pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N187 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N187 make it useful for a wide variety of rf-amplifier applications at frequencies up to 300 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N187 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N187 is hermetically sealed in the metal JEDEC TO-72 package.

▲ Metal-Oxide-Semiconductor

Maximum Ratings,

Absolute-Maximum Values, at T_A = 25°C

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No. 1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No. 2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
* LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265	°C

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* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

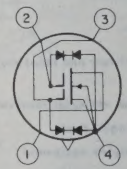
Applications

- RF amplifier, mixer, and IF amplifier in military, and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

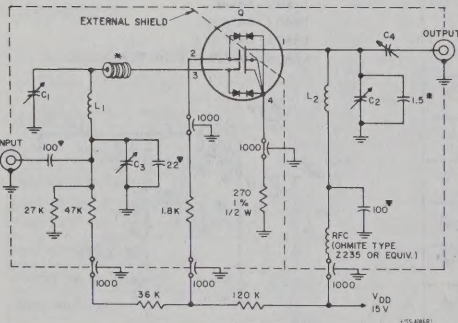
Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's
- Wide dynamic range permits large-signal handling before overload
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

TERMINAL DIAGRAM



LEAD 1-DRAIN
LEAD 2-GATE No. 2
LEAD 3-GATE No. 1
LEAD 4-SOURCE, SUBSTRATE AND CASE



# Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.

All resistors in ohms

All capacitors in pF

Q = 3N187

▼ Disc ceramic.

* Tubular ceramic.

C_1: 1.8 – 8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.

C_2: 1.5 – 5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.08 in.

L_2: 4½ turns silver-plated 0.02-in thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil ≈ .90 in. long.

Fig. 1 - 200-MHz Power gain and noise-figure test circuit

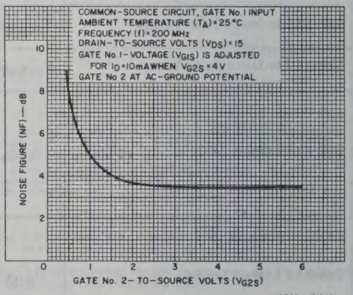


Fig. 2 - NF vs. V_{G2S}

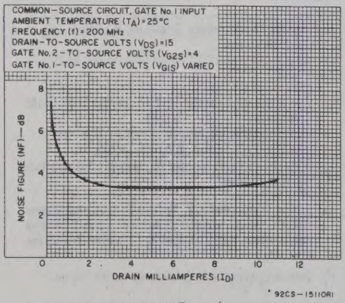


Fig. 3 - NF vs. I_D

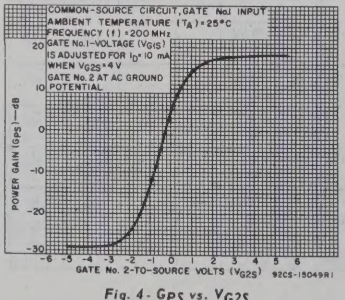


Fig. 4 - G_{PS} vs. V_{G2S}

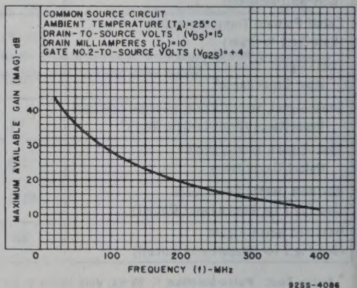


Fig. 5 - MAG. vs. f

ELECTRICAL CHARACTERISTICS, at T_A = 25° C unless otherwise specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
				Min.	Typ.	Max.	
* Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		−0.5	−2	−4	V
* Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		−0.5	−2	−4	V
* Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V	T_A = 25° C	–	–	50	nA
		V_{G2S} = V_{DS} = 0	T_A = 100° C	–	–	5	μA
* Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V	T_A = 25° C	–	–	50	nA
		V_{G2S} = V_{DS}=0	T_A = 100° C	–	–	5	μA
* Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V	T_A = 25° C	–	–	50	nA
		V_{G1S} = V_{DS}=0	T_A = 100° C	–	–	5	μA
* Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V	T_A = 25° C	–	–	50	nA
		V_{G1S} = V_{DS} = 0	T_A = 100° C	–	–	5	μA
* Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V V_{G2S} = +4 V V_{G1S} = 0		5	15	30	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1kHz		7000	12,000	18,000	μmho
* Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz		4.0	6.0	8.5	pF
* Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1)♦	C_{rss}			0.005	0.02	0.03	pF
* Small-Signal, Short-Circuit Output Capacitanc	C_{oss}			–	2.0	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 200 MHz		16	18	22	dB
Maximum Available Power Gain	MAG			–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG			–	20▲	–	dB
Noise Figure (see Fig. 1)	NF			–	3.5	4.5	dB
* Magnitude of Forward Transadmittance	$\|Y_{fs}\|$			–	12,000	–	μmho
* Phase Angle of Forward Transadmittance	θ			–	−35	–	Degrees
Magnitude of Reverse Transadmittance	$\|Y_{rs}\|$			–	25	–	μmho
Angle of Reverse Transadmittance	θ_{rs}			–	−25	–	Degrees
* Input Resistance	r_{iss}			–	1.0	–	kΩ
* Output Resistance	r_{oss}			–	2.8	–	kΩ
* Gate-to-Source Forward Breakdown Voltage: Gate No. 1 Gate No. 2	 $V_{(BR)G1SSF}$ $V_{(BR)G2SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA		6.5	10	–	V
* Gate-to-Source Reverse Breakdown Voltage: Gate No. 1 Gate No. 2	 $V_{(BR)G1SSR}$ $V_{(BR)G2SSR}$	I_{G1SSR} = I_{G2SSR} = -100 μA		−6.5	−10	–	V

▲ Limited only by practical design considerations.

† Capacitance between Gate No. 1 and all other terminals

♦ Three-terminal measurement with Gate No. 2 and Source returned to ground terminal.

* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

OPERATING CONSIDERATIONS

The flexible leads of the 3N187 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

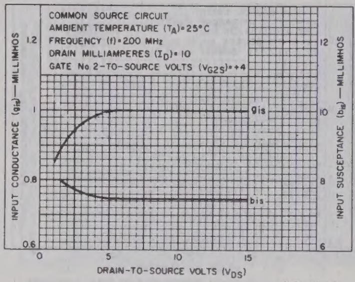


Fig. 8 - y_{is} vs. V_{DS}

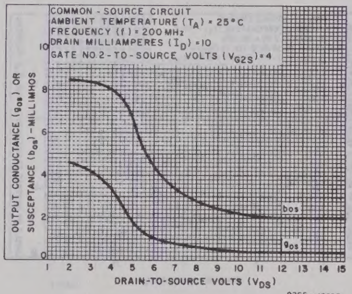


Fig. 9 - y_{os} vs. V_{DS}

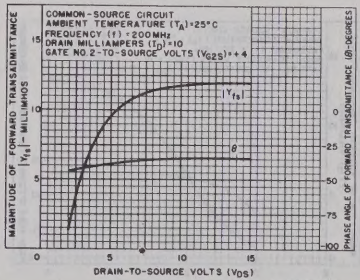


Fig. 10 - y_{fs} vs. V_{DS}

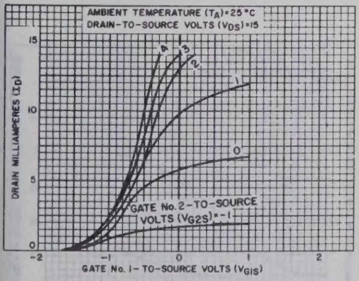


Fig. 6 - I_D vs. V_{G1S}

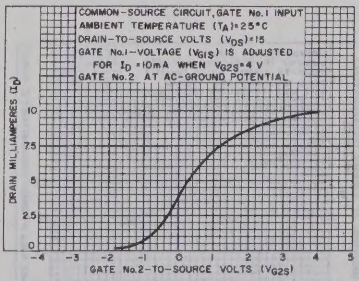


Fig. 7 - I_D vs. V_{G2S}

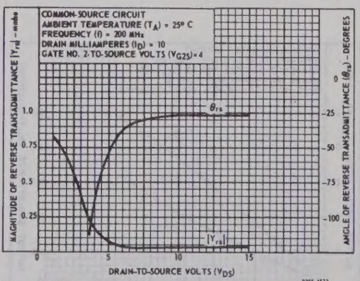


Fig. 11 - y_{rs} vs. V_{DS}

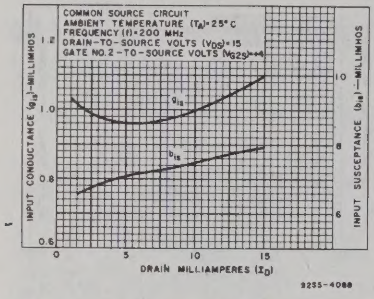


Fig. 12 - y_{is} vs. I_D

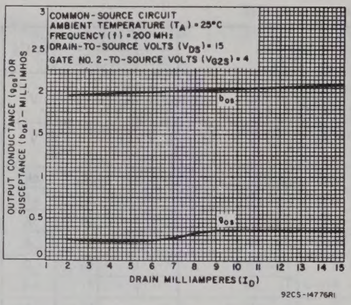


Fig. 13 - y_{os} vs. I_D

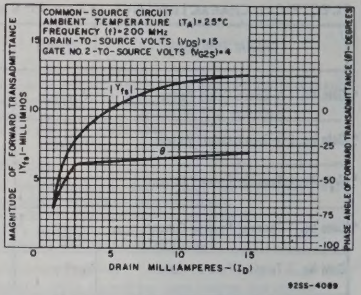


Fig. 14 - y_{fs} vs. I_D

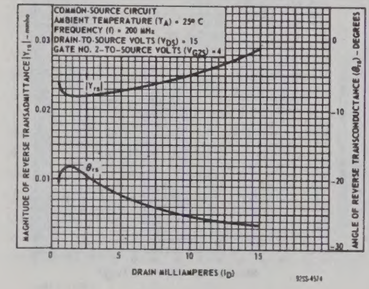


Fig. 15 - y_{rs} vs. I_D

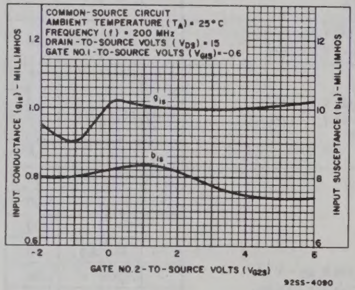


Fig. 16 - y_{is} vs. V_{G2S}

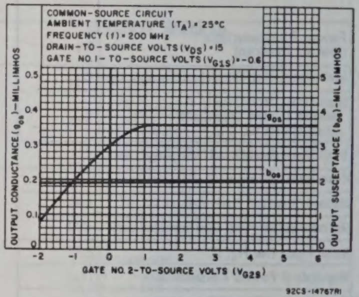


Fig. 17 - y_{os} vs. V_{G2S}

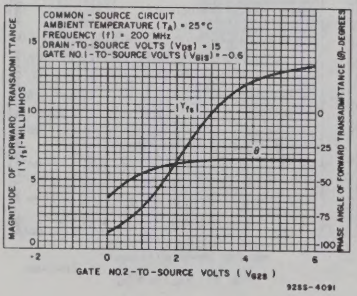


Fig. 18 - y_{fs} vs. V_{G2S}

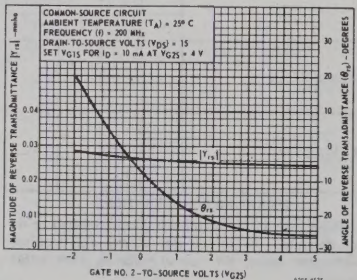


Fig. 19 - y_{rs} vs. V_{G2S}

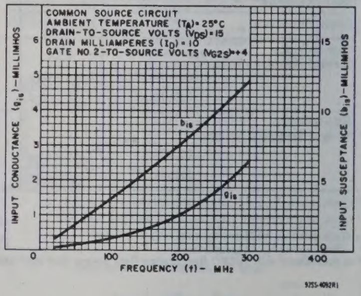


Fig. 20 - y_{is} vs. frequency

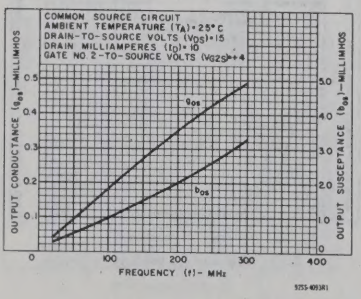


Fig. 21 - y_{os} vs. frequency

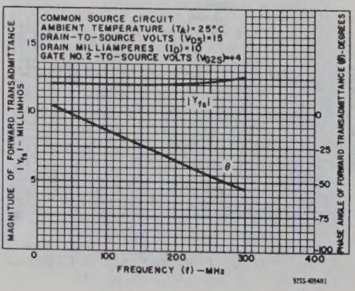


Fig. 22 - y_{fs} vs. frequency

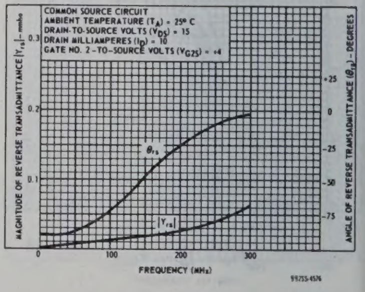


Fig. 23. - y_{rs} vs. frequency

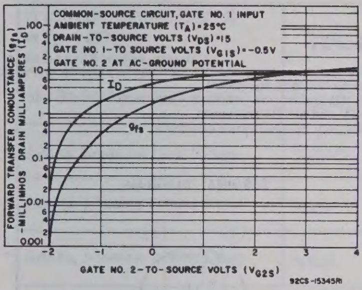


Fig. 24 - g_{fs} and I_D vs. V_{G2S}

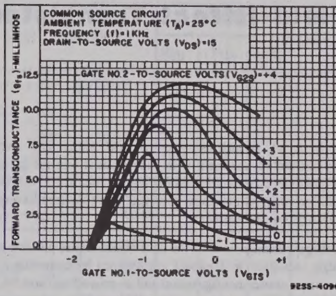


Fig. 25. - g_{fs} vs. V_{G1S}

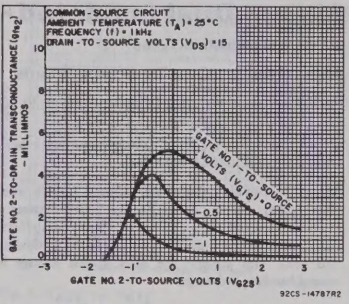


Fig. 26 - g_{fs_2} vs. V_{G2S}

3N200

Silicon Dual Insulated-Gate Field-Effect Transistor

N-Channel Depletion Types

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 500 MHz

RCA-3N200 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N200 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N200 make it useful for a wide variety of rf-amplifier applications at frequencies up to 500 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

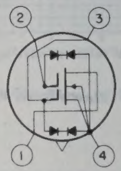
The two-gate arrangement of the 3N200 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N200 is hermetically sealed in the metal JEDEC TO-72 package.

Applications

- RF amplifier, mixer, and IF amplifier in military and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
* LEAD TEMPERATURE (During soldering):		
At distances ≥1/32 inch from seating surface for 10 seconds max.	265	°C

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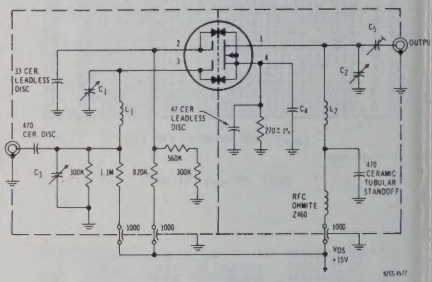
*In accordance with JEDEC registration data format (JS-9 RDF-19A)

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- Wide dynamic range permits large-signal handling before overload
- Dual-gate permits simplified agc circuitry
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance — g_{fs} = 15,000 μmho (typ.)
- High unneutralized RF power gain — G_{ps} = 12.5 dB (typ.) at 400 MHz = 19 dB (typ.) at 200 MHz
- Low VHF noise figure — 3.9 dB (typ.) at 400 MHz 3.0 dB (typ.) at 200 MHz



All resistances in ohms
All capacitances in pF

C_1, C_2: 1.3-5.4 pF variable air capacitor: Hammerland Mac 5 type or equivalent
C_3: 1.9-13.8 pF variable air capacitor: Hammerland Mac 15 type or equivalent
C_4: Approx. 300 pF - capacitance formed between socket cover & chassis
C_5: 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent
L_1, L_2: Inductance to tune circuit

Fig. 1 - 400 MHz power gain and noise figure test circuit

y and s Parameters vs. Frequency

TEST CONDITIONS: Drain-to-Source Volts (V_{DS}) = 15, Drain Milliamperes (I_D) = 10, Gate No. 2-to-Source Volts (V_{G2S}) = 4

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz)					UNITS
		100	200	300	400	500	
Maximum Available Power Gain	MAG	32	24	17.5	13	10	dB
Maximum Usable Power Gain (Unneutralized)*	MUG	32	24	17.5	13	10	dB
Y Parameters							
Input Conductance	g_{is}	0.25	0.8	2.0	3.6	6.2	mmho
Input Susceptance	b_{is}	3.4	5.8	8.5	11.2	15.5	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs}\rvert$	15.3	15.3	15.4	15.5	16.3	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	− 15	− 25	− 35	− 47	− 60	degrees
Output Conductance	g_{os}	0.15	0.3	0.5	0.8	1.1	mmho
Output Susceptance	b_{os}	1.5	2.7	3.6	4.25	5.0	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs}\rvert$	0.012	0.025	0.06	0.14	0.26	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	− 60	− 25	0	14	20	degrees
S Parameters							
Magnitude of Input Reflection Coeff.	$\lvert s_{is}\rvert$	0.97	0.90	0.84	0.78	0.70	
Angle of Input Reflection Coeff.	$\angle s_{is}$	− 20	− 32	− 55	− 68	− 82	degrees
Magnitude of Forward Transmission Coeff.	$\lvert s_{fs}\rvert$	1.50	1.40	1.25	1.1	0.9	
Angle of Forward Transmission Coeff.	$\angle s_{fs}$	153	133	112	90	70	degrees
Mangitude of Output Reflection Coeff.	$\lvert s_{os}\rvert$	0.985	0.95	0.93	0.92	0.91	
Angle of Output Reflection Coeff.	$\angle s_{os}$	− 7.5	− 16	− 22	− 28	− 34	degrees
Magnitude of Reverse Transmission Coeff.	$\lvert s_{rs}\rvert$	0.001	0.0025	0.005	0.010	0.0165	
Angle of Reverse Transmission Coeff.	$\angle s_{rs}$	100	125	141	150	142	degrees

*Limited only by practical design considerations

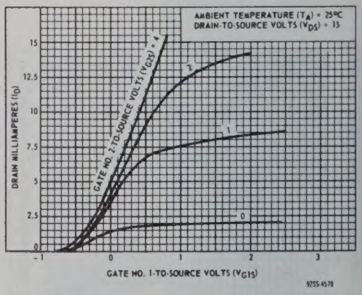


Fig. 2 - I_D vs. V_{G1S}

ELECTRICAL CHARACTERISTICS *at T_A = 25°C unless otherwise specified*	SYMBOLS	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
* Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		-0.1	-1	-3	V
* Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		-0.1	-1	-3	V
* Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0 V_{G2S} = +4 V		0.5	5.0	12	mA
* Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V I_D = 10 mA V_{G2S} = +4 V	f = 1 kHz	10,000	15,000	20,000	μmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}		f = 1 MHz	4.0	6.0	8.5	pF
* Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦	C_{rss}			0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2.0	–	pF
* Power Gain (see Fig. 1)	G_{PS}		f = 400 MHz	10	12.5	–	dB
Noise Figure (see Fig. 1)	NF			–	3.9	6.0	dB
* Bandwidth	BW			28	–	38	MHz
* Gate-to-Source Forward Breakdown Voltage Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	V_{G2S} = V_{DS} = 0	6.5	–	13	V
Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} = V_{DS} = 0				
* Gate-to-Source Reverse Breakdown Voltage Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	V_{G2S} = V_{DS} = 0	-6.5	–	- 13	V
Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} = V_{DS} = 0				

*In accordance with JEDEC registration data format (JS-9 RDF-19A)

†Capacitance between Gate No. 1 and all other terminals.

♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.

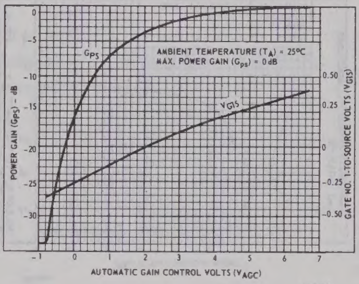


Fig. 5 - V_{AGC} vs. V_{G1S}

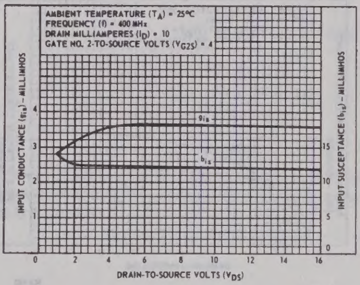


Fig. 6 - y_{is} vs. V_{DS}

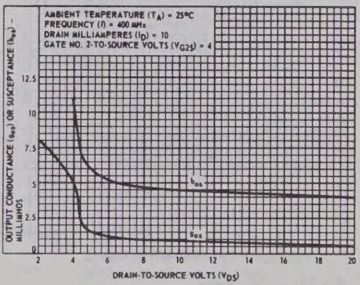


Fig. 7 - y_{os} vs. V_{DS}

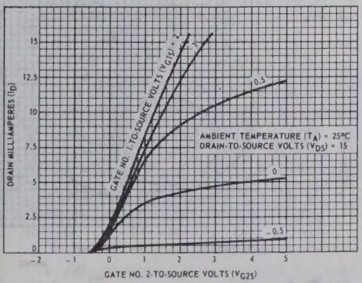


Fig. 3 - I_D vs. V_{G2S}

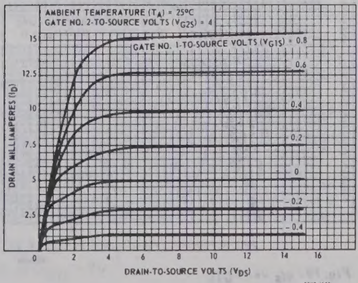


Fig. 4 - I_D vs. V_{DS}

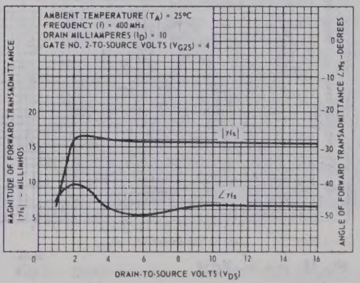


Fig. 8 - y_{fs} vs. V_{DS}

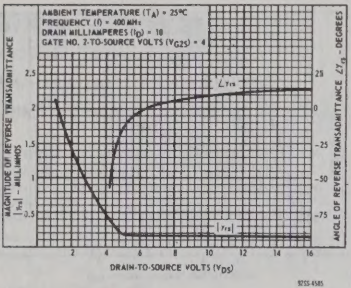


Fig. 9 - y_{rs} vs. V_{DS}

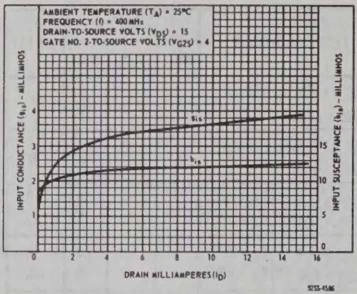


Fig. 10 - y_{is} vs. I_D

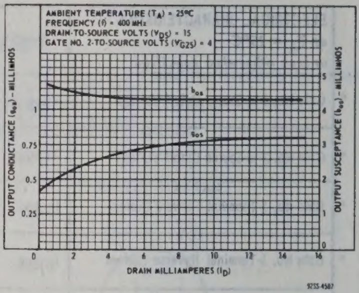


Fig. 11 - y_{os} vs. I_D

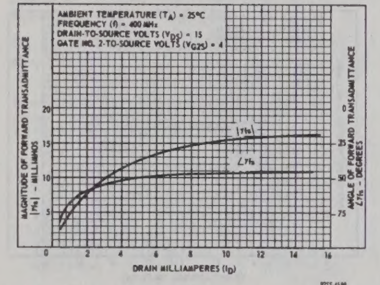


Fig. 12 - y_{fs} vs. I_D

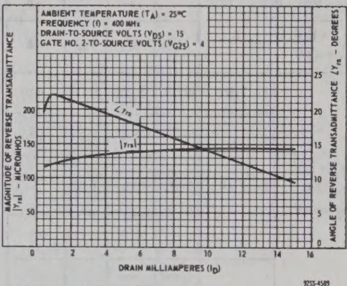


Fig. 13 - y_{rs} vs. I_D

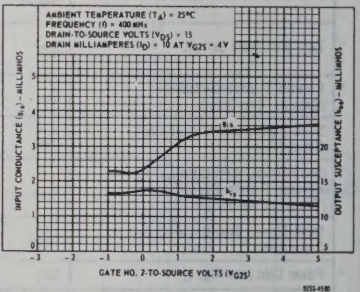


Fig. 14 - y_{is} vs. V_{G2S}

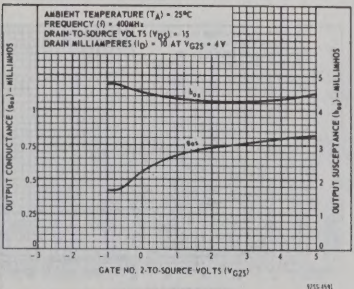


Fig. 15 - y_{os} vs. V_{G2S}

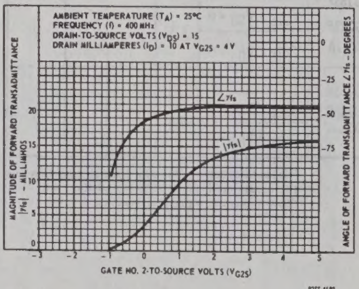


Fig. 16 - y_{fs} vs. V_{G2S}

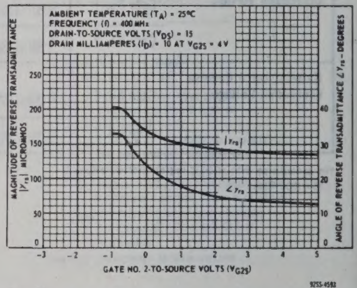


Fig. 17 - y_{rs} vs. V_{G2S}

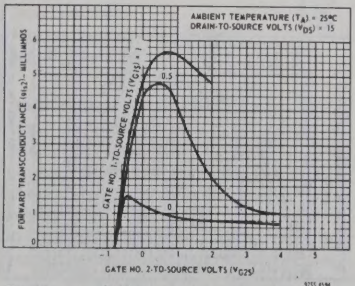


Fig. 18 - g_{fs} vs. V_{G2S}

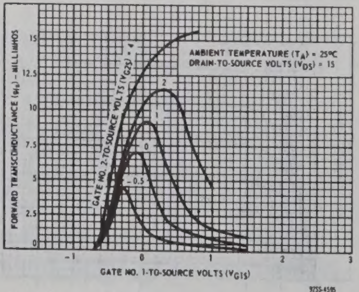


Fig. 19 - g_{fs} vs. V_{G1S}

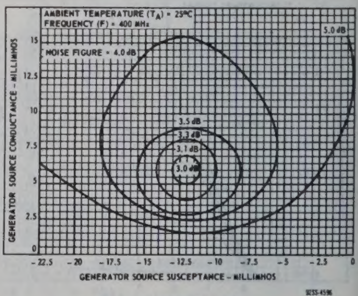


Fig. 20 - Noise figure vs. generator source admittance

3N204, 3N205, 3N206

Silicon Dual-Insulated-Gate Field-Effect Transistors

With Integrated Gate-Protection Circuits For VHF TV Applications

3N204 – RF Amplifier
3N205 – Mixer
3N206 – TV IF Amplifier

The RCA-3N204, 3N205, and 3N206 are n-channel silicon, depletion type, dual-insulated gate, field-effect transistors intended for vhf TV applications. Integrated back-to-back diodes protect the gates from excessive input voltages.

The 3N204 is intended for use in vhf rf amplifiers and delivers linear, low-noise amplification. Its extremely low feedback capacitance allows high-gain stable operation without neutralization. The 3N205 is specified for low noise vhf mixer applications. The 3N206 is intended for use in tuned high-frequency amplifiers such as TV if strips.

Features:

- Low C_{rss} – 0.03 pF max.
- High $|Y_{fs}|$ – 14 mmho typ. for 3N204 and 3N205
- Integrated gate-protection diodes

MAXIMUM RATINGS,
Absolute Maximum Values at $T_A = 25^oC$

* DRAIN-TO-GATE No.1 VOLTAGE	30	V
* DRAIN-TO-GATE No.2 VOLTAGE	30	V
* DRAIN-TO-SOURCE VOLTAGE	25	V
* GATE No.1-TERMINAL FORWARD CURRENT▲	10	mA
* GATE No.2-TERMINAL FORWARD CURRENT▲	10	mA
* GATE No.1-TERMINAL REVERSE CURRENT	–10	mA
* GATE No.2-TERMINAL REVERSE CURRENT	–10	mA
* CONTINUOUS DRAIN CURRENT	50	mA
* DEVICE DISSIPATION:		
Up to $T_A = 25^oC$	360	mW
Above $T_A = 25^oC$ derate linearly	2.4	mW/^oC
Up to $T_C = 25^oC$	1.2	W
Above $T_C = 25^oC$ derate linearly	8	mW/^oC
* AMBIENT TEMPERATURE RANGE:		
Operating	–65 to +175	^oC
Storage	–65 to +200	^oC
* LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+300	^oC

▲ Forward gate-terminal current is the current into a gate terminal with a forward-gate-to-source voltage applied. This voltage is of such polarity that an increase in its magnitude causes the channel resistance to decrease.
* In accordance with JEDEC registration data format (JS-9 RDF-19B)

OPERATING CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
3N204					
* Common-Source Spot Noise Figure, NF	V_{DD}=18 V, V_{GG}=7 V, f = 200 MHz, See Fig.13	–	–	3.5	dB
* Small-Signal Common-Source Insertion Power Gain, G_{ps}		20	–	28	dB
* Bandwidth, BW		7	–	12	MHz
* Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=18 V, ΔG_{ps}=–30dB,^{1} f=200 MHz, See Fig. 13	0	–	–2	V
* Common-Source Spot Noise Figure, NF	V_D=15 V, V_{G2S} = 4 V, f = 450 MHz, I_D = 10 mA, See Figs. 15 and 16	–	–	5	dB
* Small-Signal Common Source Insertion Power Gain, G_{ps}		14	–	–	dB
3N205					
* Small-Signal Conversion Power Gain, G_{ps} (conv)	V_{DD}=18 V, f_{LO}=245 MHz,^{3} f_{RF}=200 MHz, See Fig.17	17	–	28	dB
* Bandwidth, BW		4	–	7	MHz
3N206					
* Common-Source Spot Noise Figure, NF	V_{DD}=24 V, V_{GG}=6 V, f=45 MHz, See Fig. 14	–	–	4	dB
* Small-Signal Common-Source Insertion Power Gain, G_{ps}		25	–	35	dB
* Bandwidth, BW		3	–	6	MHz
* Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=24 V, ΔG_{ps}=–30dB,^{2} f=45 MHz, See Fig. 14	–1.6	–	0.6	V

*In accordance with JEDEC registration data format (JS-9 RDF-19B).
1. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7V.
2. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 6V.
3. Amplitude at input from local oscillator is 3 V RMS.

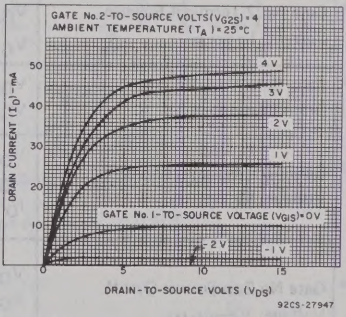


Fig.1 – Drain current vs. drain-to-source volts (pulse-tested with pulse duration = 300 μs, duty cycle ⩽2%).

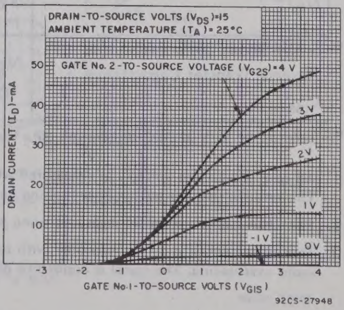


Fig.2 – Drain current vs. gate-No. 1-to-source volts (pulse-tested with pulse duration = 300 μs, duty cycle ⩽ 2%).

ELECTRICAL CHARACTERISTICS, At T_A = 25°C (unless otherwise specified)

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			MIN.	MAX.	
* Drain-to-Source Breakdown Voltage, $V_{(BR)DS}$	$I_D = 10\mu A$, $V_{G1S}=V_{G2S}= -5V$		25	–	V
* Gate No.1-to-Source Forward Breakdown Voltage, $V_{(BR)G1SSF}{}^1$	I_{G1}=10mA, $V_{G2S}=V_{DS}=0$		6	30	V
* Gate No.1-to-Source Reverse Breakdown Voltage, $V_{(BR)G1SSR}{}^1$	$I_{G1}= -10mA$, $V_{G2S}=V_{DS}=0$		–6	–30	V
* Gate No.2-to-Source Forward Breakdown Voltage, $V_{(BR)G2SSF}{}^1$	I_{G2}=10mA, $V_{G1S}=V_{DS}=0$		6	30	V
* Gate No.2-to-Source Reverse Breakdown Voltage, $V_{(BR)G2SSR}{}^1$	$I_{G2}= -10mA$, $V_{G1S}=V_{DS}=0$		–6	–30	V
* Gate No.1-Terminal Forward Current, I_{G1SSF}	V_{G1S}=5V, $V_{G2S}=V_{DS}=0$		–	10	nA
* Gate No.1-Terminal Reverse Current, I_{G1SSR}	$V_{G1S}= -5V$, $V_{G2S}=V_{DS}=0$	T_A=25°C	–	–10	nA
		T_A=150°C	–	–10	μA
* Gate No.2-Terminal Forward Current, I_{G2SSF}	V_{G2S}=5V, $V_{G1S}=V_{DS}=0$		–	10	nA
* Gate No.2-Terminal Reverse Current, I_{G2SSR}	$V_{G2S}= -5V$, $V_{G1S}=V_{DS}=0$	T_A=25°C	–	–10	nA
		T_A=150°C	–	–10	μA
* Zero-Gate No.1-Voltage Drain Current, $I_{DS}{}^2$	V_{DS}=15V, V_{GIS}=0, V_{G2S}=4V	3N204	6	30	mA
		3N205	6	30	
		3N206	3	15	
* Gate No.1-to-Source Cutoff Voltage, $V_{G1S(off)}$	V_{DS}=15V, V_{G2S}=4V, I_D=20μA		–0.5	–4	V
* Gate No.2-to-Source Cutoff Voltage, $V_{G2S(off)}$	V_{DS}=15V, V_{G1S}=0, I_D=20μA		–0.2	–4	V
* Small-Signal Common-Source Forward Transfer Admittance, $\|y_{fs}\|^3$	V_{DS}=15V, V_{G1S}=0, V_{G2S}=4V, f=1 kHz	3N204	10	22	mmho
		3N205	10	22	
		3N206	7	17	
* Small-Signal Common-Source Reverse Transfer Capacitance, C_{rss}	V_{DS}=15V, V_{G2S}=4V, I_D = 10 mA, f = 1 MHz		0.005	0.03	pF

*In accordance with JEDEC registration data format (JS-9 RDF-19B).

1. All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage-limiting network is functioning properly.
2. This characteristic must be measured using pulse techniques (t_W = 300μs, duty cycle ≤ 2%).
3. This characteristic must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate No.1 with gate No.2 at ac ground.

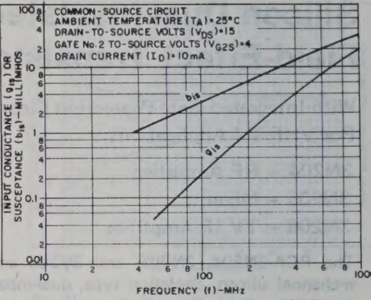


Fig.3 — Y_{is} vs. f

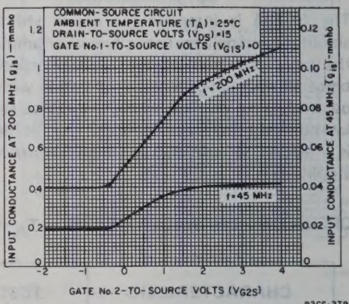


Fig.4 — Y_{is} vs. V_{G2S}

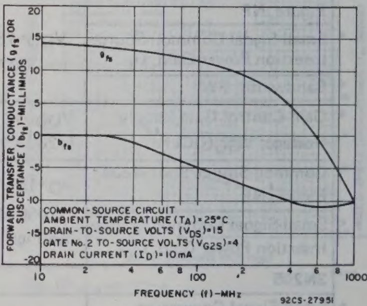


Fig.5 — Y_{fs} vs. f

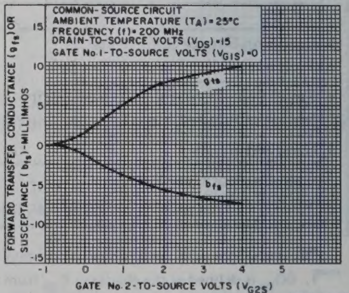


Fig.6 — Y_{fs} vs. V_{G2S}

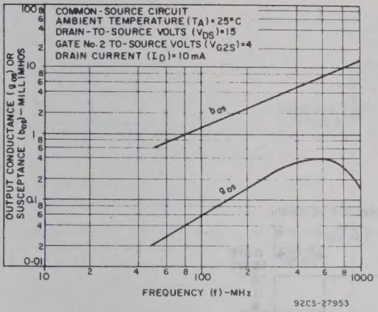


Fig.7 — Y_{OS} vs. f

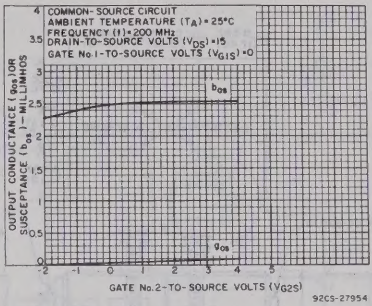


Fig.8 — Y_{os} vs. V_{G2S}

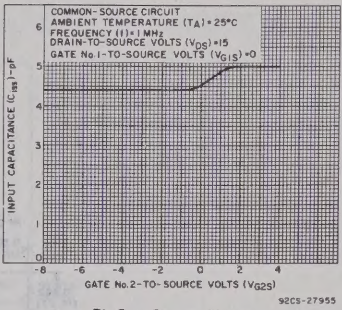


Fig.9 — C_{iss} vs. V_{G2S}

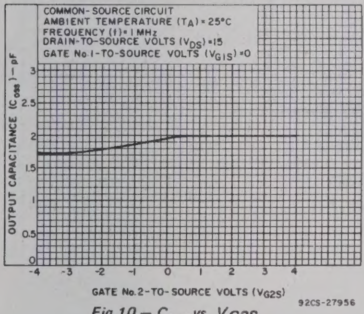
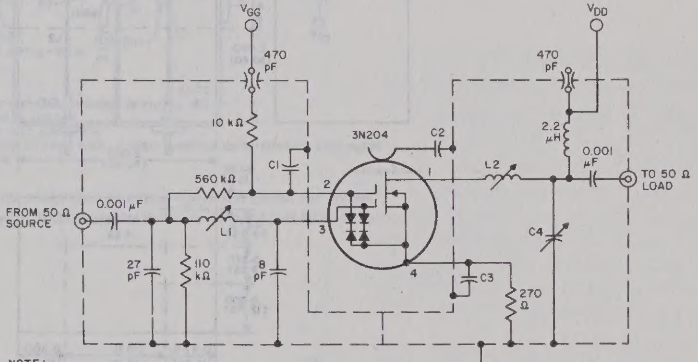


Fig.10 — C_{oss} vs. V_{G2S}



NOTE:
C1, C2, & C3: LEADLESS DISC CERAMIC, 0.001 µF
C4: ARCO 462, 5-80 pF, OR EQUIVALENT
L1: 3 TURNS No. 18 WIRE, 3/16 INCH-DIA. ALUMINUM SLUG
L2: 9 TURNS No. 20 WIRE, 3/16 INCH-DIA. ALUMINUM SLUG

92CS-27960

Fig.12 — 200-MHz power gain, gain-control voltage, and noise-figure test circuit for 3N204.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).

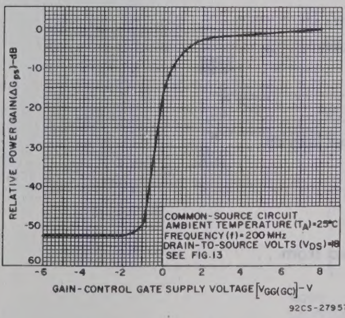
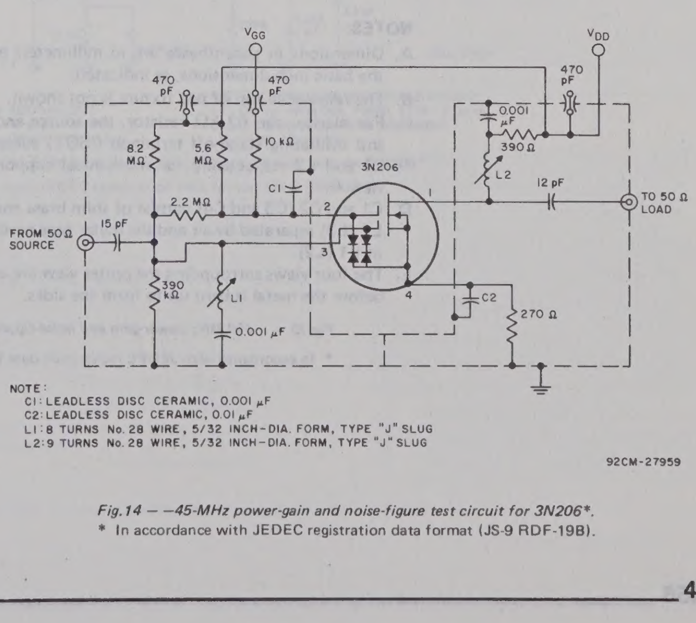


Fig.11 — ΔG_{ps} vs. $V_{GG(GC)}$



NOTE:
C1: LEADLESS DISC CERAMIC, 0.001 µF
C2: LEADLESS DISC CERAMIC, 0.01 µF
L1: 8 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG
L2: 9 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG

92CM-27959

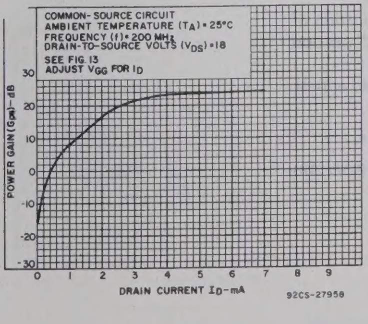
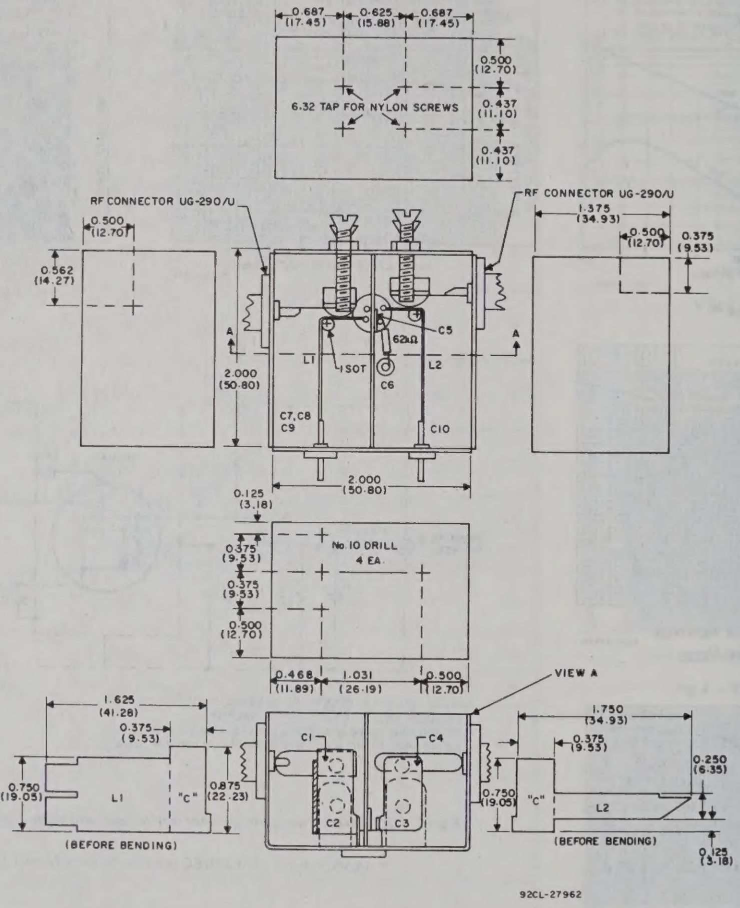


Fig.13 — G_{ps} vs. I_D

Fig.14 — –45-MHz power-gain and noise-figure test circuit for 3N206.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).



NOTES:

A. Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions, as indicated.

B. The removable top of test fixture is not shown.

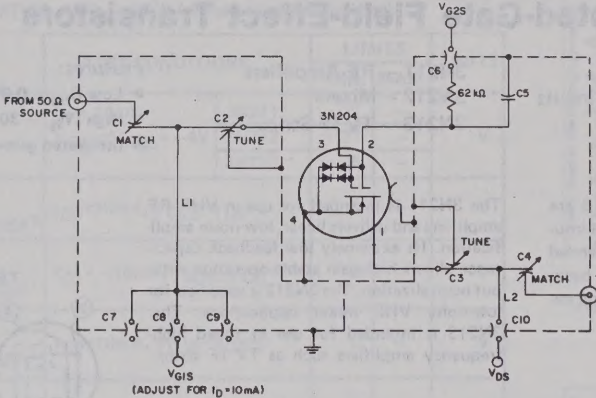
C. For clarity, the 62 kΩ resistor, the source and gate-2 socket pins, and insulating stand-off terminals (ISOT) soldered into the fold of L1 and L2 respectively for mechanical support, are not shown in view A.

D. C1 and C2 (C3 and C4) consist of shim brass and the "C" portion of L1 (L2) separated by air and the mylar tape covering the "C" portion of L1 (L2).

E. The four views surrounding the center view are as they would appear before the metal is bent up to form the sides.

Fig.15 – –450 MHz power-gain and noise-figure test fixture.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).

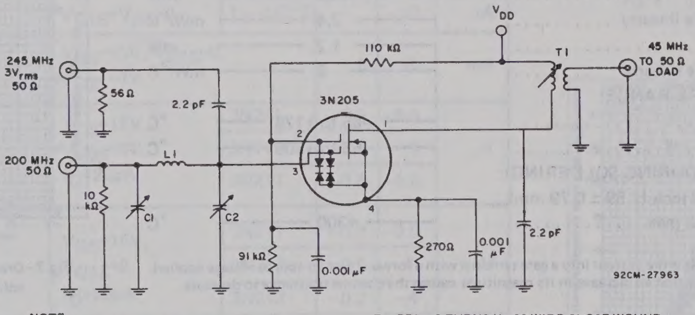


NOTE:
FOR TEST FIXTURE, SEE PICTORAL DRAWING IN FIGURE 16
C1 THRU C4: SEE FIGURE 16, NOTE D
C5: 0.001 μF LEADLESS DISC CAPACITOR
C6 THRU C10: ALLEN-BRADLEY F5AU 0.001 μF FEED-THROUGH CAPACITORS, OR EQUIVALENT
L1 & L2: SEE FIGURE 16

92CM-27961

Fig.16 — –450-MHz power-gain and noise-figure test circuit for 3N204.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).



NOTE:
C1: ARCO 462, 5–80 pF, or EQUIVALENT
C2: ARCO 460, 1.5–15 pF, OR EQUIVALENT
L1: 4 TURNS No.14 WIRE, 1/4 INCH INSIDE DIA.

T1: PRI: 16 TURNS No.30 WIRE CLOSE WOUND
ON 1/4 INCH DIA. FORM, TYPE "J" SLUG
SEC: 5 TURNS No.30 WIRE CENTERED
OVER PRIMARY

Fig.17 — –200 MHz-to-45-MHz circuit for conversion power gain for 3N205.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).

3N211, 3N212, 3N213

Silicon Dual-Insulated-Gate Field-Effect Transistors

N-Channel Depletion Types

With Integrated Gate-Protection Circuits
For VHF TV Applications

3N211 – RF Amplifiers
3N212 – Mixers
3N213 – TV IF Strips

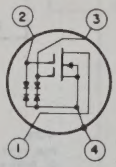
Features:

- **Low C_{rss} – 0.05 pF max.**
- **High $|Y_{fs}|$ – 30 mmho typ. for 3N211 and 3N212**
- **Integrated gate-protection diodes**

The RCA-3N211, 3N212, and 3N213 are n-channel silicon, depletion type, dual-insulated gate, field-effect transistors intended for VHF TV applications. Integrated back-to-back diodes protect the gates from excessive input voltages.

The 3N211 is intended for use in VHF RF amplifiers and delivers linear, low-noise amplification. Its extremely low feedback capacitance allows high-gain stable operation without neutralization. The 3N212 is specified for low-noise VHF mixer applications. The 3N213 is intended for use in tuned high-frequency amplifiers such as TV IF strips.

TERMINAL DIAGRAM
Bottom View



LEAD 1 – DRAIN
LEAD 2 – GATE No.2
LEAD 3 – GATE No.1
LEAD 4 – SOURCE, SUBSTRATE AND CASE

MAXIMUM RATINGS,
Absolute Maximum Values at T_A = 25°C

	3N211, 3N212	3N213	
DRAIN-TO-GATE No.1 VOLTAGE	35	40	V
DRAIN-TO-GATE No.2 VOLTAGE	35	40	V
DRAIN-TO-SOURCE VOLTAGE	27	35	V
GATE No.1-TERMINAL FORWARD CURRENT*	10		mA
GATE No.2-TERMINAL FORWARD CURRENT*	10		mA
GATE No.1-TERMINAL REVERSE CURRENT	–10		mA
GATE No.2-TERMINAL REVERSE CURRENT	–10		mA
CONTINUOUS DRAIN CURRENT	50		mA
DEVICE DISSIPATION:			
Up to T_A = 25°C	360		mW
Above T_A = 25°C derate linearly	2.4		mW/°C
Up to T_C = 25°C	1.2		mW
Above T_C = 25°C derate linearly	8		mW/°C
AMBIENT TEMPERATURE RANGE:			
Operating	–65 to +175		°C
Storage	–65 to +200		°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+300		°C

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* Forward gate-terminal current is the current into a gate terminal with a forward gate-to-source voltage applied. This voltage is of such polarity that an increase in its magnitude causes the channel resistance to decrease.

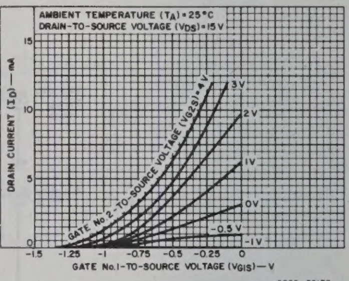


Fig.3–Drain current vs. gate No. 1-to-source voltage for all types.

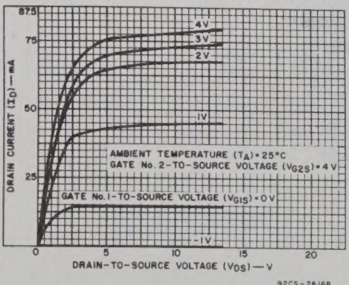


Fig.1–Drain current vs. drain-to-source voltage for all types.

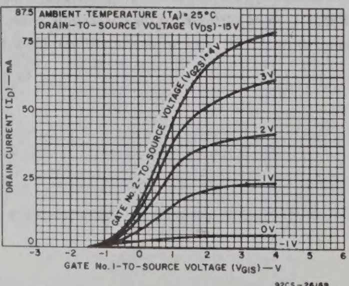


Fig.2–Drain current vs. gate No. 1-to-source voltage for all types.

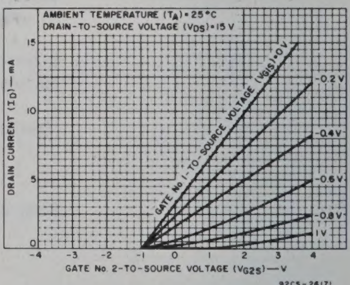


Fig.4–Drain current vs. gate No. 2-to-source voltage for all types.

(Figures 1 – 4 are pulse tested. Pulse duration = 300 µs, duty cycle ≤2%.)

ELECTRICAL CHARACTERISTICS, At $T_A = 25°C$ (unless otherwise specified)

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			MIN.	MAX.	
* Drain-to-Source Breakdown Voltage, $V_{(BR)DS}$	$I_D = 10\mu A$, $V_{G1S}=V_{G2S}=-4V$	3N211	27	–	V
		3N212	27	–	
		3N213	35	–	
* Gate No.1-to-Source Forward Breakdown Voltage, $V_{(BR)G1SSF}$[1]	$I_{G1}=10mA$, $V_{G2S}=V_{DS}=0$		6	–	V
* Gate No.1-to-Source Reverse Breakdown Voltage, $V_{(BR)G1SSR}$[1]	$I_{G1}=-10mA$, $V_{G2S}=V_{DS}=0$		−6	–	V
* Gate No.2-to-Source Forward Breakdown Voltage, $V_{(BR)G2SSF}$[1]	$I_{G2}=10mA$, $V_{G1S}=V_{DS}=0$		6	–	V
* Gate No.2-to-Source Reverse Breakdown Voltage, $V_{(BR)G2SSR}$[1]	$I_{G2}=-10mA$, $V_{G1S}=V_{DS}=0$		−6	–	V
* Gate No.1-Terminal Forward Current, I_{G1SSF}	$V_{G1S}=5V$, $V_{G2S}=V_{DS}=0$		–	10	nA
* Gate No.1-Terminal Reverse Current, I_{G1SSR}	$V_{G1S}=-5V$, $V_{G2S}=V_{DS}=0$	$T_A=25°C$	–	−10	nA
		$T_A=150°C$	–	−10	μA
* Gate No.2-Terminal Forward Current, I_{G2SSF}	$V_{G2S}=5V$, $V_{G1S}=V_{DS}=0$		–	10	nA
* Gate No.2-Terminal Reverse Current, I_{G2SSR}	$V_{G2S}=-5V$, $V_{G1S}=V_{DS}=0$	$T_A=25°C$	–	−10	nA
		$T_A=150°C$	–	−10	μA
* Zero-Gate No.1-Voltage Drain Current, I_{DS}[2]	$V_{DS}=15V$, $V_{G1S}=0$, $V_{G2S}=4V$		6	40	mA
* Gate No.1-to-Source Cutoff Voltage, $V_{G1S(off)}$	$V_{DS}=15V$, $V_{G2S}=4V$, $I_D=20\mu A$	3N211	−0.5	−5.5	V
		3N212	−0.5	−4	
		3N213	−0.5	−5.5	
* Gate No.2-to-Source Cutoff Voltage, $V_{G2S(off)}$	$V_{DS}=15V$, $V_{G1S}=0$, $I_D=20\mu A$	3N211	−0.2	−2.5	V
		3N212	−0.2	−4	
		3N213	−0.2	−4	
* Small-Signal Common-Source Forward Transfer Admittance, $\|y_{fs}\|$[3]	$V_{DS}=15V$, $V_{G1S}=0$, $V_{G2S}=4V$, f=1 kHz	3N211	17	40	mmho
		3N212	17	40	
		3N213	15	35	
* Small-Signal Common-Source Reverse Transfer Capacitance, C_{rss}	$V_{DS}=15V$, $V_{G2S}=4V$, $I_D=1mA$, f=1MHz		0.005	0.05	pF

*In accordance with JEDEC registration data format (JS-9 RDF-19B).

1. All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage-limiting network is functioning properly.
2. This characteristic must be measured using pulse techniques (t_W = 300μs, duty cycle ≤ 2%).
3. This characteristic must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate No.1 with gate No.2 at ac ground.

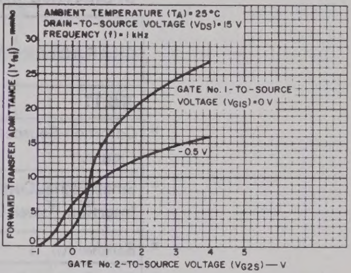


Fig. 5 – $|Y_{fs}|$ vs. V_{G2S} for 3N211 and 3N212.

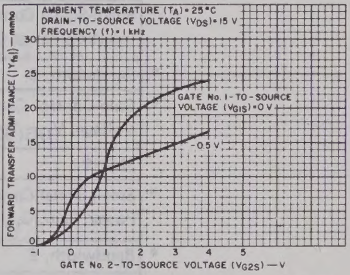


Fig. 6 – $|Y_{fs}|$ vs. V_{G2S} for 3N213.

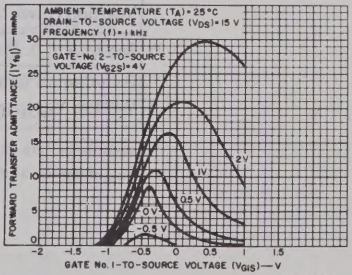


Fig. 7 – $|Y_{fs}|$ vs. V_{G1S} for 3N211, and 3N212.

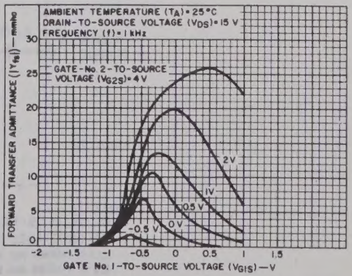


Fig. 8 – $|Y_{fs}|$ vs. V_{G1S} for 3N213.

OPERATING CHARACTERISTICS at $T_A = 25^\circ C$

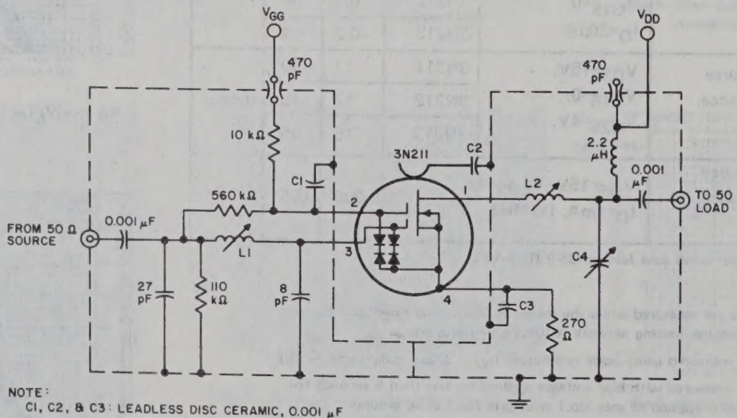
CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
3N211					
* Common-Source Spot Noise Figure, F	V_{DD}=18V, V_{GG}=7V, f = 200MHz, See Fig.9	–	–	3.5	dB
* Small-Signal Common-Source Insertion Power Gain, G_{ps}		24	–	35	dB
* Bandwidth, B		5	–	12	MHz
* Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=18V,ΔG_{ps}= –30dB,[1] f=200MHz, See Fig.9	0	–	–2	V
* Common-Source Spot Noise Figure, F	V_{DD}=24V, V_{GG}=6V, f=45MHz, See Fig.10	–	–	4	dB
* Small-Signal Common-Source Insertion Power Gain, G_{ps}		29	–	37	dB
* Bandwidth, B		3.5	–	6	MHz
* Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=24V, ΔG_{ps}= –30dB,[2] f=45MHz, See Fig.10	–	–	±1	V
3N212					
* Small-Signal Conversion Power Gain, G_{ps} (conv)	V_{DD}=18V, f_{LO}=245MHz,[3] f_{RF}=200MHz, See Fig.11	21	–	28	dB
* Bandwidth, B		4	–	7	MHz
3N213					
* Common-Source Spot Noise Figure, F	V_{DD}=24V, V_{GG}=6V, f=45MHz, See Fig.9	–	–	4	dB
* Small-Signal Common-Source Insertion Power Gain, G_{ps}		27	–	35	dB
* Bandwidth, B		3.5	–	6	MHz
* Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=24V, ΔG_{ps}= –30dB,[2] f=45MHz, See Fig.9	–	–	±1	V

*In accordance with JEDEC registration data format (JS-9 RDF-19B).

[1] ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7V.

[2] ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 6V.

[3] Amplitude at input from local oscillator is adjusted for maximum $G_{ps(conv)}$.

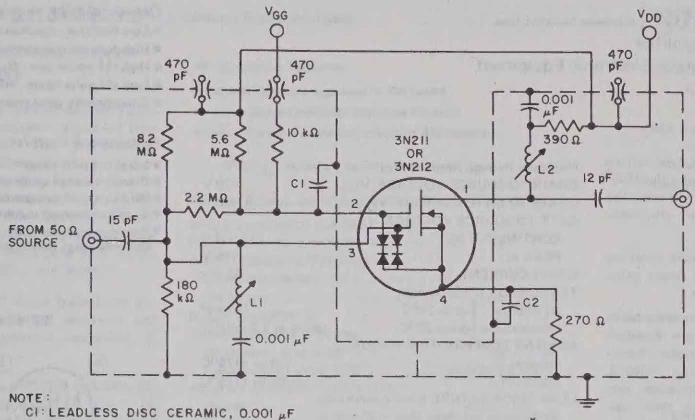


NOTE:
C1, C2, & C3: LEADLESS DISC CERAMIC, 0.001 µF
C4: ARCO 462, 5-80 pF, OR EQUIVALENT
L1: 3 TURNS No. 18 WIRE, 3/16 INCH-DIA. ALUMINUM SLUG
L2: 8 TURNS No. 20 WIRE, 3/16 INCH-DIA. ALUMINUM SLUG

* JEDEC REGISTERED DATA — — JEDEC RELEASE No. 6438.

92CM-26176

Fig.9—200 MHz power gain, gain control voltage, and noise figure test circuit for 3N211.*



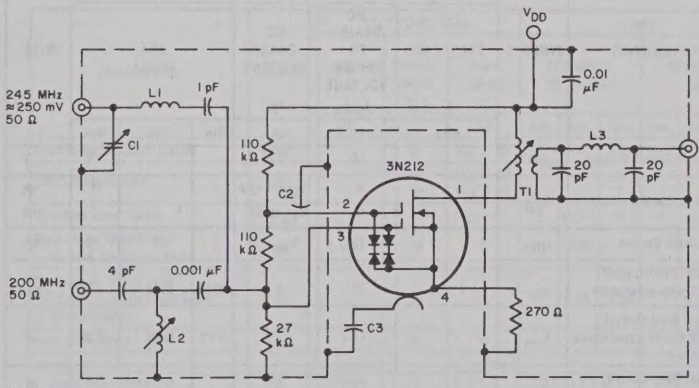
NOTE:
C1: LEADLESS DISC CERAMIC, 0.001 µF
C2: LEADLESS DISC CERAMIC, 0.01 µF
L1: 8 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG
L2: 9 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG

* JEDEC REGISTERED DATA -- JEDEC RELEASE No. 6438.

92CM-26177

Fig.10—45 MHz power gain and noise figure test circuit for 3N211 and 3N213.*

TEST CIRCUITS (CONT'D)



NOTE:
L1: 7 TURNS No. 34 WIRE, 1/4 INCH DIA. ALUMINUM SLUG
L2: 5 1/2 TURNS No. 20 WIRE, 1/4 INCH DIA. ALUMINUM SLUG
L3: 7 TURNS No. 24 WIRE, 1/4 INCH DIA. AIR CORE
T1: PRI: 25 TURNS No. 30 WIRE CLOSE WOUND ON 1/4 INCH DIA. FORM, TYPE "J" SLUG
SEC: 4 TURNS No. 30 WIRE CENTERED OVER PRIMARY
C1: ARCO TYPE 462, 5-80 pF
C2: 0.001 µF LEADLESS DISC
C3: 0.01 µF LEADLESS DISC

92CM-26178

* JEDEC REGISTERED DATA -- JEDEC RELEASE No. 6438.

Fig.11—200 MHz-to-45 MHz circuit for conversion power gain for 3N212.*

40467A

Silicon MOS Transistor N-Channel Depletion Type

For VHF Tuners and Other VHF Amplifier
Applications in Industrial & Commercial Electronic Equipment
Operating up to 220 MHz

RCA-40467A is an n-channel depletion-type silicon insulated-gate field-effect transistor utilizing the MOS■ construction. It is intended primarily for vhf-amplifier applications in industrial and commercial electronic equipment.

The 40467A is useful in vhf applications requiring devices capable of providing high useful power gains at frequencies up to approximately 220 MHz.

The 40467A features high forward transconductance, high dc gate-to-source resistance, and low feedback capacitance. Because of the improved transfer characteristic and increased dynamic range, the 40467A provides substantially better cross-modulation performance in linear-amplifier applications than conventional (bipolar) transistors and is free from diode-current loading, a problem that exists in junction type FET s. This device is hermetically sealed in the TO-72 metal case and utilizes full-gate construction.

Maximum Ratings, *Absolute-Maximum Values at T_A=25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 V
DRAIN-TO-GATE VOLTAGE, V_{DG}	+20 V
GATE-TO-SOURCE VOLTAGE, V_{GS}:	
CONTINUOUS (dc)	+1, −8 V
PEAK ac	+15 V
DRAIN CURRENT, I_D	50 mA
TRANSISTOR DISSIPATION:	
At ambient temperatures up to 25°C	330 mW
At ambient temperatures above 25°C	derate at 2.2 mW/°C
AMBIENT TEMPERATURE RANGE:	
Storage	−65 to +175°C
Operating	−65 to +175°C
LEAD TEMPERATURE (During Soldering):	
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265°C

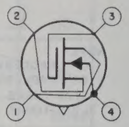
Device Features:

- **Low feedback capacitance - C_{rss} = 0.25 pF typ.**
- **High forward transconductance - g_{fs} = 7500 μmho typ.**
- **High vhf power gain - G_{PS} = 16 dB typ at 200 MHz**
- **Low vhf noise figure - NF = 3.5 dB typ at 200 MHz**
- **Exceptionally good cross-modulation characteristics**

Performance Features:

- **Large dynamic range**
- **Greatly reduced spurious responses**
- **Permits use of vacuum-tube biasing techniques**
- **Excellent thermal stability**
- **Superior cross-modulation performance and greater dynamic range than bipolar transistors**

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

ELECTRICAL CHARACTERISTICS AT T_C = 25°C WITH BULK (SUBSTRATE) CONNECTED TO SOURCE

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC DRAIN CURRENT I_D	LIMITS RCA 40467A			UNITS
		MHz	V	mA	Min	Typ.	Max.	
Gate-to-Source Cutoff Voltage	V_{GS}(off)		12	0.1	-	-	-8	V
Gate Leakage Current	I_{GSS}		0 0	V_{GS} = +1V V_{GS} = -8V	- -	- -	1 1	nA nA
Zero-Bias Drain Current	I_{DSS}		15	V_{GS} = 0	5	15	30	mA
Small-Signal, Short-Circuit Forward Transconductance	g_{fs}	1 KHz	15	5	4000	7500	-	μmho
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15	5	0.12	0.25	0.35	pF
Small Signal Short-Circuit Input Capacitance	C_{iss}	1	15	5	-	5.5	-	pF
Input Admittance	Y_{is}	Common Source Configuration f = 200 mHz V_{DS} = 15V I_D = 5 mA			-	0.4 + j7.3	-	
Forward Transfer Admittance	Y_{fs}				-	7 - J2	-	
Output Admittance	Y_{os}				-	0.28 + J1.8	-	
Maximum Available Power Gain	MAG	200	15	5	-	21	-	dB
Maximum Usable Power Gain (unneutralized)	MUG	200	15	5	-	12	-	dB
Maximum Usable Power Gain (neutralization)	MUG	200	15	5	12	16	-	dB
Noise Figure	NF	200	15	5	-	3.5	5	dB

For characteristics curves, refer to types 3N128 and 3N143.

■ Metal-Oxide Semiconductor

40468A, 40559A

MOS Silicon Transistors

N-Channel Depletion Types

For RF Amplifier and Mixer Applications in FM and AM/FM Receivers

RCA-40468A and 40559A are silicon insulated-gate field-effect transistors of the n-channel depletion type utilizing the MOS* construction. They are intended primarily for use as the rf amplifier and mixer, respectively, in FM receivers covering the 88 to 108 MHz band, but can be used for general amplifier applications at frequencies up to 125 MHz. For circuit design and typical performance data refer to RCA Application Note AN3535 "An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer".

The wide dynamic range of these transistors reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

Operating as a neutralized amplifier at 100 MHz, the 40468A can provide a power gain of 17 dB (typ.). A power gain of 14 dB (typ.) can be realized without neutralization.

Performance Features:

- **reduced spurious responses in FM tuners**
- **reverse bias on substrate improves linearity**
- **reduced cross-modulation effects in AM receivers**

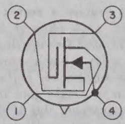
Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25^oC$:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
GATE-TO-SOURCE VOLTAGE, V_{GS}:		
CONTINUOUS (dc)	+1, -8	V
PEAK ac	±15	V
DRAIN CURRENT, I_D	25	mA
TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate at 2.2 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265	°C

Device Features:

- **high forward transconductance - -**
  gfs = 7500 μmho typ. for 40468A
- **low feedback capacitance - -**
  c_{rss} = 0.35 pF max. for 40468A
  0.38 pF max. for 40559A
- **high useful power gains - -**
  neutralized - 17 dB typ.
  unneutralized - 14 dB typ.
- **hermetically sealed in TO-72 metal package**

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

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* Metal-Oxide-Semiconductor.

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$
With Bulk (Substrate) Connected to Source Unless Otherwise Specified

Characteristics	Symbols	TEST CONDITIONS Frequency f	DC Drain-to-Source V_{DS}	DC Drain Current I_D	LIMITS RCA-40468A RF Amplifier Min.	Typ.	Max.	RCA-40559A Mixer Min.	Typ.	Max.	Units
		MHz	V	mA							
Drain-to-Source Cutoff Current	$I_D(off)$	-	12	V_{GS} = -8V	-	-	100	-	-	500	μA
Gate Leakage Current	I_{GSS}	- -	0 0	V_{GS} = -8V V_{GS} = +1V	- -	- -	1 1	- -	- -	1 1	nA nA
Zero-Bias Drain Current	I_{DSS}	-	15	V_{GS} = 0	5	15	30	5	15	30	mA
Small-Signal, Short-Circuit Forward Transconductance	g_{fs}	1 kHz	15	5	-	7500	-	-	-	-	μmho
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15	5	-	0.25	0.35	-	0.25	0.38	pF
Input Capacitance	C_{iss}	1	15	5	-	5.5	-	-	5.5	-	pF
Admittance	–	RF Mixer		RF Mixer	-			-			-
Input Admittance	Y_{is}	100 MHz	15	5 3	0.155 + j 3.45			0.14 + j 3.38			mmho
Forward Transfer Admittance	Y_{fs}	100 MHz	15	5 3	7.4 + j 0.9			-			mmho
Output Admittance	Y_{os}	100 MHz 10.7 MHz	15	5 3	0.21 + j 0.9			0.076 + j 0.153			mmho
Forward Conversion Transconductance	$g_{fs}(c)$	1 kHz	15	3	-	-	-	-	2800*	-	μmho
Maximum Available Power Gain	MAG	100	15	5	-	26	-	-	-	-	dB
Maximum Usable Power Gain (Unneutralized)	MUG	100	15	5	–	14	-	-	-	-	dB
Maximum Usable Power Gain (Neutralized)	MUG	100	15	5	14	17	-	-	-	-	dB
Maximum Available Conversion Gain	MAG_c	f_{in} = 100 f_{out} = 10.7	15	3	-	-	-	-	22	-	dB
Noise Figure	NF	100	15	5	-	3.5	5	-	-	-	dB

* Bulk (Substrate)-to-Source Volts (V_{BS}) = -3.

For characteristics curves, refer to types 3N128 and 3N143.

40600, 40601, 40602

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS

N-Channel Depletion Types

For VHF TV Receiver Applications

RCA 40600, 40601, and 40602 are n-channel depletion type, dual-insulated-gate, field-effect transistors utilizing the MOS construction. These devices have characteristics which make them highly desirable for rf-amplifier applications (40600), mixer applications (40601), and first-if-amplifier applications (40602) in vhf TV receivers and other types of commercial equipment operating at frequencies up to approximately 250 MHz.

These transistors feature a series arrangement of two separate channels, each channel having an independent control gate. In amplifier applications the 40600 and 40602 with their wide dynamic range provide substantially better cross-modulation performance than is obtainable with bipolar or single-gate field-effect transistors. In mixer applications the 40601 provides excellent isolation between the oscillator and rf signals because each of the two signal frequencies being mixed has its own control element. The wide dynamic range of the 40601 minimizes cross-modulation which is generally encountered in mixer stages.

Provision of two insulated gates also results in extremely low feedback capacitances (0.02 pF typ.), a feature which enables the 40600 and 40602 to provide high maximum useable power gains in unneutralized circuits – for example, 20 dB at 200 MHz typ. for the 40600, and 35 dB typ. at 44 MHz for the 40602. The gain of the rf and if stages can be controlled by applying agc voltage to gate No.2 and agc delay is easily obtained. Virtually no agc power is required for full gain reduction.

Types 40600, 40601, and 40602 are hermetically sealed in metal JEDEC TO-72 packages.

APPLICATIONS

- **VHF TV Receiver**
  - **40600 for rf amplifier applications**
  - **40601 for mixer applications**
  - **40602 for first-if-amplifier applications**

PERFORMANCE FEATURES

- **superior cross-modulation performance and greater dynamic range than bipolar and single-gate field-effect transistors**
- **permits use of vacuum-tube biasing techniques**
- **excellent thermal stability**

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS 40600, 40601, 40602 Min.	Typ.	Max.	UNITS
Gate No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15V, I_D = 200 μA V_{G2S} = +4V	-	-2	-	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15V, I_D = 200 μA V_{G1S} = 0	-	-2	-	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0, V_{DS} = 0	-	-	1	nA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0, V_{DS} = 0	-	-	1	nA
Drain Current	I_{DSS}	V_{DS} = +13V, V_{G1S} = 0, V_{G2S} = +4V	-	18	-	mA
Forward Transconductance	g_{fs}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 kHz	-	10000	-	μmho

TYPICAL PERFORMANCE CHARACTERISTICS, at T_A = 25°C

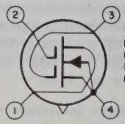
CHARACTERISTICS	SYMBOLS	40600 RF AMPLIFIER f = 200 MHz	40602 IF AMPLIFIER f = 44 MHz	40601 MIXER f = 200 MHz	UNITS
		V_{G1S} is adjusted for I_D = 10 mA Gate No.2 at AC ground potential V_{DS} = 13V, V_{G2S} = +4V		Local-oscillator injection Voltage on Gate No.2 = 750 mV V_{DS} = 15V V_{G2S} = +0.6V V_{G1S} = 0.75V	
Small-Signal, Short Circuit Reverse-Transfer Capacitance (Drain-to-Gate No.1) at f = 1 MHz	C_{rss}	0.02 typ. 0.03 max.	0.02 typ. 0.03 max.	0.02 typ. 0.03 max.	pF
Output Capacitance	C_{oss}	2.2	2.2	2.2 at f = 44 MHz	pF
Input Capacitance	C_{iss}	5.5	5.5	5.5	pF
Input Resistance	r_{iss}	1.2	10	1.2	KΩ
Output Resistance	r_{oss}	2.8	12	12 at f = 44 MHz	KΩ
Magnitude of Forward Transadmittance	$\|Y_{fs}\|$	11000	11000	2700*	μmho
Phase Angle of Forward Transadmittance	$\angle\theta$	-46	-11	-	degrees
Maximum Available Power Gain	MAG	20	35	14**	dB
Maximum Usable Power Gain (Unneutralized)	MUG_u	20▲	1 Stage 28 2 Stages 26 3 Stages 24	- - -	dB dB dB
Power Gain See Fig.1 for measurement circuit	G_{PS}	17.5	-	-	dB
Noise Figure	NF	5 max.	-	-	dB

* Magnitude of forward conversion transadmittance ** Maximum available conversion gain ▲ Limited by practical design considerations

DEVICE FEATURES

- **extremely low feedback capacitance**
  C_{rss} = 0.02 pF typ.
- **high power gain**
  MUG_u = 20 dB typ. for 40600
  MAG = 35 dB typ. for 40602
  MAG_c = 14 dB typ. for 40601

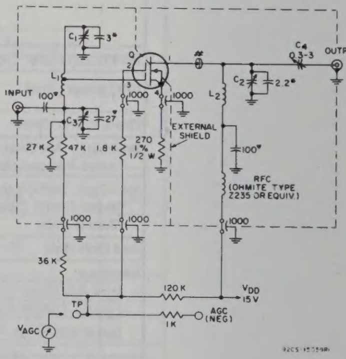
TERMINAL DIAGRAM



Lead 1 — Drain
Lead 2 — Gate No. 2
Lead 3 — Gate No. 1
Lead 4 — Source, Substrate and Case

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . . . . 0 to +20 V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:
  Continuous (dc) . . . . +1 to -8 V
  Peak ac . . . . +20 to -8 V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:
  Continuous (dc) . . . . -8 to 40% of V_{DS} V
  Peak ac . . . . -8 to +20 V
DRAIN-TO-GATE VOLTAGE, V_{DG1} or V_{DG2}. +20 V
DRAIN CURRENT, I_D (Pulsed):
  Pulse duration $\leq$ 20 ms, duty factor $\leq$ 0.15 . . . . 50 mA
TRANSISTOR DISSIPATION, P_T:
  At ambient temperatures up to 25°C . . . . 400 mW
  At ambient temperatures above 25°C . . . . .derate linearly at 2.67 mW/°C
AMBIENT TEMPERATURE RANGE:
  Storage and Operating . . . . -65 to +175 °C
LEAD TEMPERATURE (During soldering):
  At distances $\geq$ 1/32" from seating surface for 10 seconds max. . . . . 265 °C



* Tubular ceramic.

▼ Disk ceramic.

# Ferrite bead (½ used); Indiana General No. H1742C-(A-147) or F1157-1-H, or equivalent.

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13, or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"- 0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200 MHz Power Gain and Noise Figure Test Circuit for 40600 and 40602

For characteristics curves, refer to type 3N140.

40603, 40604

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS

N-Channel Depletion Types
For FM Tuner Applications

RCA 40603 and 40604 are n-channel silicon, depletion type, dual insulated-gate, field-effect transistors utilizing the MOS construction.

These devices have exceptional characteristics for rf-amplifier (40603) and mixer applications (40604) in FM tuners and other commercial equipment operating at frequencies up to approximately 150 MHz. These transistors feature a series arrangement of two separate channels, each channel having an independent control gate. For amplifier applications the 40603 with its wide dynamic range provides substantially better cross-modulation performance and relative freedom from spurious responses than is obtainable with bipolar or single-gate field-effect transistors. The mixing function performed by the 40604 is unique in that the signal applied to gate No.2 is used to modulate the input-gate (gate No.1) transfer characteristic. This technique is superior to conventional "square law" mixing, which can only be accomplished in the non-linear region of the device transfer characteristic.

Because of the low feedback capacitance (0.02 typ. pF) the 40603 can provide a power gain of 25 dB (typ.) at 100 MHz in an unneutralized amplifier circuit.

The gain of the rf stage can be controlled by applying agc voltage to gate No.2. Virtually no agc power is required for full gain reduction.

The 40603 and 40604 are hermetically sealed in JEDEC TO-72 packages.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	0 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-8 to +1	V
Peak ac	-8 to +20	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-8 to 40% of V_{DS}	V
Peak ac	-8 to +20	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} or V_{DG2}	+20	V
DRAIN CURRENT, I_D (Pulsed):		
Pulse duration $\leq$ 20 ms, duty factor $\leq$ 0.15	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	400	mW
At ambient temperatures above 25°C	derate linearly at 2.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances $\geq$ 1/32" from seating surface for 10 seconds max.	265	°C

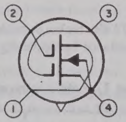
PERFORMANCE FEATURES

- large dynamic range permits large-signal handling before overload
- dual gates allow product mixing with extremely low harmonic generation
- greatly reduces spurious responses in FM receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability
- superior cross-modulation performance and greater dynamic range than bipolar and single-gate field-effect transistors

DEVICE FEATURES

- extremely low feedback capacitance
  C_{rss} = 0.02 pF typ.
- high unneutralized RF power gain
  MUG = 25 dB (typ.) for 40603
- low noise figure
  NF = 2.5 dB typ. for 40603

TERMINAL DIAGRAM



Lead 1 — Drain
Lead 2 — Gate No. 2
Lead 3 — Gate No. 1
Lead 4 — Source, Substrate and Case

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			40603 RF AMPLIFIER		40604 MIXER		
			Typ.	Max.	Typ.	Max.	
Gate No.1-to-Source Cutoff Voltage	$V_{G1S}(off)$	V_{DS} = +15 V, I_D = 200 μA V_{G2S} = +4 V	-2	--	-2	--	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S}(off)$	V_{DS} = +15 V, I_D = 200 μA V_{G1S} = 0	-2	--	-2	--	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20 V, V_{G2S} = 0, V_{DS} = 0	--	1	--	1	nA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20 V, V_{G1S} = 0, V_{DS} = 0	--	1	--	1	nA
Zero-Bias-Voltage Drain Current	I_{DSS}	V_{G2S} = +4 V, V_{G1S} = 0, V_{DS} = +13 V	18	--	18	--	mA
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate-No.1)	C_{rss}	V_{DS} = +13 V, I_D = 10 mA, f = 1 MHz V_{G2S} = +4 V	0.02	0.03	0.02	0.03	pF
Input Capacitance	C_{iss}	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz	5.5	--	5.5	--	pF
Output Capacitance	C_{oss}	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V, f = 100 MHz	2.1	--	2.3	--	pF
Input Resistance	r_{is}	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V, f = 100 MHz	3.5	--	3.5	--	kΩ
Output Resistance	r_{os}	V_{DS} = +13 V I_D = 10 mA V_{G2S} = +4 V f = 100 MHz	4	--	--	--	kΩ
		f = 10.7 MHz	--	--	20	--	kΩ
Forward Transconductance	g_{fs}	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 kHz	10,000	--	2800*	--	μmho
Maximum Available Power Gain	MAG	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V f = 100 MHz, f_{out} for 40604 (mixer) = 10.7 MHz	26	--	21	--	dB
Maximum Usable Power Gain (Unneutralized)	MUG		25▲	-	--	--	dB
Noise Figure	NF		2.5	--	--	--	dB

* conversion transconductance

▲ or limited [illegible] design considerations

For characteristics curves, refer to type 3N140.

40673

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTOR
N-Channel Depletion Type With Integrated Gate-Protection Circuits
For RF Amplifier Applications up to 400 MHz

RCA-40673 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS* pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 40673 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-40673 make it useful for a wide variety of rf-amplifier applications at frequencies up to 400 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two gate arrangement of the 40673 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 40673 is hermetically sealed in the metal JEDEC TO-72 package.

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*Metal-Oxide-Semiconductor.

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +1	V
Peak ac	-6 to +6	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
DRAIN CURRENT, I_D	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥1/32 inch from seating surface for 10 seconds max.	265	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15V, I_D = 200μA V_{G2S} = +4V	–	–2	–4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15V, I_D = 200μA V_{G1S} = 0	–	–2	–4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = +1 or –6 V V_{DS} = 0, V_{G2S} = 0	–	–	50	nA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = ±6V V_{DS} = 0, V_{G1S} = 0	–	–	50	nA
Zero-Bias Drain Current	I_{DSS}	V_{DS} = +15V V_{G2S} = +4V V_{G1S} = 0	5	15	35	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DS} = +15V, I_D = 10mA V_{G2S} = +4V, f = 1kHz	–	12,000	–	μmho
Small-Signal, Short-Circuit Input Capacitance †	C_{iss}	V_{DS} = +15V, I_D = 10mA V_{G2S} = +4V, f=1MHz	–	6	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1) ♦	C_{rss}		0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}		–	2.0	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15V, I_D = 10mA V_{G2S} = +4V, f = 200 MHz	14	18	–	dB
Maximum Available Power Gain	MAG		–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG		–	20*	–	dB
Noise Figure (see Fig. 1)	NF		–	3.5	6.0	dB
Magnitude of Forward Transadmittance	$\lvert Y_{fs} \rvert$		–	12,000	–	μmho
Phase Angle of Forward Transadmittance	θ		–	–35	–	degrees
Input Resistance	r_{iss}		–	1.0	–	k Ω
Output Resistance	r_{oss}		–	2.8	–	k Ω
Protective Diode Knee Voltage	V_{knee}	$I_{DIODE(REVERSE)}$ = ±100μA	–	±10	–	V

*Limited only by practical design considerations.

†Capacitance between Gate No. 1 and all other terminals

♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.

For characteristics curves, refer to type 3N187.

APPLICATIONS

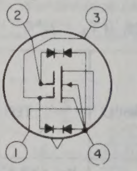
- RF amplifier, mixer, and IF amplifier in military, industrial, and consumer communications equipment
- aircraft and marine vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

PERFORMANCE FEATURES

- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- wide dynamic range permits large-signal handling before overload
- dual-gate permits simplified agc circuitry
- virtually no agc power required
- greatly reduces spurious responses in fm receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability

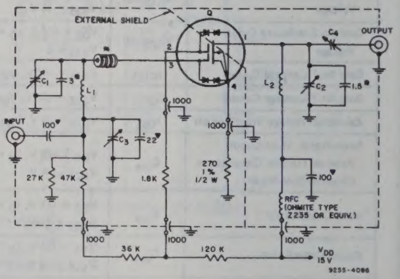
DEVICE FEATURES

- back-to-back diodes protect each gate against handling and in-circuit transients
- low gate leakage currents —— I_{G1SS} & I_{G2SS} = 20 nA(max.) at T_A = 25°C
- high forward transconductance —— g_{fs} = 12,000 μmho (typ.)
- high unneutralized RF power gain —— G_{ps} = 18 dB(typ.) at 200 MHz
- low VHF noise figure —— 3.5 dB(typ.) at 200 MHz



TERMINAL DIAGRAM

LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE



#Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.

Q = 40673

▼ Disc ceramic.

*Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1: 1.8 – 8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.

C_2: 1.5 – 5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4½ turns silver-plated 0.02-in. thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil ≈ .90 in. long.

Fig. 1. 200-MHz Power gain and noise-figure test circuit

40819

Silicon Dual-Insulated-Gate Field-Effect Transistor

N-Channel Depletion Type

With Integrated Gate-Protection Circuits

For RF Amplifier Applications up to 250 MHz

RCA-40819 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor (FET).

The excellent overall performance characteristics of the RCA-40819 make it useful for a wide variety of rf-amplifier applications at frequencies up to 250 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 40819 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac grounding Gate No.2. The reduced capacitance allows operation at maximum gain *without neutralization* and reduces local oscillator feedthrough to the antenna – features of special importance in rf and if amplifiers.

Special back-to-back diodes are diffused directly into the MOS pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts and protect the gates against damage in all normal handling and usage.

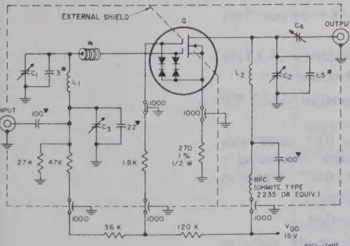
ELECTRICAL CHARACTERISTICS, at T_A = 25° C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 200 μA V_{G2S} = +4 V	–	–2	–4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 200 μA V_{G1S} = 0	–	–2	–4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = ± 6 V V_{DS} = 0, V_{G2S} = 0	–	–	50	nA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = ± 6 V V_{DS} = 0, V_{G1S} = 0	–	–	50	nA
Zero-Bias Drain Current	I_{DSS}	V_{DS} = + 15 V V_{G2S} = +4 V, V_{G1S} = 0	5	15	35	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 kHz	–	12,000	–	μmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz	–	6	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1)♠	C_{rss}		0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}		–	2	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 200 MHz	14	18	–	dB
Maximum Available Power Gain	MAG		–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG		–	20*	–	dB
Noise Figure (see Fig. 1)	NF		–	3.5	6.0	dB
Magnitude of Forward Transadmittance	$\lvert Y_{fs} \rvert$		–	12,000	–	μmho
Phase Angle of Forward Transadmittance	θ		–	–35	–	degrees
Input Resistance	r_{iss}		–	1	–	kΩ
Output Resistance	r_{oss}		–	2.8	–	kΩ
Protective Diode Knee Voltage	V_{knee}	I_{diode} (reverse) = ±100 μA	–	±10	–	V

* Limited only by practical design considerations.

† Capacitance between Gate No.1 and all other terminals.

♠ Three-terminal measurement with Gate No.2 and Source returned to guard terminal.



#Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in OD; 0.03 in ID; 0.063 in thickness.

Q = 40673

▼ Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C1: 1.8 – 8.7 pF variable air capacitor: E. F. Johnson Type 160-104, or equivalent.

C2: 1.5 – 5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L1: 4 turns silver-plated 0.02-in thick, 0.075-0.085 in wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L2: 4-1/2 turns silver-plated 0.02 in thick, 0.085-0.095-in wide, 5/16-in; ID Coil = .90 in long.

Fig. 1. 200 MHz power gain and noise figure test circuit

For characteristics curves, refer to type 3N187.

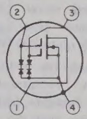
The back-to-back diode configuration permits the 40819 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The 25-volt drain-to-source rating permits the use of higher voltage power supplies.

The 40819 is hermtically sealed in the metal JEDEC TO-72 package.

TERMINAL DIAGRAM

LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE,
SUBSTRATE, AND CASE



Device Features

- back-to-back diodes protect each gate against handling and in-circuit transients
- high forward transconductance: g_{fs} = 12,000 μmho (typ.)
- high unneutralized RF power gain: G_{ps} = 18 dB (typ.) at 200 MHz
- low VHF noise figure: 3.5 dB (typ.) at 200 MHz
- low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA at T_A = 25° C
- increased drain-to-source voltage rating: V_{DS} = –0.2 to +25 V

Performance Features

- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- wide dynamic range permits large-signal handling before overload
- virtually no agc power required
- greatly reduces spurious responses in FM receivers
- dual gate permits simplified AGC circuitry

Applications

- RF amplifier, mixer, and IF amplifier in military, industrial, and consumer communications equipment
- aircraft and marine vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

Absolute Maximum Values, at T_A = 25°C:

Drain-to-Source Voltage, V_{DS}	–0.2 to +25	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+31	V
Drain Current, I_D	50	mA
Transistor Dissipation, P_T:		
At T_A up to 25°C	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C	
Ambient Temperature Range:		
Operating and Storage	–65 to +175	°C
Lead Temperature (During Soldering):		
At distances 1/32 in from seating surface for 10 s max.	265	°C

Maximum Ratings

Continuous Working Voltage#, at T_A = 25°C:

Gate No.1-to-Source Voltage, V_{G1S} . .	–6 to +3	V
Gate No.2-to-Source Voltage, V_{G2S} . .	–6 to +6 or 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+25	V

Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the absolute Maximum Ratings are not exceeded.

40820, 40821

Silicon Dual-Insulated-Gate Field-Effect Transistors

N-Channel Depletion Types

With Integrated Gate-Protection Circuits
For VHF-TV Tuner Applications

40820 – RF Amplifier 40821 – Mixer

Device Features

- **back-to-back diodes protect each gate against handling and in-circuit transients**
- **high forward transconductance: g_{fs} = 12,000 μmho (typ.)**
- **high unneutralized RF power gain: G_{ps} = 17 dB (typ.) at 200 MHz (40820)**
- **low VHF noise figure: 3.5 dB (typ.) at 200 MHz (40820)**
- **low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA**

RCA-40820 and 40821 are n-channel silicon, depletion type, dual-insulated-gate, MOS▲ field-effect transistors for RF amplifier (40820) and mixer (40821) applications in VHF-TV receivers and other commercial equipment operating at frequencies up to 250 MHz.

These devices designed for VHF performance, provide excellent power gain, low-noise figures and have wide dynamic range. The dual-gate feature offers good cross-modulation performance over the AGC range and reduces feedback capacitance by shielding Gate No. 1 from the drain. The very low feedback capacitance also eliminates the need for circuit neutralization and reduces local oscillator feed-through to the antenna.

Virtually no AGC power is required because of the high gate input resistance of the MOS FET types. Automatic AGC delay can be achieved with a very slight change in the input impedance by the application of AGC voltage to Gate No. 2.

Performance Features

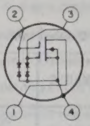
- **superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s**
- **wide dynamic range permits large-signal handling before overload**
- **virtually no agc power required**
- **dual gate permits simplified AGC circuitry**

The dual-gate arrangement also makes it possible to isolate the local oscillator signal from the incoming signal by applying each signal to a separate gate.

Integral back-to-back diodes protect the gates against damage in normal handling and usage by limiting transient voltages that exceed ±10 volts. The 40820 and 40821 are hermetically sealed in metal JEDEC TO-72 packages.

▲ Metal-Oxide-Semiconductor.

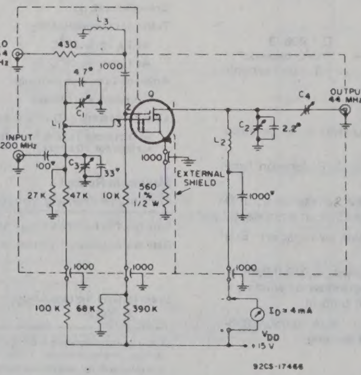
TERMINAL DIAGRAM



LEAD 1 – DRAIN
LEAD 2 – GATE No.2
LEAD 3 – GATE No.1
LEAD 4 – SOURCE, SUBSTRATE, AND CASE

Maximum Ratings	40820	40821	
Continuous Working Voltage#, at T_A = 25°C:			
Gate No. 1-to-Source Voltage, V_{G1S}	–6 to +3	–4.5 to +3	V
Gate No. 2-to-Source Voltage, V_{G2S}	-6 to +6 or 40% of V_{DS} (whichever value is less)	-4.5 to +4.5 or -4.5 to 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	+20	V
Absolute Maximum Values, at T_A = 25°C:			
Drain-to-Source Voltage, V_{DS}	–0.2 to +20	–0.2 to +20	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+26	+24.5	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	–65 to +175	–65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C

Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.



Q = 40821
▼Disc. ceramic.
* Tubular ceramic.
All resistors in ohms
All capacitors in pF

C_1, C_2:	1.5–5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.
C_3:	1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.
C_4:	0.9–7 pF compression-type capacitor: ARCO 400 or equivalent.
L_1:	5 turns silver-plated 0.02" thick, 0.07"–0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.
L_2:	Ohmite Z-235 RF choke or equivalent
L_3:	J. W: Miller Co. #4580 0.1 μH RF choke or equivalent.
Note:	If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

Fig.1 – Conversion power gain test circuit for type 40821.

For characteristics curves, refer to type 3N187.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS 40820 Min.	Typ.	Max.	LIMITS 40821 Min.	Typ.	Max.	UNITS
Gate No. 1 to Source Cutoff Voltage	$V_{G1S(off)}$	$V_{DS} = +15V, I_D = 200\mu A, V_{G2S} = +4V$		–	–1	–3	–	–1	–3	V
Gate No. 2 to Source Cutoff Voltage	$V_{G2S(off)}$	$V_{DS} = +15V, I_D = 200\mu A, V_{G1S} = 0$		–	–1	–3	–	–1	–3	V
Gate-to-Source Forward Breakdown Voltage Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} I_{G2SSF} 100 µA	V_{G2S} V_{DS} 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} V_{DS} 0	–	9	–	–	11	–	V
Gate-to-Source Reverse Breakdown Voltage Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} I_{G2SSR} 100 µA	V_{G2S} V_{DS} 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} V_{DS} 0	–	9	–	–	11	–	V
Gate No. 1 Terminal Forward Current	I_{G1SSF}	V_{DS} V_{G2S} 0	V_{G1S} 6 V	–	–	50		–	–	nA
			V_{G1S} 4.5 V	–	–	–	–	–	50	nA
Gate No. 1 Terminal Reverse Current	I_{G1SSR}	V_{DS} V_{G2S} 0	V_{G1S} 6 V	–	–	50		–	–	nA
			V_{G1S} 4.5 V	–	–	–		–	50	nA
Gate No. 2 Terminal Forward Current	I_{G2SSF}	V_{DS} V_{G1S} 0	V_{G2S} 6 V	–	–	50	–	–	–	nA
			V_{G2S} 4.5 V	–	–	–	–		50	nA
Gate No. 2 Terminal Reverse Current	I_{G2SSR}	V_{DS} V_{G1S} 0	V_{G2S} –6 V		–	50	–	–		nA
			V_{G2S} 4.5 V	–	–	–	–	–	50	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} +15 V, V_{G1S} 0, V_{G2S} +4 V		0.5	8	15	0.5	8	20	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} +15 V I_D 10 mA V_{G2S} +4 V	f 1 kHz	–	12000	–	–	12000	–	µmho
Small Signal, Short Circuit Input Capacitance◆	C_{iss}		f 1 MHz		6	8.5	–	6	9	pF
Small Signal, Short Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1)♠	C_{rss}			0.005	0.02	0.03	0.005	0.02	0.04	pF
Small Signal, Short Circuit Output Capacitance	C_{oss}			–	2	–	–	2	–	pF
Power Gain (see Fig. 6)	G_{PS}			14	17	–	–	–	–	dB
Noise Figure (see Fig. 6)	NF		f 200 MHz	–	4.5	6	–	–	–	dB
Conversion Gain	$G_{PS(C)}$		f 200/44 MHz	–	–	–	11	–	–	dB

◆ Capacitance between Gate No. 1 and all other terminals

♠ Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.

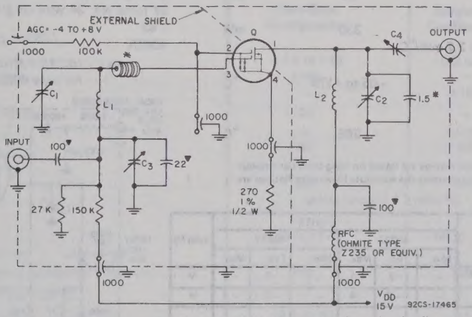


Fig.2 – 200 MHz power gain and noise figure test circuit for type 40820.

*Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in OD; 0.03 in ID, 0.063 in thickness.

Q = 40820

▼ Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1: 1.8 – 8.7 pF variable air capacitor: E. F. Johnson Type 160-104, or equivalent.

C_2: 1.5 – 5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in thick, 0.075-0.085 in wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4-1/2 turns silver-plated 0.02 in thick, 0.085-0.095 in wide, 5/16-in; ID Coil ≈ 0.90 in. long.

Table 1 – y parameters vs. frequency

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz) 50	100	200	250	UNITS
Y Parameters						
Input Conductance	g_{is}	0.08	0.33	1.0	1.6	mmho
Input Susceptance	b_{is}	1.8	3.6	7.5	9.8	mmho
Magnitude Forward Transadmittance	$\|y_{fs}\|$	12	12	12	12.3	mmho
Angle of Forward Transadmittance	$<y_{fs}$	–2	–13	–35	–45	degrees
Output Conductance	g_{os}	0.10	0.18	0.36	0.42	mmho
Output Susceptance	b_{os}	0.5	1.0	2.0	2.6	mmho
Magnitude of Reverse Transadmittance	$\|y_{rs}\|$	8	12	25	40	µmho
Angle of Reverse Transadmittance	$<y_{rs}$	–88	–73	–25	–10	degrees

40822 - 40823

Silicon Dual-Insulated-Gate Field-Effect Transistors

N-Channel Depletion Types

With Integrated Gate-Protection Circuits

For FM Tuner Applications

40822 – RF Amplifier **40823** – Mixer

RCA-40822 and 40823 are n-channel silicon, depletion type, dual-insulated-gate, field-effect transistors for RF amplifier (40822) and mixer (40823) applications in FM receivers and other commercial equipment operating at frequencies up to 150 MHz.

These devices designed for VHF performance, provide excellent power gain, low-noise figures and have wide dynamic range. The dual-gate feature offers good cross-modulation performance over the AGC range and reduces feedback capacitance by shielding Gate No. 1 from the drain. The very low feedback capacitance also eliminates the need for circuit neutralization and reduces local oscillator feed-through to the antenna.

Virtually no power is required in AGC utilizing the 40822 and 40823. In addition, these devices minimize input impedance variations and automatically achieve AGC delay when AGC is applied to Gate No. 2. The dual-gate arrangement also makes it possible to isolate the local oscillator signal from the incoming signal by applying each signal to a specific gate.

Back-to-back diodes, diffused directly into the MOS pellet, protect the gates against damage in normal handling and usage by limiting transient voltages that exceed +10 volts. The 40822 and 40823 are hermetically sealed in metal JEDEC TO-72 packages.

Performance Features

- **superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's**
- **wide dynamic range permits large-signal handling before overload**
- **virtually no agc power required**
- **greatly reduces spurious responses in FM receivers**
- **dual gate permits simplified AGC circuitry**

Device Features

- **back-to-back diodes protect each gate against handling and in-circuit transients**
- **high forward transconductance: g_{fs} = 12,000 μmho (typ.)**
- **high unneutralized RF power gain: G_{ps} = 24 dB (typ.) at 100 MHz (40822)**
- **low VHF noise figure: 2 dB (typ.) at 100 MHz (40822)**
- **low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA at T_A = 25°C**

Maximum Ratings

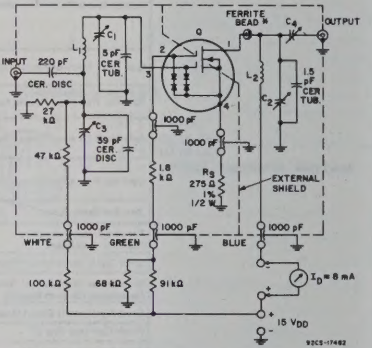
	40822	40823	
Continuous Working Voltage[#], *at T_A = 25°C:*			
Gate No. 1-to-Source Voltage, V_{G1S}	–6 to +3	–4.5 to +3	V
Gate No. 2-to-Source Voltage, V_{G2S}	-6 to +6 or 40% of V_{DS} (whichever value is less)	-4.5 to +4.5 or 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	+20	V
Absolute Maximum Values, at T_A = 25°C:			
Drain-to-Source Voltage, V_{DS}	–0.2 to +18	–0.2 to +18	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+24	+22.5	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	–65 to +175	–65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C

[#] Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS 40822 Min.	40822 Typ.	40822 Max.	LIMITS 40823 Min.	40823 Typ.	40823 Max.	UNITS
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15V, I_D = 200μA, V_{G2S} = +4V		–	–2	–4	–	–2	–4	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15V, I_D = 200μA, V_{G1S} = 0		–	–2	–4	–	–2	–4	V
Gate-to-Source Forward Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	V_{G2S} = V_{DS} = 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} = V_{DS} = 0	–	9	–	–	11	–	V
Gate-to-Source Reverse Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	V_{G2S} = V_{DS} = 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} = V_{DS} = 0	–	9	–	–	11	–	V
Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{DS} = V_{G2S} = 0	V_{G1S} = 6 V	–	–	50	–	–	–	nA
			V_{G1S} = 4.5 V	–	–	–	–	–	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{DS} = V_{G2S} = 0	V_{G1S} = –6 V	–	–	50	–	–	–	nA
			V_{G1S} = –4.5 V	–	–	–	–	–	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{DS} = V_{G1S} = 0	V_{G2S} = 6 V	–	–	50	–	–	–	nA
			V_{G2S} = 4.5 V	–	–	–	–	–	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{DS} = V_{G1S} = 0	V_{G2S} = -6 V	–	–	50	–	–	–	nA
			V_{G2S} = –4.5 V	–	–	–	–	–	50	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V		5	15	30	5	15	35	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V I_D = 10 mA V_{G2S} = +4 V	f = 1 kHz	–	12000	–	–	12000	–	μmho
Small-Signal, Short-Circuit Input Capacitance †	C_{iss}		f = 1 MHz	–	6.5	9.5	–	6.5	10	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♠	C_{rss}			0.005	0.020	0.030	0.005	0.025	0.045	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2	–	–	2	–	pF
Power Gain (see Fig. 5)	G_{PS}		f = 100MHz	19	24	–	–	–	–	dB
Noise Figure (see Fig. 5)	NF			–	2	3.5	–	–	–	dB
Conversion Gain	$G_{PS(C)}$		f = 100 to 10.7MHz	–	–	–	14	18	–	dB

† Capacitance between Gate No. 1 and all other terminals.

♠ Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.



1.3-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

2.7-19.6 pF variable air capacitor: E.F. Johnson Type 160-110 or equivalent.

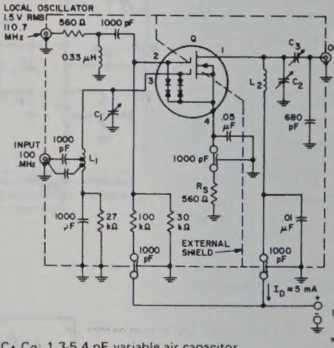
80 pF max. compression-type capacitor: Arco 405 or equivalent

8 turns No. 22 wire on 1/4" diameter air core. One turn spacing between windings. Tapped at one turn from low end.

37 turns No. 34 wire on 3/16" diameter air core. Unloaded Q = 63

40823.

Fig.1 - 100/10.7-MHz conversion power gain test circuit for type 40823.



C_1:

C_2:

C_3:

L_1:

L_2:

Q:

C_1,C_2: 1.3-5.4 pF variable air capacitor

C_3: 1-10 pF variable air capacitor, piston type: Johanson Co., No. 4335

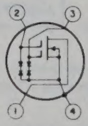
C_4: 1-15 pF variable air capacitor, precision piston type: Roanwell Corp. SG11129/AG

L_1,L_2: 0.22 μH RF choke (7T): Miller, No. 4584

*Ferramic toroid (1/2 used): Indiana General, No. CF101-(0-6)

Fig.2 - 100-MHz power gain and noise figure test circuit for type 40822.

TERMINAL DIAGRAM



LEAD 1 – DRAIN
LEAD 2 – GATE No.2
LEAD 3 – GATE No.1
LEAD 4 – SOURCE, SUBSTRATE AND CASE

For characteristics curves, refer to type 3N187.

Silicon Dual-Insulated Gate Field-Effect Transistor

N-Channel Depletion Type

With Integrated Gate-Protection Circuits

General-Purpose Economy Type for Applications from DC to 500 MHz

RCA-40841 is an n-channel silicon, depletion type, dual-insulated gate, field-effect transistor intended for general-purpose applications from DC to frequencies up to 500 MHz.

This MOS/FET provides excellent power gain, linear-circuit operation and has a wide dynamic operating range. Its square-law characteristics result in low cross-modulation performance over the AGC range. Its dual-gate construction reduces feedback capacitance by shielding Gate No. 1 from the drain, and makes it possible to isolate the local oscillator signal from the incoming signal by applying the two signals to separate gates. The very low feedback capacitance of this device eliminates the need for neutralization in circuits using the dual-gate configuration. Use of the device in the RF input stage of a receiver reduces local oscillator feed-through to the antenna. The 40841 requires negligible AGC power, provides automatic delay when AGC is applied to Gate No. 2, and exhibits slight input impedance variations during AGC functioning. The device has exceptionally high input impedance, an attribute for timing-circuit design.

Back-to-back diodes are fabricated on the same monolithic silicon pellet as the MOS/FET to protect the gates against damage due to electrostatic charges frequently encountered during normal handling. These back-to-back diodes also function as "transient trappers" by limiting in-circuit transient voltages that exceed ±10 volts.

Maximum ratings and electrical characteristics are included in the data for operation of the 40841 as the equivalent of a single-gate device. For single-gate operation, connect Gate No. 1 (Term. 2) to Gate No. 2 (Term. 3), as shown in the Terminal Diagrams on Page 2. The 40841 MOS/FET is hermetically sealed in the metal JEDEC TO-72 package.

Device Features:

- back-to-back diodes protect gate insulation against damage due to static changes frequently encountered during handling
- high forward transconductance: g_{fs} = 12,000 µmho (typ.)
- high power gain: G_{ps} = 32 dB (typ.) at 44 MHz
- gate leakage currents: I_{G1SS} and I_{G2SS} = 60 nA (max.) at T_A = 25°C
- high input impedance
- excellent thermal stability

Performance Features:

- superior cross-modulation performance and greater dynamic range than bipolar and junction-gate FETs
- wide dynamic range permits large-signal handling before overloading
- virtually no agc power required
- greatly reduced spurious responses in AM and FM receivers
- dual-gate configuration permits simplified AGC circuitry
- operates at frequencies to 500 MHz without neutralization in circuits utilizing the dual-gate configuration
- operates up to UHF with low-noise performance

The following dual-gate MOS/FET types are specified for applications requiring premimum-grade performance: 3N200, 3N187, 40673, 40819, 40820, 40821, 40822, and 40823.

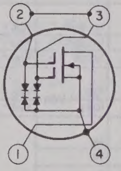
Detailed information, utilizing RCA dual-gate protected MOS/FETs in RF applications, is given in the following RCA Application Notes: AN-4431 "RF Applications of the Dual-Gate MOS/FET up to 500 MHz" and AN-4018 "Design of Gate-Protected MOS Field-Effect Transistors".

Applications:

- DC amplifiers
- RF amplifiers
- mixers
- IF amplifiers
- video amplifiers
- differential amplifiers
- frequency multipliers
- phase splitters
- industrial timers — long time delays
- thyristor trigger circuits
- choppers
- voltage-controlled attenuators
- constant-current source
- voltage regulators
- telemetry & multiplex
- servo amplifiers
- proximity switches

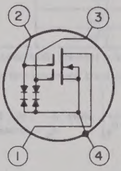
TERMINAL DIAGRAMS

SINGLE-GATE CONFIGURATION



LEAD 1—DRAIN
LEADS—2 AND 3—GATE
LEAD 4—SOURCE, SUBSTRATE AND CASE

DUAL-GATE CONFIGURATION



LEAD 1—DRAIN
LEAD 2—GATE No.2
LEAD 3—GATE No.1
LEAD 4—SOURCE SUBSTRATE AND CASE

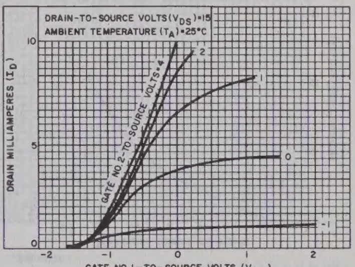


Fig.1—I_D vs. V_{G1S}.

Maximum Ratings

	Dual-Gate Configuration	Single-Gate Configuration	
Absolute Maximum Values, at T_A = 25°C:			
Drain-to-Source Voltage, V_{DS}	–0.2 to +18	–0.2 to +18	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	–	µA
Gate Terminal Current, I_{GS}	–	±100	µA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+24	–	V
Drain-to-Gate Voltage, V_{DG}	–	+24	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	–65 to +175	–65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C
Continuous Working Voltage#, at T_A = 25°C:			
Gate No. 1-to-Source Voltage, V_{G1S}	–4.5 to +3	–	V
Gate No. 2-to-Source Voltage, V_{G2S}	-4.5 to +4.5 or 40% of V_{DS} (whichever value is less)	–	V
Gate-to-Source Voltage, V_{GS}	–	–4.5 to +3	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	–	V
Drain-to-Gate Voltage, V_{DG}	–	+20	V

#Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.

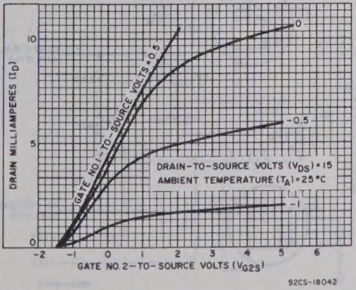


Fig.2—I_D vs. V_{G2S}.

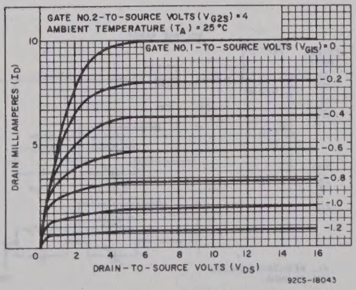


Fig.3—I_D vs. V_{DS}.

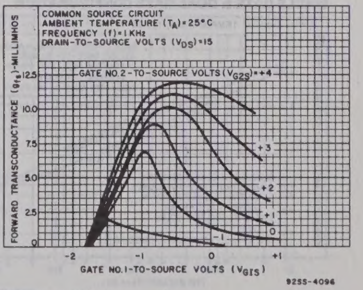


Fig.4—g_{fs} vs. V_{G1S}.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CONFIGURATION DUAL-GATE MIN.	DUAL-GATE TYP.	DUAL-GATE MAX.	SINGLE-GATE MIN.	SINGLE-GATE TYP.	SINGLE-GATE MAX.	UNITS
Gate-to-Source Cutoff Voltage:										
Dual-Gate (No. 1)	$V_{G1S(off)}$	$V_{DS} = +15V, I_D = 200\mu A, V_{G2S} = +4V$		–	–2	–	–	–	–	V
Dual-Gate (No. 2)	$V_{G2S(off)}$	$V_{DS} = +15V, I_D = 200\mu A, V_{G1S} = 0$		–	–2	–	–	–	–	V
Single Gate	$V_{GS(off)}$	$V_{DS} = +15V, I_D = 200\mu A$		–	–	–	–	–1.6	–	V
Gate-to-Source Forward Breakdown Voltage:		$I_{G1SSF} =$								
Dual-Gate (No. 1)	$V_{(BR)G1SSF}$	$I_{G2SSF} =$	$V_{G2S} = V_{DS} = 0$	–	9	–	–	–	–	V
Dual-Gate (No. 2)	$V_{(BR)G2SSF}$	$100\mu A$	$V_{G1S} = V_{DS} = 0$	–	9	–	–	–	–	V
Single-Gate	$V_{(BR)GSSF}$	$I_{GSSF} = 100\mu A, V_{DS} = 0$		–	–	–	–	9	–	V
Gate-to-Source Reverse Breakdown Voltage:		$I_{G1SSR} =$								
Dual-Gate (No. 1)	$V_{(BR)G1SSR}$	$I_{G2SSR} =$	$V_{G2S} = V_{DS} = 0$	–	9	–	–	–	–	V
Dual-Gate (No. 2)	$V_{(BR)G2SSR}$	$100\mu A$	$V_{G1S} = V_{DS} = 0$	–	9	–	–	–	–	V
Single-Gate	$V_{(BR)GSSR}$	$I_{GSSR} = 100\mu A, V_{DS} = 0$		–	–	–	–	9	–	V
Gate Terminal Forward Current:										
Dual-Gate (No. 1)	I_{G1SSF}	$V_{DS} = V_{G2S} = 0, V_{G1S} = 6\ V$		–	–	60	–	–	–	nA
Dual Gate (No. 2)	I_{G2SSF}	$V_{DS} = V_{G1S} = 0, V_{G2S} = 6\ V$		–	–	60	–	–	–	nA
Single-Gate	I_{GSSF}	$V_{DS} = 0, V_{GS} = 6\ V$		–	–	–	–	–	120	nA
Gate Terminal Reverse Current:										
Dual-Gate (No. 1)	I_{G1SSR}	$V_{DS} = V_{G2S} = 0, V_{G1S} = -6\ V$		–	–	60	–	–	–	nA
Dual-Gate (No. 2)	I_{G2SSR}	$V_{DS} = V_{G1S} = 0, V_{G2S} = -6\ V$		–	–	60	–	–	–	nA
Single-Gate	I_{GSSR}	$V_{DS} = 0, V_{GS} = -6\ V$		–	–	–	–	–	120	nA
Zero-Bias Drain Current:										
Dual-Gate	I_{DS}	$V_{DS} = +15\ V, V_{G1S} = 0, V_{G2S} = +4\ V$		–	10	–	–	–	–	mA
Single-Gate	I_{DSS}	$V_{DS} = +15\ V, V_{GS} = 0$		–	–	–	–	3.7	–	mA
Forward Transconductance (Gate-to-Drain)		$V_{DS} = +15\ V$ $I_D = 10\ mA$ [Dual-Gate only $V_{G2S} = +4\ V$]								
Dual-Gate	g_{fs}		1 kHz	–	12000	–	–	–	–	µmho
Single-Gate	g_{fs}			–	–	–	–	7000	–	µmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}		f = 1 MHz	–	6.5	–	–	11	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♣	C_{rss}			–	0.02	–	–	0.54	–	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2	–	–	2	–	pF
Audio Spot Noise Figure*										
Dual-Gate	NF		f = 1 kHz	–	0.46	–	–	–	–	dB
Single-Gate	NF		f = 1 kHz	–	–	–	–	0.29	–	dB
Power Gain	G_{ps}		44 MHz	–	32	–	–	–	–	dB
Conversion Gain	$G_{ps(C)}$			–	24	–	–	–	–	dB

† Capacitance between Gate No. 1 and all other terminals (Dual-Gate), Gate and all other terminals (Single-Gate)

♣ Three-terminal measurement with Gate No. 2 and Source returned to guard terminal (Dual-Gate)

* Noise Figure = $10 \log_{10} \left[1 + \frac{e_n^2}{4\ KT\ BW\ R_g} \right]$ where $K = 1.38 \times 10^{-23}$; T = Temperature in °Kelvin; BW = Bandwidth in Hz; R_g = Generator resistance

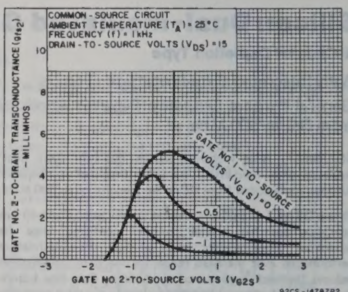


Fig.5–g_{fs2} vs. V_{G2S}.

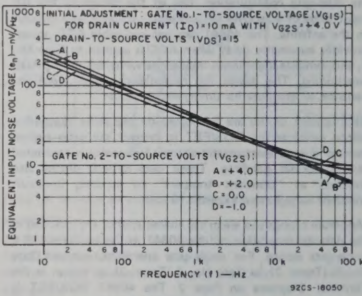


Fig.6–e_n vs. f.

TYPICAL CHARACTERISTICS FOR 40841 IN SINGLE-GATE CONFIGURATION
(Terminals 2 and 3 tied together to comprise effective single-gate)

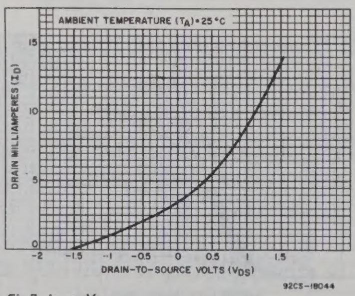


Fig.7–I_D vs. V_{DS}.

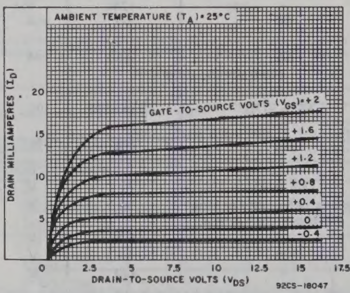


Fig.8–I_D vs. V_{DS}.

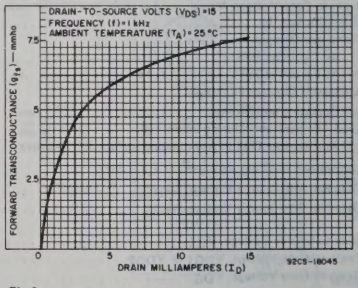


Fig.9–g_{fs} vs. I_D.

TYPICAL CHARACTERISTICS FOR 40841 IN SINGLE-GATE & DUAL-GATE CONFIGURATION

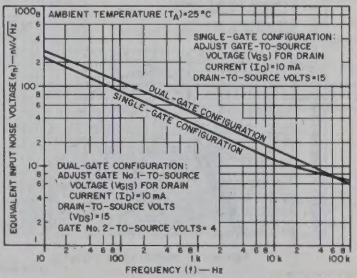


Fig.10–e_n vs. f.

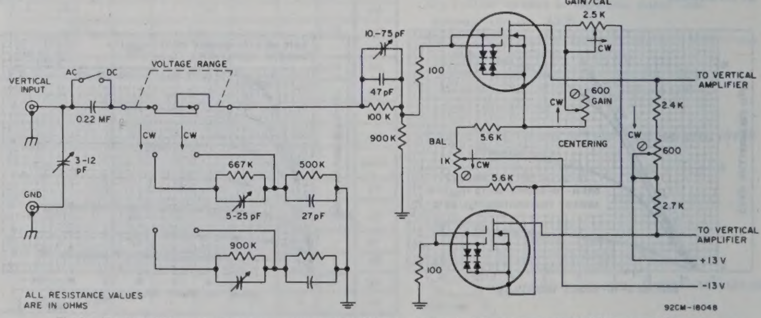
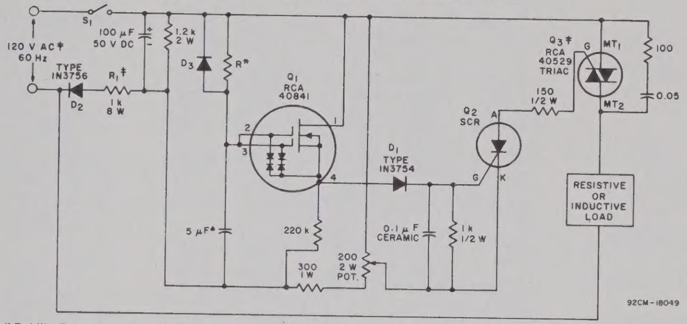


Fig.11–Typical differential amplifier utilizing the 40841 in the vertical input stage of a solid-state oscilloscope.

SOLID-STATE TIMER FOR INDUSTRIAL APPLICATIONS



▲ Cornell-Dubilier Electronics—Type MMW or equivalent.

• R controls duration of time delay. At R = 60 MΩ up to 5-minute delay (IRC resistor, Type CGH or equivalent)

‡ This circuit can also be used at supply voltages of 240 V AC and 24V AC (60Hz) by changing the values of R1 and Q3.

TIMING CIRCUIT CHARACTERISTICS

$T_A = -25^{\circ}C$ to $+60^{\circ}C$

Accuracy: ±10% (over temperature)

Repeatability: ±3% (at 25°C)

Reset Time: Less than 150 ms

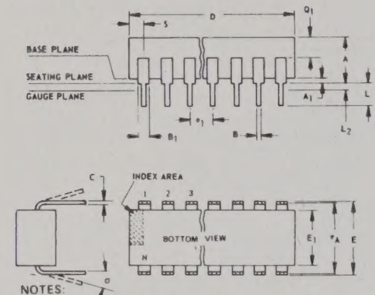
Q2: $V_{DRM} = 60V$
$I_{GT} = 200\mu A$
$I_T = 0.8A$

D3: $I_R = 1nA$
$V_R = 60V$

Fig.12—Typical timing circuit utilizing the 40841 in a single-gate configuration.

Dimensional Outlines

Dimensional Outlines



NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

CERAMIC DUAL-IN-LINE PACKAGES

(D) Suffix (JEDEC MO-001-AD) 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-4411R2

(D) Suffix (JEDEC MO-001-AE) 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R5

DUAL-IN-LINE PLASTIC AND FRIT-SEAL CERAMIC PACKAGES

(E) and (G) Suffixes (JEDEC MO-001-AN) 8-Lead Plastic (Mini-DIP)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.889	1.65
C	0.008	0.012	1	0.203	0.304
D	0.370	0.400		9.40	10.16
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.762
α	0	15	4	0	15
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.381	1.52

92CS-24026RI

(E, (F) and (G) Suffixes (JEDEC MO-001-AB) 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

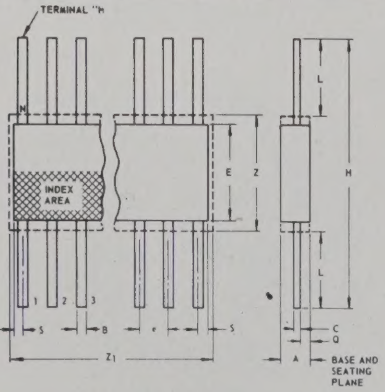
92SS-4296R3

(E), (F), and (G) Suffixes (JEDEC MO-001-AC) 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R4

CERAMIC FLAT PACKS



NOTES:
1. Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

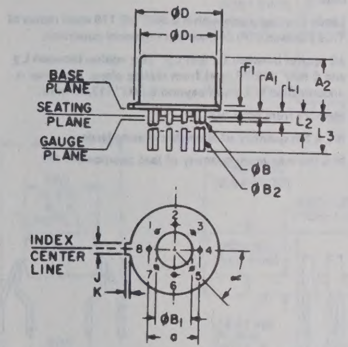
(K) Suffix (JEDEC MO-004-AF) 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0 381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS 4300R3

TO–5 STYLE PACKAGES

(T) Suffix (JEDEC MO-002-AL) 8-Lead TO-5 Style



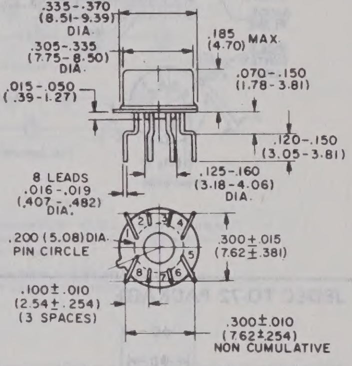
92CS-19431R2

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.200 TP		2	5.88 TP	
A_1	0.010	0.050		0.26	1.27
A_2	0.165	0.185		4.20	4.69
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0.125	0.160		3.18	4.06
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	45° TP			45° TP	
N	8		6	8	
N_1	3		5	3	

NOTES

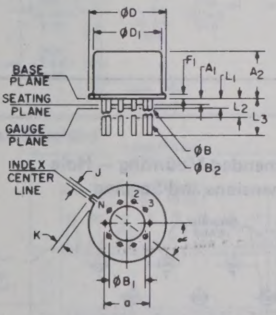
1. Refer to JEDEC Publication No 95 for Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2.ϕB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

(S) Suffix 8-Lead TO-5 Style with Dual-In-Line Formed Leads (DIL-CAN)



92CS-20296R3

(T) Suffix (JEDEC MO-006-AF) 10-Lead TO-5 Style



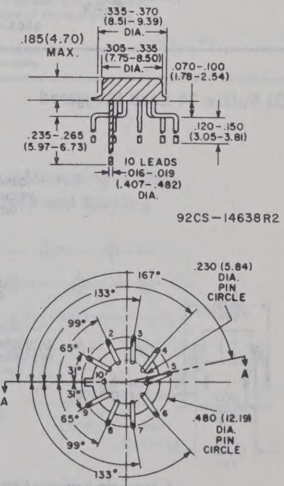
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230 TP		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0	0		0	0
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	36° TP			36° TP	
N	10		6	10	
N_1	1		5	1	

NOTES:

1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

92CS-15835

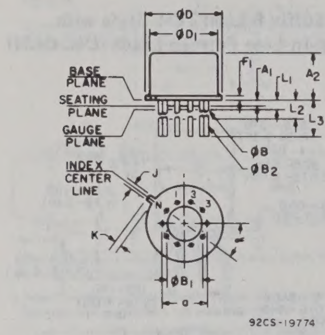
(V) Suffix
10 Formed Leads Radially Arranged TO-5 Type



Dimensional Outlines

TO–5 STYLE PACKAGE (Cont'd)

(T) Suffix(JEDEC MO-006-AG)12-Lead TO-5 Style

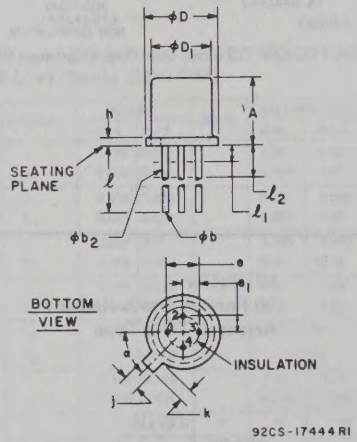


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0	0		0	0
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	30° TP			30 TP	
N	12		6	12	
N_1	1		5	1	

NOTES:

1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

JEDEC TO-72 PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.210	4.32	5.33	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e_1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1 (Four leads) Maximum number leads omitted in this outline, "none" (0) The number and position of leads actually present are indicated in the product registration Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads

Note 2 (All leads) ϕb_2 applies between l_1 and l_2 ϕb applies between l_2 and 500" (12 70 mm) from seating plane Diameter is uncontrolled in l_1 and beyond 500" (12 70 mm) from seating plane

Note 3 Measured from maximum diameter of the product

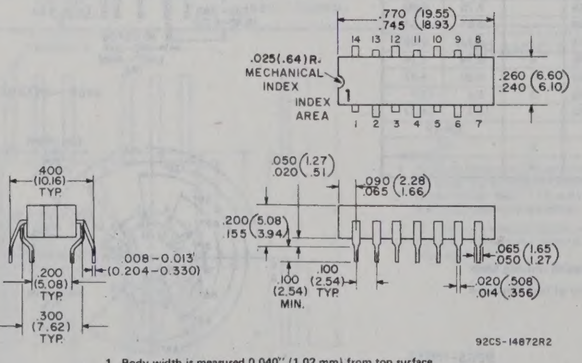
Note 4 Leads having maximum diameter 019" (483 mm) measured in gaging plane 054" (1 37 mm) + 001" (025 mm), - 000" (000 mm) below the seating plane of the product shall be within 007" (178 mm) of their true position relative to a maximum width tab

Note 5 The product may be measured by direct methods or by gage

Note 6: Tab centerline

QUAD-IN-LINE PLASTIC PACKAGES

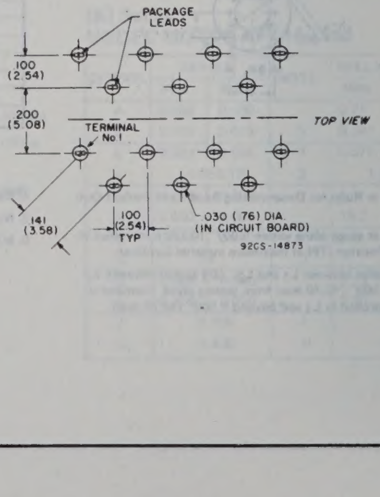
(Q) Suffix 14-Lead Staggered



1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

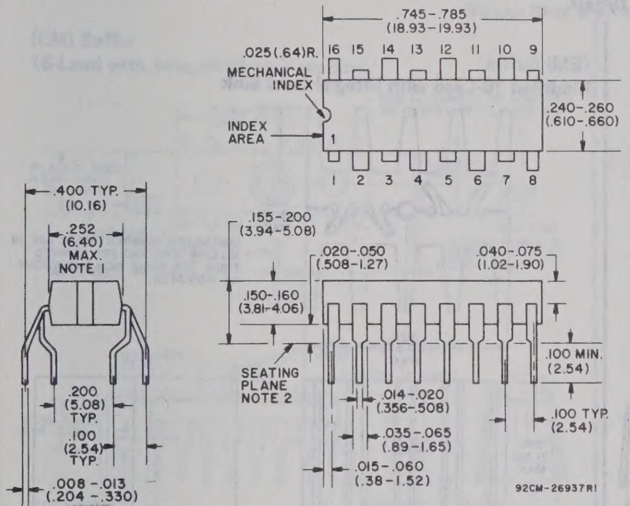
Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

Recommended Mounting – Hole Dimensions and Spacing

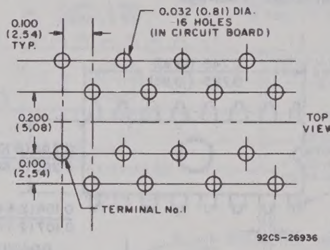


QUAD IN-LINE PACKAGES (Cont'd)

(W) Suffix 16-Lead Staggered



Recommended Mounting – Hole Dimensions and Spacing

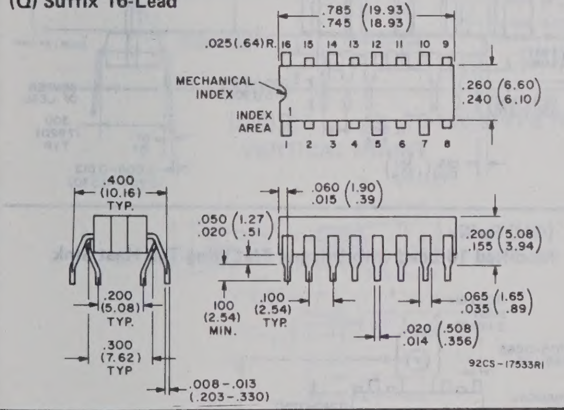


NOTES:

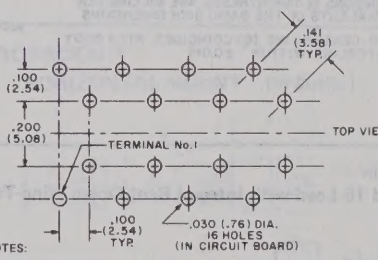
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

(Q) Suffix 16-Lead



Recommended Mounting – Hole Dimensions and Spacing



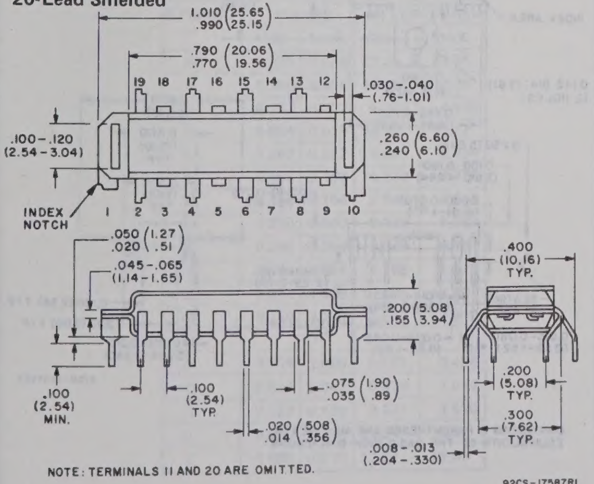
NOTES:

1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

92CS-17580

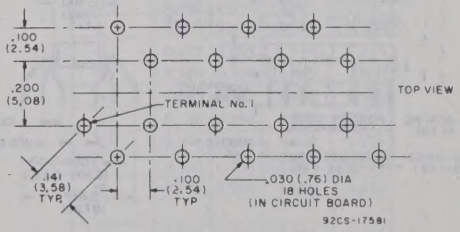
20-Lead Shielded



NOTE: TERMINALS 11 AND 20 ARE OMITTED.

92CS-17587R1

Recommended Mounting – Hole Dimensions and Spacing



NOTES:

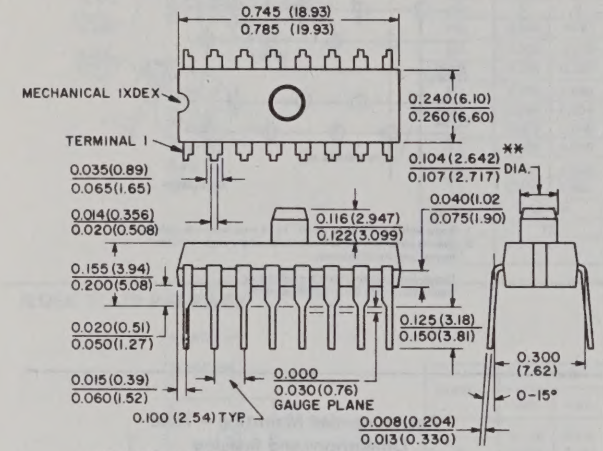
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

Dimensional Outlines

DUAL-IN-LINE AND QUAD-IN-LINE PLASTIC PACKAGES
(Power Stud and Heat-Sink Types)

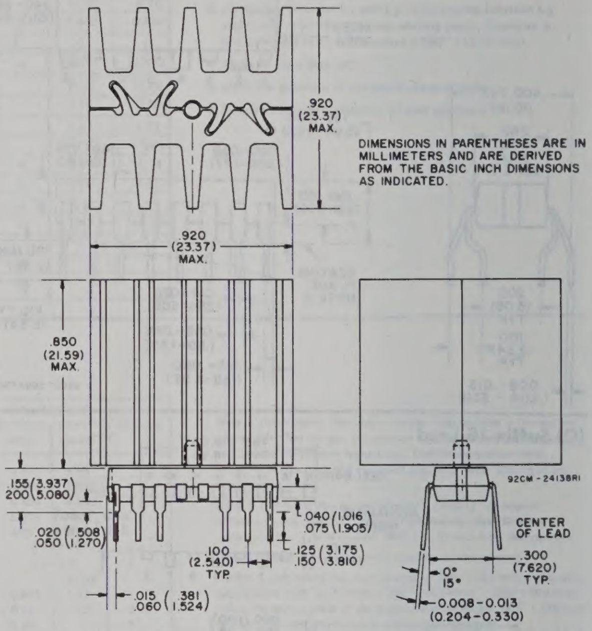
(E) Suffix
16-Lead "Power-Stud" Package



DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS OF THE BASIC INCH DIMENSIONS

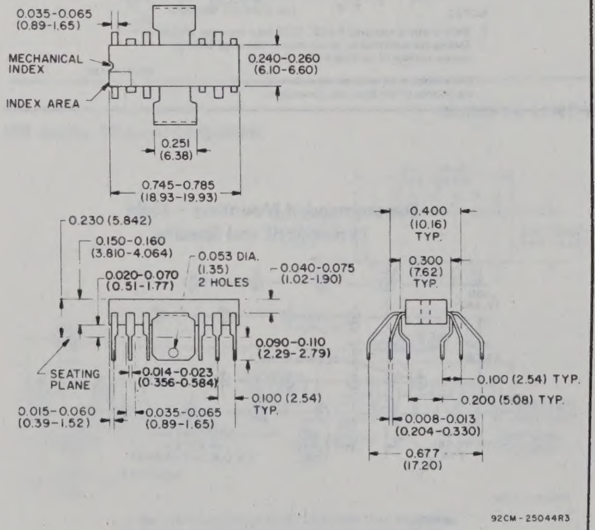
** STUD CENTERLINE (℄) COINCIDES WITH BODY CENTERLINE WITHIN ±0.015

(EM) Suffix
Modified 16-Lead with Integral Heat Sink



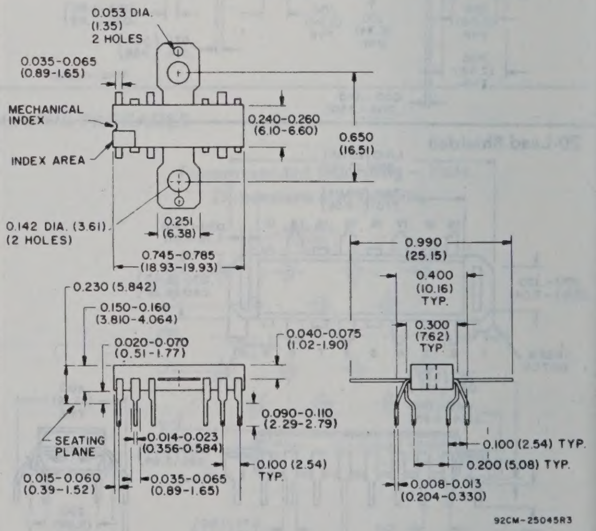
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS AND ARE DERIVED FROM THE BASIC INCH DIMENSIONS AS INDICATED.

(Q) Suffix
Modified 16-Lead with Integral Bent Down Wing-Tab Heat Sink



DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS OF THE BASIC INCH DIMENSIONS

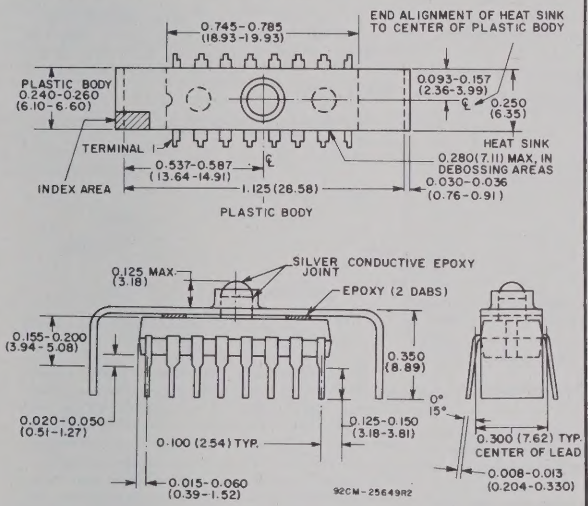
(QM) Suffix
Modified 16-Lead with Integral Flat Wing-Tab Heat Sink



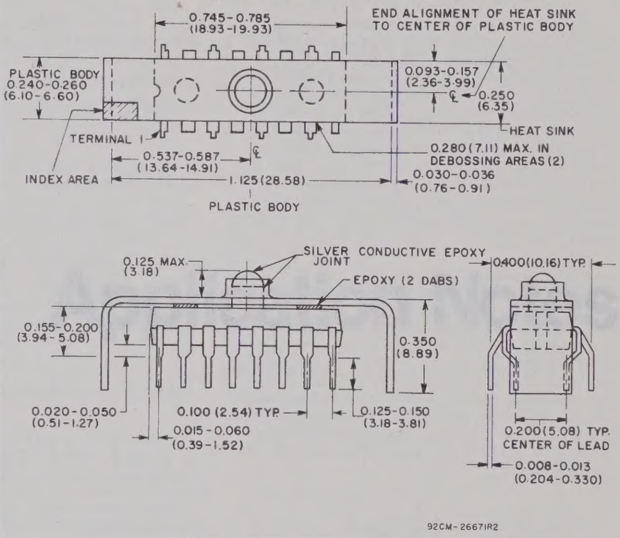
DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS OF THE BASIC INCH DIMENSIONS

DUAL-IN-LINE AND QUAD-IN-LINE PLASTIC PACKAGES
(Power Stud and Heat-Sink Types)

(EM) Suffix
16-Lead with Integral Strap Heat Sink

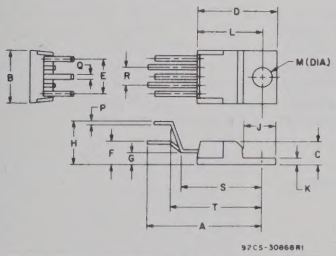


(QM) Suffix
16-Lead Staggered with Integral Strap Heat Sink



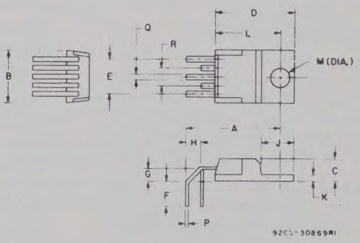
TO-220-STYLE (VERSA-V) PLASTIC PACKAGE

VERTICAL MOUNT

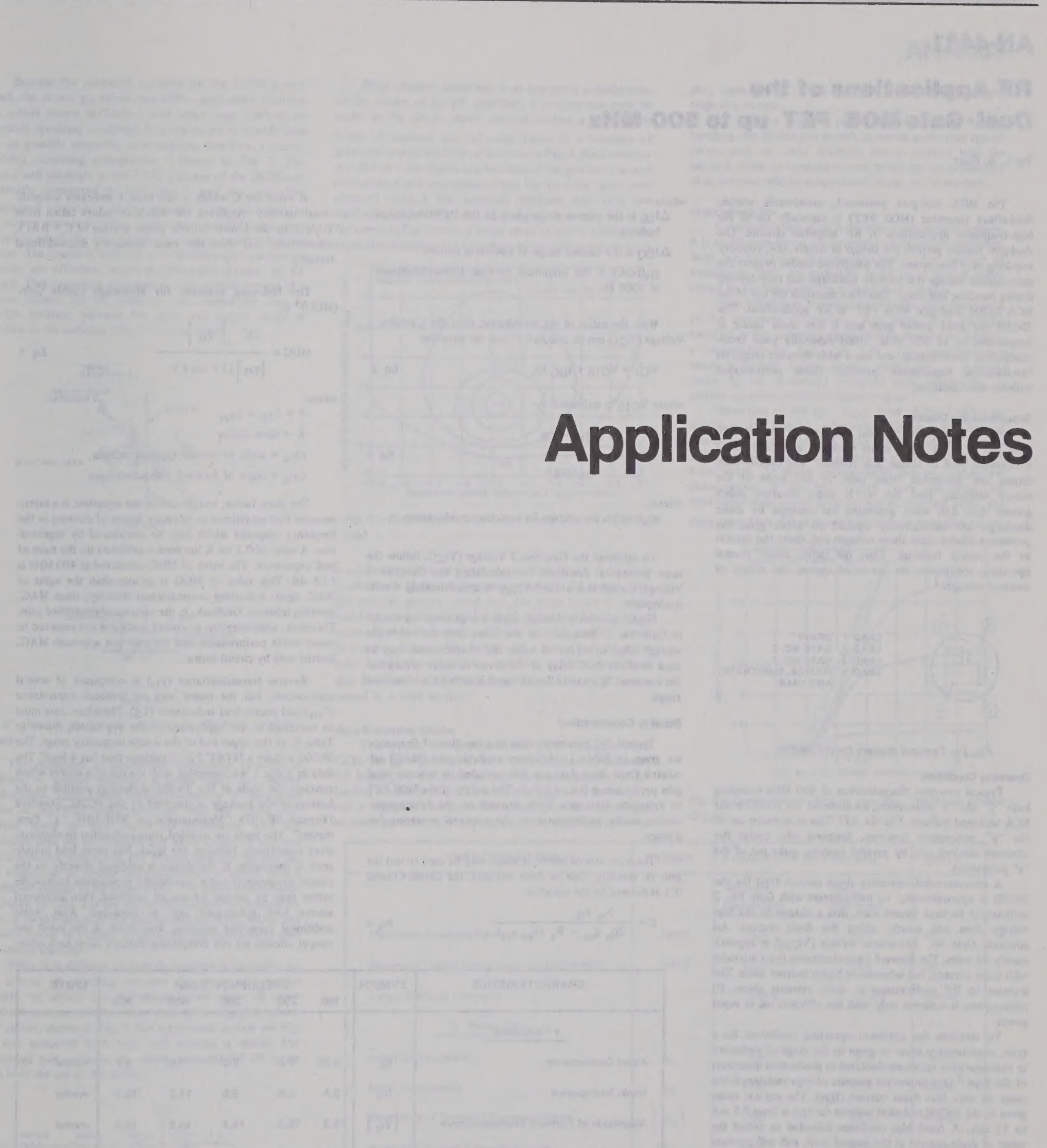


SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.876	0.896	22.25	22.75
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.168	0.188	4.268	4.775
G	0.100	0.104	2.540	2.641
H	0.320	0.340	8.128	8.638
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530
S	0.600	0.630	15.24	16.00
T	0.680	0.710	17.27	18.03

HORIZONTAL MOUNT (M Suffix)



SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.726	0.746	18.44	18.94
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.221	0.251	5.614	6.375
G	0.100	0.104	2.540	2.641
H	0.143	0.163	3.633	4.140
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530



Application Notes

AN-4431

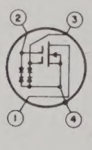
RF Applications of the Dual-Gate MOS FET up to 500 MHz

by L. S. Baar

The RCA dual-gate protected, metal-oxide silicon, field-effect transistor (MOS FET) is especially useful for high-frequency applications in RF amplifier circuits. The dual-gate feature permits the design of simple AGC circuitry requiring very low power. The integrated diodes protect the gates against damage due to static discharge that may develop during handling and usage. This Note describes the use of the RCA-3N200 dual-gate MOS FET in RF applications. The 3N200 has good power gain and a low noise factor at frequencies up to 500 MHz, offers especially good cross-modulation performance, and has a wide dynamic range; its low-feedback capacitance provides stable performance without neutralization.

Gate-Protection Diodes

Fig. 1 shows the terminal diagram for the 3N200. Gate No. 1 is the input signal electrode and Gate No. 2 is normally used to obtain gain control. The back-to-back diodes are connected from each of the gates to the source terminal, lead No. 4. If short duration pulses greater than ±10 volts, generated for example by static discharge, are inadvertently applied to either gate, the protective diodes limit these voltages and shunt the current to the source terminal. Thus the gates, under normal operating conditions, are protected against the effects of overload voltages.[1]



LEAD 1 - DRAIN
LEAD 2 - GATE NO. 2
LEAD 3 - GATE NO. 1
LEAD 4 - SOURCE, SUBSTRATE, AND CASE

Fig. 1 – Terminal diagram for the 3N200.

Operating Conditions

Typical two-port characteristics at 400 MHz including both "y" and "s" parameters, are given for the 3N200 in the RCA technical bulletin, File No. 437. This note makes use of the "y" parameters; however, designers who prefer the alternate method can, by parallel analysis, make use of the "s" parameters.

A recommended operating drain current (I_D) for the 3N200 is approximately 10 milliamperes with Gate No. 2 sufficiently forward biased such that a change in the bias voltage does not greatly affect the drain current. An adequate Gate No. 2-to-source voltage (V_{G2S}) is approximately +4 volts. The forward transadmittance (y_{fs}) increases with drain current, but saturates at higher current levels. The increase in RF performance at drain currents above 10 milliamperes is achieved only with less efficient use of input power.

To establish the optimum operating conditions for a type, consideration must be given to the range of variations in characteristics values encountered in production quantities of the type.[2] One important measure of type variation is the range of zero bias drain current (I_{DS}). The current range given in the 3N200 technical bulletin for I_{DS} is from 0.5 mA to 12 mA. A fixed bias condition intended to center the range of drain current at the desired level, still will produce an operating drain current range of 11.5 milliamperes with a resultant wide range of forward transconductance (g_{fs}). The drain current can be regulated by applying dc feedback with a bypassed source resistor (R_S). A good approximation of R_S (where $I_{DQ} \geq I_{DS}/2$) can be calculated by the use of the following formula*, assuming that V_{G1S} vs. I_{DS} is linear over the current range under consideration:

$$R_S \approx \left(\frac{1}{g_{fs}(\text{min.})}\right)\left(\frac{\Delta I_{DS}}{\Delta I_{DQ}} - 1\right) \qquad \text{Eq. 1}$$

where:

ΔI_{DS} is the current range given in the 3N200 technical bulletin

ΔI_{DQ} is the desired range of operating current

$g_{fs}(\text{min.})$ is the minimum forward transconductance at 1000 Hz

With the value of R_S established, then the Gate-No. 1 Voltage (V_{G1}) can be calculated from the equation

$$V_{G1} = V_{G1S} + I_{DQ} R_S \qquad \text{Eq. 2}$$

where V_{G1S} is estimated by:

$$V_{G1S} \approx \frac{I_{DQ} - I_{DS}}{g_{fs}(\text{avg.})} \qquad \text{Eq. 3}$$

where:

$g_{fs}(\text{avg.})$ is the average forward transconductance

To establish the Gate-No. 2 Voltage (V_{G2}), follow the same procedure described for calculating the Gate-No. 1 Voltage, except that a fixed V_{G2S} of approximately 4 volts is adequate.

If gain control is desired, apply a negative-going voltage to Gate No. 2. Because Gate No. 2 has little control in the voltage range of +2 to +5 volts, this characteristic may be used to effect AGC delay of the device in order to maintain the low noise figure until the RF signal is out of the noise-level range.

Stability Considerations

Typical "y" parameter data as a function of frequency are given in Table 1. Maximum available gain (MAG) calculated from these data are also included to indicate ideal gain performance (i.e., $y_{rs} = 0$). The ability of the MOS FET to approach these gain levels depends on the device maintaining stable performance at the required operating frequency.

There are several methods which may be used to test for gain vs. stability. One of these methods, the Linvill Criteria (C), is defined by the equation:

$$C = \frac{y_{rs}\, y_{fs}}{2g_{is}\, g_{os} - R_e\,(y_{rs}\, y_{fs})} \qquad \text{Eq. 4}$$

A value for C which is less than 1 indicates unconditional stability. Applying the 400-MHz values taken from Table 1 to the Linvill Criteria yields a value of C = 0.615; substantially less than the value indicating unconditional stability.

The following equation for Maximum Usable Gain (MUG)[3] is:

$$\text{MUG} = \frac{2K\,|y_{fs}|}{|y_{rs}|\,(1 + \cos\theta)} \qquad \text{Eq. 5}$$

where:

$\theta = \angle y_{fs} + \angle y_{rs}$

K = skew factor

$\angle y_{rs}$ = angle of reverse transadmittance

$\angle y_{fs}$ = angle of forward transadmittance

The skew factor, introduced in this equation, is a safety measure that establishes an arbitrary degree of skewing in the frequency response which may be introduced by regeneration. A value of 0.2 for K has been established on the basis of past experience. The value of MUG calculated at 400 MHz is 13.8 dB. This value of MUG is greater than the value of MAG, again indicating unconditional stability, since MAG, ignoring inherent feedback, is the conjugately matched gain. Therefore, neutralization or circuit loading is not required to insure stable performance, and the gain can approach MAG, limited only by circuit losses.

Reverse transadmittance (y_{rs}) is composed of several components, but the major ones are feedback capacitance (C_{rss}) and source-lead inductance (L_S). Therefore, care must be exercised in the application of the y_{rs} values, shown in Table 1, at the upper end of the usable frequency range. The 3N200 utilizes a JEDEC TO-72 package that has 4 leads. The data in Table 1 was compiled with the use of a socket which contacts the leads of the 3N200 as close as possible to the bottom of the package as specified by the JEDEC Standard Proposal SP-1028 "Measurement of VHF-UHF "y" Parameters". The leads are shielded from each other to eliminate stray capacitance between the leads, but some lead inductance is inevitable. If the device is soldered directly to the circuit components using commercial production techniques rather than by precise laboratory methods, then additional source lead inductance can be expected. Also, some additional capacitive coupling may result if the input and output circuits are not completely isolated from each other.

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz) 100	200	300	400	500	UNITS
y Parameters							
Input Conductance	g_{is}	0.25	0.8	2.0	3.6	6.2	mmho
Input Susceptance	b_{is}	3.4	5.8	8.5	11.2	15.5	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs}\rvert$	15.3	15.3	15.4	15.5	16.3	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	-15.0	-25.0	-35.0	-47.0	-60.0	degrees
Output Conductance	g_{os}	0.15	0.3	0.5	0.8	1.1	mmho
Output Susceptance	b_{os}	1.5	2.7	3.6	4.25	5.4	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs}\rvert$	0.012	0.025	0.06	0.14	0.26	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	-60.0	-25.0	0	14.0	20.0	degrees
Maximum Available Gain	MAG	32.0	24.0	17.5	13	10.0	dB

Table 1 – "y" Parameters from 100 to 500 MHz

*See Appendix

Because the published y_{rs} value for the 3N200 is very small, the circuit y_{rs} values may differ significantly from the y_{rs} values shown in Table 1 and hence, may result in an unstable operating condition. It is impossible to provide data for all possible mounting combinations, therefore, a recommended mounting arrangement is shown in Fig. 2. The source and substrate in the T0-72 package of the 3N200 are internally connected to lead No. 4 and the case. The source-lead inductance can be reduced, if the case is used as the source connection. Fig. 2 illustrates a partial component layout in which the case is held by a clamp or other fingered device. The clamp is soldered to a feedthrough capacitor to provide an effective, very-low inductance bypass to RF signals. This mounting arrangement still permits the use of a source resistor for DC stability, and enables the case to provide isolation between the input and output circuit in addition to the isolation afforded by the shield.

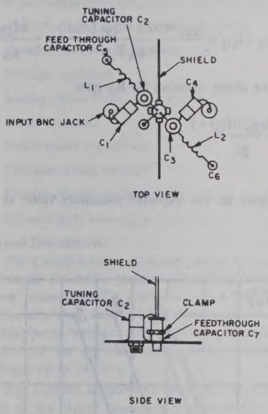


Fig. 2 – Partial component layout of 400-MHz amplifier circuit

The reduction of source-lead inductance provides in addition to greater stability, a lower input and output conductance. Table 2 shows the differences in "y" parameter values at 400 MHz when measured with the source connection made to lead No. 4 (in accordance with the published data for the 3N200) and when measured with the case connected directly to the ground plane of the test jig. The magnitude of reverse transadmittance is halved with a significant change in its phase angle. The input conductance is reduced by 30%, and the output conductance is reduced by 13%. A recalculation of the expressions for MAG, MUG, and Linvill Criteria (C) shows a significant improvement in gain and circuit stability.

While it is difficult to provide accurate information on the effects of shielding between the input and output circuits, its effect can be demonstrated when all other feedback components have been reduced to negligible values. The circuit, shown in Fig. 3 (for component layout see Fig. 2), was measured both with and without a shield. The maximum gain, without the shield, averaged 0.8 dB lower than with the use of the shield.

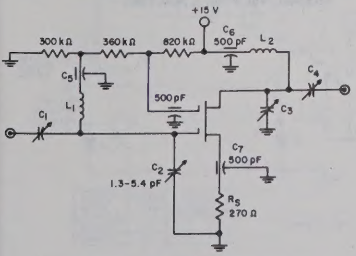


Fig. 3 – 400-MHz amplifier circuit

When receiver sensitivity is an important consideration in the design of an RF amplifier, a compromise must be made in the circuit power gain to achieve a lower noise factor. A contour plot of noise figure as a function of generator source admittance is shown in Fig. 4. Each contour is a plot of noise figure as a function of the generator source conductance and susceptance. Data for the noise figure were obtained from a test amplifier designed with very low feedback. Even though the area of very low-noise figure in the curves in Fig. 4 cover a broad range of source admittance, impedance-matching for maximum power gain could result in a relatively poor noise figure. As shown in Table 2, the input conductance (g_{is}) with the case grounded is 2.5 mmho. With the reactive portion tuned out, the noise factor at power matched conditions is almost 1 dB higher than the optimum noise figure. However, matching to 5.0 mmho results in a near optimum noise factor with a loss of only 0.5 dB in gain. In addition, impedance matching to high conductance also benefits crossmodulation performance, as will be discussed in a later section.

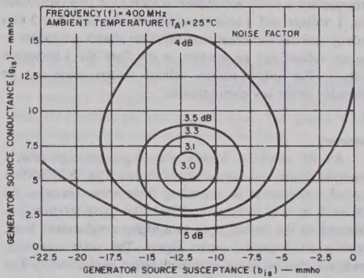


Fig. 4 – Noise factor vs. generator source (input) admittance (y_{is})

Gate Protection Diodes

The diodes incorporated into RCA dual-gate MOS FETs, for gate protection, have been designed to minimize RF loading on the input circuits. The small amount of RF loading results in only a fraction of a dB loss in power gain and a negligible increase in the noise figure. The advantages of diode protection, greatly outweigh the slight loss in power gain, especially in an RF amplifier intended for the input stage of a receiver.

In addition to the protection afforded in normal handling, the diodes also provide in-circuit protection against events such as: static discharge due to contact with the antenna, delay in transmit-receive switching, or connection of an antenna with an accumulated charge to the receiver.

Crossmodulation

Crossmodulation is an important consideration because it is an inherent device characteristic where circuit considerations are secondary. Crossmodulation is the transfer of modulation from an undesired signal on a desired signal caused by the non-linear characteristics of a device.

Crossmodulation is proportional to the third-order term of the expansion of the I_D - V_{GS} curve. It is normally specified as the undesired signal voltage required to produce a crossmodulation factor of 0.01. The crossmodulation factor is defined as the percent modulation on a desired carrier by the modulated undesired signal divided by the percent modulation of the undesired signal.[4]

Inspection of the I_D - V_{G1S} curve of Fig. 5 offers an insight to the possible crossmodulation as a function of gain-reduction performance. When both channels of the 3N200 are fully conducting current, as shown by the V_{G2S} = 4-volt curve, the device approximately follows a square-law characteristic. If the I_D - V_{G1S} curve was ideal, the third-order term would be zero; but in practical cases, the third-order term and crossmodulation have some low values.

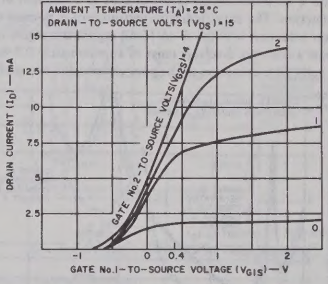


Fig. 5 – Drain current (I_D) vs. gate No. 1-to-source voltage (V_{G1S})

CHARACTERISTICS	SYMBOL	FREQUENCY (f) = 400 MHz		UNITS
		Normal Connection	Case Grounded	
Maximum Available Power Gain	MAG	13.0	15.7	dB
Maximum Usable Power Gain (unneutralized)	MUG	13.8	19.4	dB
Linvill Stability Factor, C	C	0.615	0.335	mmho
"y" Parameters				
Input Conductance	g_{is}	3.6	2.5	mmho
Input Susceptance	b_{is}	11.2	11.7	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	15.5	15.5	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	-47.0	-40.0	degrees
Output Conductance	g_{os}	0.8	0.65	mmho
Output Susceptance	b_{os}	4.25	4.25	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs} \rvert$	0.14	0.07	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	14.0	49.0	degrees

Table 2 – "y" Parameters at 400 MHz with source connection to lead No. 4 and with case connected to ground plane of test jig

When the gain is reduced, by the application of bias to Gate No. 2, the square-law characteristic changes to a curve with a knee. Sharp curvatures usually result in larger high-order terms and poorer crossmodulation performance can be expected at lower gain conditions. If in Fig. 6, Circuit A, we assume a fixed bias (V_{G1S}) of approximately +0.4 volt, then the expected variation in crossmodulation is determined at the points where the ordinate at $V_{G1S} = +0.4$ volt crosses the curves. Crossmodulation performance at values of $V_{G2S} = +4$ volts to cutoff is as follows: good (low crossmodulation) at +4 volts, poorer at +2 volts, poorest at +1 volt, and again improves from zero volts to cutoff.

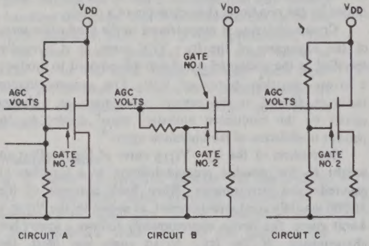


Fig. 6 – Biasing circuits using the 3N200

Curve A, Fig. 7 shows a curve of the undesired signal with a crossmodulation factor of 0.01 as a function of gain reduction. The curve indicates performance is poorest when gain reduction is in the 3- to 15-dB region; this region represents a Gate No. 2-voltage range of approximately 0.5 volt to 2 volts. The exception to the poor crossmodulation performance in this range is the sharp peak which occurs at the 5-dB level and is due to a curve inversion that takes place just prior to the knee. Beyond the 15-dB level, crossmodulation generally shows an improvement.

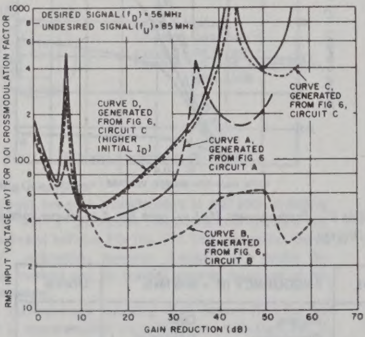


Fig. 7 – Crossmodulation vs. gain reduction using biasing circuits shown in Fig. 6

If Gate No. 1 is also reverse biased in conjunction with Gate No. 2 in the manner shown in Fig. 6, Circuit B, then the overall performance is poorer because the Gate No. 1 voltage will tend to follow the knee of each curve. This occurrence is evident in Fig. 7, Curve B. If Gate No. 1 is biased as shown in Fig. 6, Circuit C, the Gate No. 1-to-Source voltage intercepts the Gate No. 2 curves where the curvature is less severe, indicating as shown by Fig. 7, Curve C an improvement in crossmodulation performance. A further slight improvement is possible by the use of a higher initial operating drain current, which effectively moves the intercepts to the right on each curve. This improvement is indicated in Fig. 7, Curve D.

The curves in Fig. 7 establish that the biasing arrangement which provides optimum crossmodulation performance is the one in which Gate No. 1 forward bias increases as Gate No. 2 controls the gain. This biasing arrangement is easily accomplished by the use of a fixed Gate No. 1 voltage and a source resistor. As the Gate No. 2 bias voltage reduces the drain current, there is also a decrease in source voltage and an increase in the Gate No. 1-to-Source voltage. The gate-to-source voltage ratings must not be exceeded under any circumstances.

Summary

An RF amplifier, ideally, should provide high gain, a low-noise figure, and low crossmodulation. The 3N200 offers a good compromise in providing these three features. As indicated in the section on "Stability Considerations" a mismatch at the circuit input to a higher conductance level, provides an improved noise figure. The same mismatch condition also improves crossmodulation performance. The input signal at the gate of the device, when mismatched as indicated above, is lower than if it is power matched. The same ratio applies to any undesired signal and, thus, reduces the possibility of crossmodulation interference.

Appendix

The drain current of a device is established by the relationship

$$I_D = g_{fs} V_{G1S} + I_{DS}$$

where:

I_{DS} = drain current

at:

$V_{G1S} = 0, \quad V_{G2S} = +4$ volts.

If a source resistor is used, as shown in Fig. A1, the gate No. 1-to-source voltage is

$$V_{G1S} = V_{G1} - I_D R_S$$

then

$$I_D = g_{fs} (V_{G1} - I_D R_S) + I_{DS} \quad \text{or}$$

$$I_D = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}}{1 + g_{fs} R_S}$$

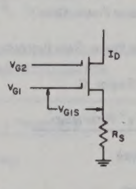


Fig. A1 – Bias circuit using the 3N200

The typical curves in Fig. A2 show drain current vs. Gate No. 1-to-Source Voltage as a function of I_{DS} level. These curves are almost linear when the typical operating drain current is in the 10-milliampere region. For the remainder of the analysis a linear relationship will be assumed for the required range of quiescent current. The assumption of linearity dictates that g_{fs} is a constant.

The required range of drain current is $I_{D2} - I_{D1}$

where:

$$I_{D2} = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}\,(\text{max.})}{1 + g_{fs} R_S}$$

$$I_{D1} = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}\,(\text{min.})}{1 + g_{fs} R_S}$$

$$\Delta I_D = I_{D2} - I_{D1} = \frac{I_{DS}\,(\text{max.}) - I_{DS}\,(\text{min.})}{1 + g_{fs} R_S} = \frac{\Delta I_{DS}}{1 + g_{fs} R_S}$$

Solving the above equation for R_S gives

$$R_S = \frac{(\Delta I_{DS}/\Delta I_D) - 1}{g_{fs}}$$

where:

g_{fs} is equal to the expected minimum value at the required I_D

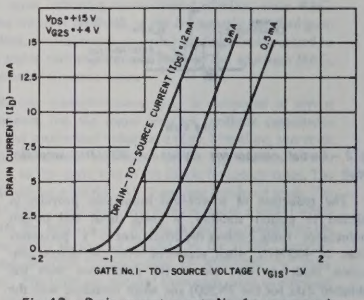


Fig. A2 – Drain current vs. gate No. 1-to-source voltage

References:

1. L. A. Jacobus and S. Reich, "Design of Gate-Protected MOS Field-Effect Transistors", RCA Application Note AN-4018
2. S. Reich, "Field-Effect Transistor Biasing Techniques", EEE, Sept. 1970
3. R. A. Santilli, "RF and IF Amplifier Design Considerations", IEEE Transactions on Broadcast and TV Receivers, Nov. 1967
4. H. Thanos, "Crossmodulation on Transistorized TV Tuners", IEEE Transactions on Broadcast and TV Receivers, Vol. 9 No. 3, Nov. 1963

Some Applications of a Programmable Power/Switch Amplifier

by L. R. Campbell and H. A. Wittlinger

The RCA-CA3094 unique monolithic programmable power switch/amplifier IC consists of a high-gain preamplifier driving a power-output amplifier stage. It can deliver average power of 3 watts or peak power of 10 watts to an external load, and can be operated from either a single or dual power supply. This Note briefly describes the characteristics of the CA3094, and illustrates its use in the following circuit applications:

Class A instrumentations and power amplifiers

Class A driver-amplifier for complementary power transistors

Wide-frequency-range power multivibrators

Current- or voltage-controlled oscillators

Comparators (threshold detectors)

Voltage regulators

Analog timers (long time delays)

Alarm systems

Motor-speed controllers

Thyristor-firing circuits

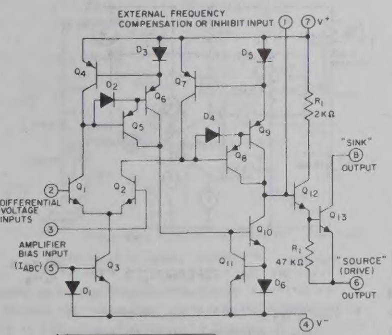
Battery-charger regulator circuits

Ground-fault-interrupter circuits

Circuit Description

The CA3094 series of devices offers a unique combination of circuit flexibility and power-handling capability. Although these monolithic IC's dissipate only a few microwatts when quiescent, they have a high current-output capability (100 milliamperes average, 300 milliamperes peak) in the active state, and the premium-grade devices can operate at supply voltages up to 44 volts.

Fig. 1 shows a schematic diagram of the CA3094. The portion of the circuit preceding transistors Q_{12} and Q_{13} is the preamplifier section and is generically similar to that of the RCA-CA3080 Operational Transconductance Amplifier (OTA).[1,2] The CA3094 circuits can be gain-programmed by either digital and/or analog signals applied to a separate Amplifier-Bias-Current (I_{ABC}) terminal (No. 5 in Fig. 1) to control circuit sensitivity. Response of the amplifier is essentially linear as a function of the current at terminal 5. This additional signal input "port" provides added flexibility in many applications. Thus, the output of the amplifier is a function of input signals applied differentially at terminals 2 and 3 and/or in a single-ended configuration at terminal 5. The output portion of the monolithic circuit in the CA3094 consists of a Darlington-connected transistor pair with access provided to both the collector and emitter terminals to provide capability to "sink" and/or "source" current.


EXTERNAL FREQUENCY COMPENSATION OR INHIBIT INPUT ①
⑦ V+
D3
D5
Q4
Q2
Q7
Q6
Q5
R1 2KΩ
D4
Q9
Q8
"SINK" ⑧ OUTPUT
② DIFFERENTIAL VOLTAGE INPUTS ③
Q1
Q2
Q12
Q13
Q10
AMPLIFIER BIAS INPUT (I_{ABC}) ⑤
Q3
D1
Q11
R1 47 KΩ
D6
"SOURCE" (DRIVE) ⑥ OUTPUT
④ V−

OUTPUT MODE	OUTPUT TERM	INPUTS	
		INV	NON-INV
"SOURCE"	6	2	3
"SINK"	8	3	2

92CS-20294

Fig. 1–CA3094 circuit schematic diagram.

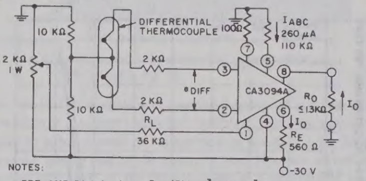
The CA3094 series of circuits consists of six types that differ only in voltage-handling capability and package options, as shown below; other electrical characteristics are identical.

Package Options	Maximum Voltage Rating
CA3094S; CA3094T	24 V
CA3094AS; CA3094AT	36 V
CA3094BS; CA3094BT	44 V

The suffix "S" indicates circuits packaged in TO-5 enclosures with leads formed to an 8-lead dual-in-line configuration (0.1" pin spacing). The suffix "T" indicates circuits packaged in 8-lead TO-5 enclosures with straight leads. The generic CA3094 type designation is used throughout this Note.

Class A Instrumentation Amplifiers

One of the more difficult instrumentation problems frequently encountered is the conversion of a differential input signal to a single-ended output signal. Although this conversion can be accomplished in a straightforward design through the use of classical op-amps, the stringent matching requirements of resistor ratios in feedback networks make the conversion particularly difficult from a practical standpoint. Because the gain of the preamplifier section in the CA3094 can be defined as the product of the transconductance and the load resistance ($g_m R_L$), feedback is not needed to obtain predictable open-loop gain performance. Fig. 2 shows the CA3094 in this basic type of circuit.



NOTES:

PRE-AMP GAIN (A_V) = $g_m R_L$ = (5) (10^{-3}) (36) (10^3) ≈ 180 (OUTPUT AT TERMINAL 1)

FOR LINEAR OPERATION: DIFFERENTIAL INPUT ≤ |±26 mV| (WITH APPROX. 1% DEVIATION FROM LINEARITY)

OUTPUT VOLTAGE (E_O) = A_V ($\pm e_{diff}$) = (180)(±26 mV) = ± 4.7 V

OUTPUT CURRENT, $I_O \approx \frac{4.7\ V}{560\ \Omega}$ = 8.35 mA

$$I_O \approx \frac{(g_m R_L)(e_{diff})}{R_E}$$

92CS 20266

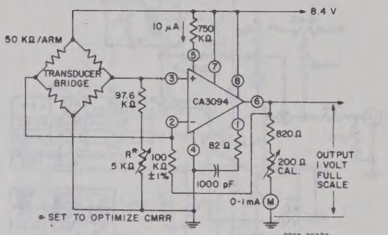
Fig. 2–Open-loop instrumentation amplifier with differential input and single-ended output.

The gain of the preamplifier section (to terminal No. 1) is $g_m R_L = (5 \times 10^{-3})(36 \times 10^3) = 180$. The transconductance g_m is a function of the current into terminal No. 5, I_{ABC}, the amplifier-bias-current. In this circuit an I_{ABC} of 260 microamperes results in a g_m of 5 millimhos. The operating point of the output stage is controlled by the 2-kilohm potentiometer. With no differential input signal ($e_{diff} = 0$), this potentiometer is adjusted to obtain a quiescent output current I_O of 12 milliamperes. This output current is established by the 560-ohm emitter resistor, R_E, as follows:

$$I_O \approx \frac{(g_m R_L)(e_{diff})}{R_E}$$

Under the conditions described, an input swing e_{diff} of ±26 millivolts produces a variation in the output current I_O of ±8.35 milliamperes. The nominal quiescent output voltage is 12 milliamperes times 560 ohms or 6.7 volts. This output level drifts approximately −4 millivolts, or −0.0595 per cent, for each °C change in temperature. Output drift is caused by temperature-induced variations in the base-emitter voltage of the two output transistors, Q_{12} and Q_{13}.

Fig. 3 shows the CA3094 used in conjunction with a resistive-bridge input network; and Fig. 4 shows a single-supply amplifier for thermocouple signals. The RC networks* connected between terminals 1 and 4 in Figs. 3 and 4 provide compensation to assure stable operation.



92CS-20279

Fig. 3–Single-supply differential-bridge amplifier.

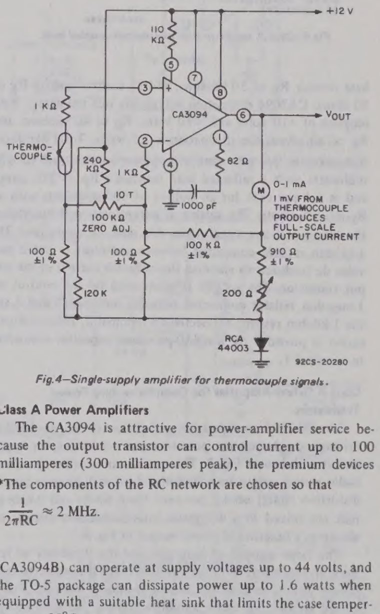


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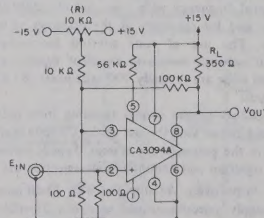
Fig. 4–Single-supply amplifier for thermocouple signals.

Class A Power Amplifiers

The CA3094 is attractive for power-amplifier service because the output transistor can control current up to 100 milliamperes (300 milliamperes peak), the premium devices (CA3094B) can operate at supply voltages up to 44 volts, and the TO-5 package can dissipate power up to 1.6 watts when equipped with a suitable heat sink that limits the case temperature to 55°C.

Fig. 5 shows a Class A amplifier circuit using the CA3094A that is capable of delivering 280 milliwatts to a 350-ohm resistive load. This circuit has a voltage gain of 60 dB and a



92CS 2028

Fig. 5–Class-A amplifier – 280-mW capability into a resistive load.

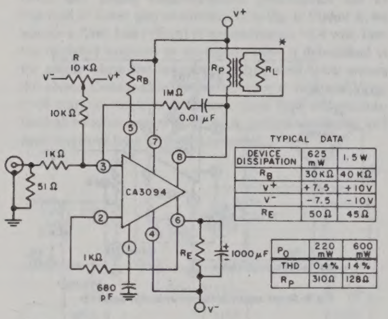
3-dB bandwidth of about 50 kHz. Operation is stable without the use of a phase-compensation network. Potentiometer R is used to establish the quiescent operating point for class A operation.

---

*The components of the RC network are chosen so that

$$\frac{1}{2\pi RC} \approx 2\ \text{MHz}.$$

The circuit of Fig. 6 illustrates the use of the CA3094 in a class A power-amplifier circuit driving a transformer-coupled load. With dual power supplies of +7.5 volts and −7.5 volts, a



TYPICAL DATA

DEVICE DISSIPATION	625 mW	1.5 W
R_B	30 KΩ	40 KΩ
V^+	+7.5	+10V
V^-	−7.5	−10V
R_E	50Ω	45Ω

P_O	220 mW	600 mW
THD	0.4%	1.4%
R_P	310Ω	128Ω

* GEN. RADIO TYPE 1840-A OUTPUT POWER METER OR EQUIVALENT

92CS-20282

Fig.6—Class-A amplifier with transformer-coupled load.

base resistor R_B of 30 kilohms, and an emitter resistor R_E of 50 ohms, CA3094 dissipation is typically 625 milliwatts. With supplies of +10 volts and −10 volts, R_B of 40 kilohms, and R_E of 45 ohms, the dissipation is 1.5 watts. Total harmonic distortion is 0.4 per cent at a power-output level of 220 milliwatts with a reflected load resistance R_P of 310 ohms, and is 1.4 per cent for an output of 600 milliwatts with an R_P of 128 ohms. The setting of potentiometer R establishes the quiescent operating point for class A operation. The 1-kilohm resistor connected between terminals 6 and 2 provides dc feedback to stabilize the collector current of the output transistor. The ac gain is established by the ratio of the 1-megohm resistor connected between terminals 8 and 3 and the 1-kilohm resistor connected to terminal 3. Phase compensation is provided by the 680-picofarad capacitor connected to terminal 1.

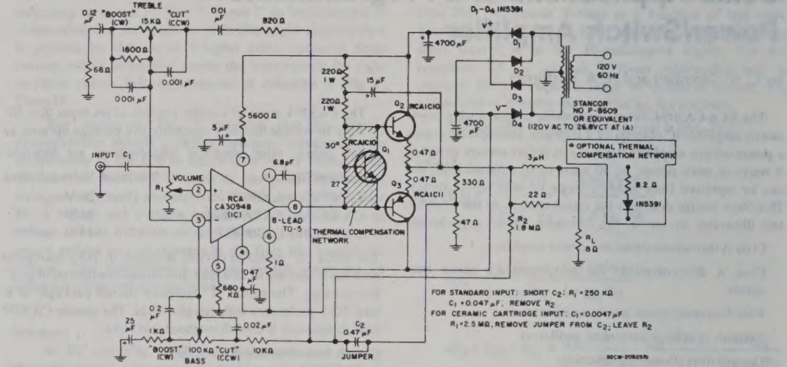
Class A Driver-Amplifier for Complementary Power Transistors

The CA3094 configuration and characteristics are ideal for driving complementary power-output transistors;[3] a typical circuit is shown in Fig. 7. This circuit can provide 12 watts of audio power output into an 8-ohm load with intermodulation distortion (IMD) of 0.2 per cent when 60-Hz and 2-kHz signals are mixed in a 4:1 ratio. Intermodulation distortion is shown as a function of power output in Fig. 8.

The large amount of loop gain and the flexibility of feedback arrangements with the CA3094 make it possible to incorporate the tone controls into a feedback network that is closed around the entire amplifier system. The tone controls in the circuit of Fig. 7 are part of the feedback network connected from the amplifier output (junction of the 330- and 47-ohm resistors driven by the emitters of Q_2 and Q_3) to terminal 3 of the CA3094. Fig. 9 shows voltage gain as a function of frequency with tone controls adjusted for "flat" response and for responses at the extremes of tone-control rotation. The use of tone controls incorporated in the feedback network results in excellent signal-to-noise ratio. Hum and noise are typically 700 microvolts (83 dB down) at the output.

In addition to the savings resulting from reduced parts count and circuit size, the use of the CA3094 leads to further savings in the power-supply system. Typical values of power-supply rejection and common-mode rejection are 90 dB and 100 dB, respectively. An amplifier with 40-dB gain and 90-dB power-supply rejection would require a 31-millivolt power-supply ripple to produce one millivolt of hum at the output. Therefore, no filtering is required other than that provided by the energy-storage capacitors at the output of the rectifier system shown in Fig. 7.

For applications in which the operating temperature range is limited (e.g., consumer service) the thermal compensation network (shaded area) can be replaced by a more economical configuration consisting of a resistor-diode combination (8.2 ohms and 1N5391) as shown in Fig. 7.



FOR STANDARD INPUT: SHORT C_2; R_1 = 250 KΩ
C_1 = 0.047 μF; REMOVE R_2
FOR CERAMIC CARTRIDGE INPUT: C_1 = 0.0047 μF
R_1 = 2.5 MΩ, REMOVE JUMPER FROM C_2; LEAVE R_2

92CM-20825R1

For 12-W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")		
Music (at 5% THD, regulated supply)	15	W
Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8	12	W
Total Harmonic Distoration		
At 1 W, unregulated supply	0.05	%
At 12 W, unregulated supply	0.57	%
Voltage Gain	40	dB
Hum and Noise (Below continuous Power Output)	83	dB
Input Resistance	250	kΩ
Tone Control Range	See Fig. 9	

Fig.7—12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.

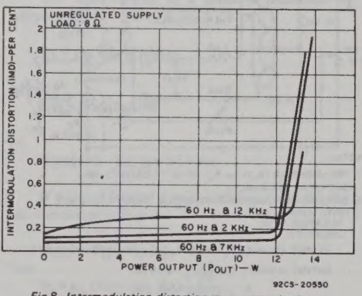


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Fig.8—Intermodulation distortion vs. power output.

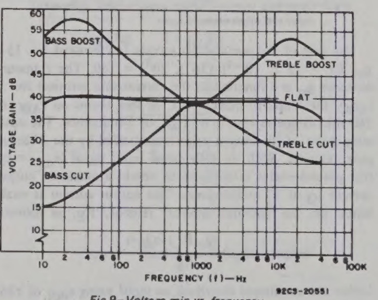

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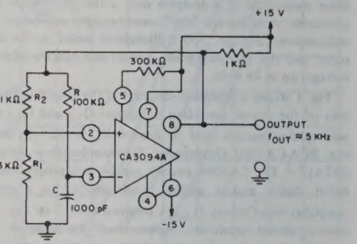
Fig.9—Voltage gain vs. frequency.

Power Multivibrators (Astable and Monostable)

The CA3094 is suitable for use in power multivibrators because its high-current output transistor can drive low-impedance circuits while the input circuitry and the frequency-determining elements are operating at micropower levels. A typical example of an astable multivibrator using the CA3094 with a dual power supply is shown in Fig. 10. The output frequency f_{OUT} is determined as follows:

$$f_{OUT} = \frac{1}{2RC\ln[(2R1/R2)+1]}$$

If R2 is equal to 3.08 R1, then f_{OUT} is simply the reciprocal of RC.

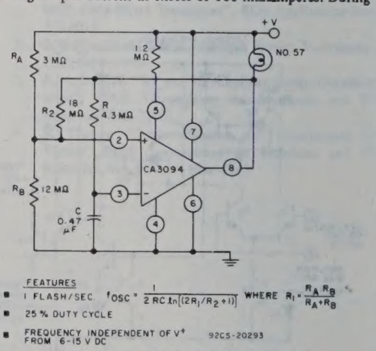


NOTE: $f_{OUT} = \frac{1}{2RC\ \ln\left(\frac{2R_1}{R_2}+1\right)}$; If $R_2 = 3.08R_1$, $f_{OUT} = \frac{1}{RC}$

92CS-20290

Fig.10—Astable multivibrator using dual supply.

Fig. 11 is a single-supply astable multivibrator circuit which illustrates the use of the CA3094 for flashing an incandescent lamp. With the component values shown, this circuit produces one flash per second with a 25-per-cent "on"-time while delivering output current in excess of 100 milliamperes. During the 75-per-cent "off"-time it idles with micropower consumption. The flashing rate can be maintained within ±2 per cent of the nominal value over a battery voltage range from 6 to 15 volts and a temperature excursion from 0 to 70°C. The CA3094 series of circuits can supply peak-power output in



FEATURES
- 1 FLASH/SEC $f_{OSC} = \frac{1}{2RC\ln[(2R_1/R_2+1)]}$ WHERE $R_1 = \frac{R_A R_B}{R_A+R_B}$
- 25% DUTY CYCLE
- FREQUENCY INDEPENDENT OF V^+ FROM 6-15 V DC

92CS-20293

Fig.11—Astable multivibrator using single supply.

excess of 10 watts when used in this type of circuit. The frequency of oscillation f_{OSC} is determined by the resistor ratios, as follows:

$$f_{OSC} = \frac{1}{2RC\ln\left[(2\,R_1/R_2) + 1\right]}$$

where

$$RI = \frac{R_A R_B}{R_A + R_B}$$

Provisions can easily be made in the circuit of Fig. 11 to vary the multivibrator pulse length while maintaining an essentially constant pulse repetition rate. The circuit shown in Fig. 12 incorporates a potentiometer Rp for varying the width of pulses generated by the astable multivibrator to drive a light-emitting diode (LED).

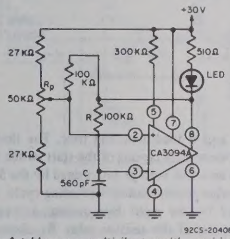


Fig. 12—Astable power multivibrator with provisions for varying duty cycle.

Fig. 13 shows a circuit incorporating independent controls (R_{ON} and R_{OFF}) to establish the "on" and "off" periods of the current supplied to the LED. The network between points "A" and "B" is analogous in function to that of the 100-kilohm resistor R in Fig. 12.

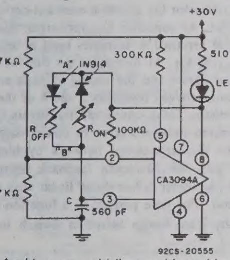


Fig. 13—Astable power multivibrator with provisions for independent control of LED "on-off" periods.

The CA3094 is also suitable for use in monostable multivibrators, as shown in Fig. 14. In essence, this circuit is a pulse counter in which the duration of the output pulses is independent of trigger-pulse duration. The meter reading is a function of the pulse repetition rate which can be monitored with the speaker.

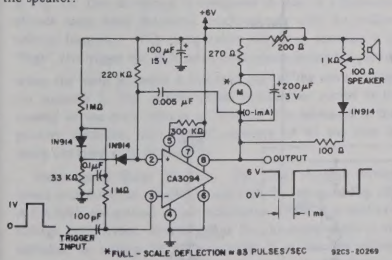


Fig. 14—Power monostable multivibrator.

Current- or Voltage-Controlled Oscillators

Because the transconductance of the CA3094 varies linearly as a function of the amplifier bias current (I_{ABC}) supplied to terminal 5, the design of a current- or voltage-controlled oscillator is straightforward, as shown in Fig. 15. Fig. 16 and 17 show oscillator frequency as a function of I_{ABC} for a current-controlled oscillator for two different values of capacitor C in Fig. 15. The addition of an appropriate resistor (R) in series with terminal 5 in Fig. 15 converts the circuit into a voltage-controlled oscillator. Linearity with respect to either current or voltage control is within 1 per cent over the middle half of the characteristics. However, variation in the symmetry of the output pulses as a function of frequency is an inherent characteristic of the circuit in Fig. 15, and leads to distortion when this circuit is used to drive the phase detector in phase-locked-loop applications. This type of distortion can be eliminated by interposing an appropriate flip-flop between the output of the oscillator and the phase-locked discriminator circuits.

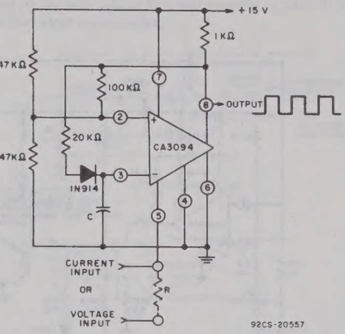


Fig. 15—Current- or voltage-controlled oscillator.

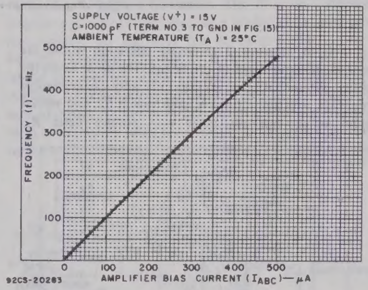


Fig. 16—Frequency as a function of I_{ABC} for C=1000 pF for circuit in Fig. 15.

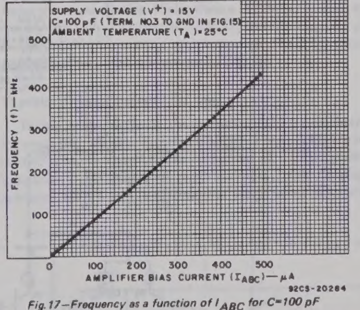


Fig. 17—Frequency as a function of I_{ABC} for C=100 pF for circuit in Fig. 15.

Comparators (Threshold Detectors)

Comparator circuits are easily implemented with the CA3094, as shown by the circuits in Fig. 18. The circuit of Fig. 18(a) is arranged for dual-supply operation; the input voltage exceeds the positive threshold, the output voltage swings essentially to the negative supply-voltage rail (it is assumed that there is negligible resistive loading on the output terminal). An input voltage that exceeds the negative threshold value results in a positive voltage output essentially equal to the positive supply voltage. The circuit in Fig. 18(b), connected for single-supply operation, functions similarly.

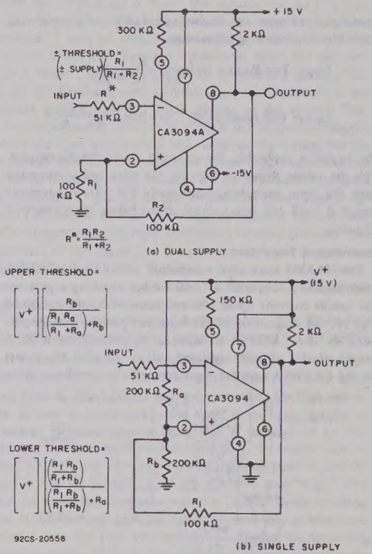


Fig. 18—Comparators (threshold detectors) — dual- and single-supply types.

Fig. 19 shows a dual-limit threshold detector circuit in which the high-level limit is established by potentiometer R1

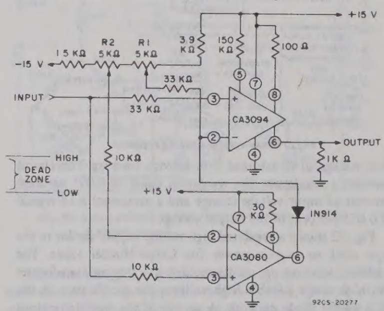


Fig. 19—Dual-limit threshold detector.

and the low-level limit is set by potentiometer R2 to actuate the CA3080 low-limit detector.[1,2] A positive output signal is delivered by the CA3094 whenever the input signal exceeds either the high-limit or the low-limit values established by the appropriate potentiometer settings. This output voltage is approximately 12 volts with the circuit shown.

The high current-handling capability of the CA3094 makes it useful in Schmitt power-trigger circuits such as that shown in Fig. 20. In this circuit, a relay coil is switched whenever the

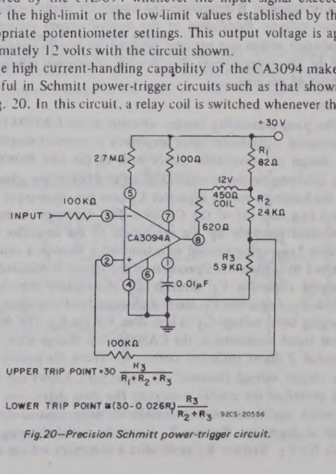


Fig. 20—Precision Schmitt power-trigger circuit.

input signal traverses a prescribed upper or lower trip point, as defined by the following expressions:

$$\text{Upper Trip Point} = 30\left(\frac{R3}{R1 + R2 + R3}\right)$$

$$\text{Lower Trip Point} \cong (30 - 0.026R1)\frac{R3}{R2 + R3}$$

The circuit is applicable, for example, to automatic ranging. With the values shown in Fig. 20, the relay coil is energized when the input exceeds approximately 5.9 volts and remains energized until the input signal drops below approximately 5.5 volts.

Power-Supply Regulators

The CA3094 is an ideal companion device to the CA3085 series regulator circuits[4] in dual-voltage tracking regulators that handle currents up to 100 milliamperes. In the circuit of Fig. 21, the magnitude of the regulated positive voltage provided by the CA3085A is adjusted by potentiometer R. A sample of this positive regulated voltage supplies the power for the CA3094A negative regulator and also supplies a reference voltage to its terminal 3 to provide tracking. This circuit provides a maximum line regulation equal to 0.075 per cent per volt of input voltage change and a maximum load regula- of 0.075 per cent of the output voltage.

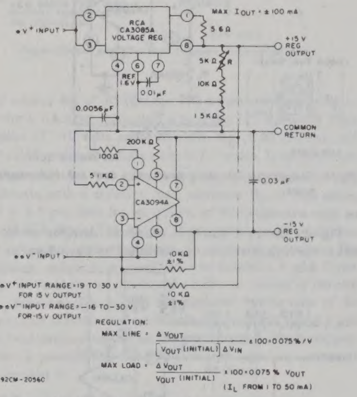

MAX. IOUT = ± 100 mA
•V+ INPUT
RCA CA3085A VOLTAGE REG
5.6 Ω
+15 V REG OUTPUT
5K Ω R
REF 1.6V
0.01 μF
10K Ω
0.0056 μF
1.5K Ω
COMMON RETURN
200K Ω
100 Ω
5.1 KΩ
CA3094A
0.03 μF
-15 V REG OUTPUT
••V- INPUT
10 KΩ ±1%
•V+ INPUT RANGE = 19 TO 30 V FOR 15 V OUTPUT
••V- INPUT RANGE = -16 TO -30 V FOR -15 V OUTPUT
REGULATION:
MAX LINE = ΔVOUT / [VOUT (INITIAL)] ΔVIN x 100 = 0.075%/V
MAX LOAD = ΔVOUT / VOUT (INITIAL) x 100 = 0.075% VOUT (IL FROM 1 TO 50 mA)
92CM-20560

Fig.21—Dual-voltage tracking regulator.

Fig. 22 shows a regulated high-voltage supply similar to the type used to supply power for Geiger-Mueller tubes. The CA3094, used as an oscillator, drives a step-up transformer which develops suitable high voltages for rectification in the RCA-44007 diode network. A sample of the regulated output voltage is fed to the CA3080A operational transconductance amplifier through the 198-megohm and 910-kilohm divider to control the pulse repetition rate of the CA3094. Adjustment of potentiometer R determines the magnitude of the regulated output voltage. Regulation of the desired output voltage is maintained within one per cent despite load-current variations of 5 to 26 microamperes. The dc-to-dc conversion efficiency is about 48 per cent.

Timers

The programmability feature inherent in the CA3094 (and operational transconductance amplifiers in general) simplifies the design of presettable timers such as the one shown in Fig. 23. Long timing intervals (e.g., up to 4 hours) are achieved by discharging a timing capacitor C_1 into the signal-input terminal (e.g., No. 3) of the CA3094. This discharge current is controlled precisely by the magnitude of the amplifier bias current I_{ABC} programmed into terminal 5 through a resistor selected by switch S2. Operation of the circuit is initiated by charging capacitor C_1 through the momentary closing of switch S_1. Capacitor C_1 starts discharging and continues discharging until voltage E_1 is less than voltage E_2. The differential input transistors in the CA3094 then change state, and terminal 2 draws sufficient current to reverse the polarity of the output voltage (terminal 6). Thus, the CA3094 not only has provision for readily presetting the time delay, but also provides significant output current to drive control devices such as thyristors. Resistor R_5 limits the initial charging current for C_1. Resistor R_7 establishes a minimum voltage of at least 1 volt at terminal 2 to insure operation within the common-mode-input range of the device. The diode limits the maximum differential input voltage to 5 volts. Gross changes in time-range selection are made with switch S2, and vernier trimming adjustments are made with potentiometer R_6.

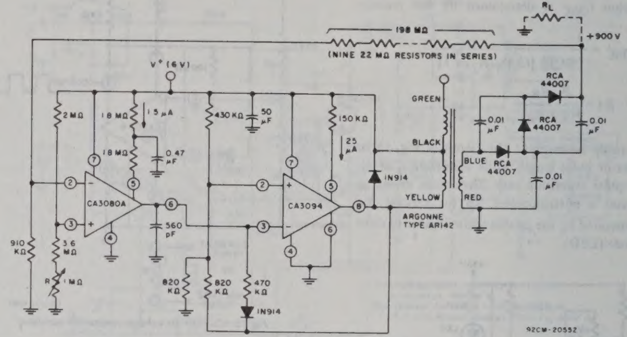


Fig.22—Regulated high-voltage supply.

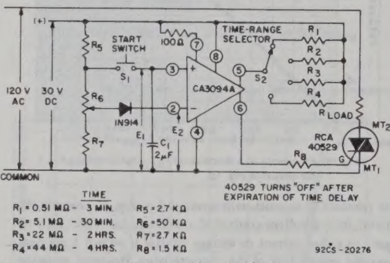


Fig.23—Presettable analog timer.

In some timer applications, such as that shown in Fig. 24, a meter readout of the elapsed time is desirable. This circuit uses the CA3094 and the CA3083 transistor array[5] to control the meter and a load-switching triac. The timing cycle starts with the momentary closing of the start switch to charge capacitor C_1 to an initial voltage determined by the 50-kilohm vernier timing adjustment. During the timing cycle, capacitor C_1 is discharged by the input bias current at terminal 3, which is a function of the resistor value R_1 chosen by the time-range selection switch. During the timing cycle the output of the CA3094, which is also the collector voltage of Q_1, is "high". The base drive for Q_1 is supplied from the positive supply through a 91-kilohm resistor. The emitter of Q_1, through the 75-ohm resistor, supplies gate-trigger current to the triac. Diode-connected transistors Q_4 and Q_5 are connected so that transistor Q_1 acts as a constant-current source to drive the triac. As capacitor C_1 discharges, the CA3094 output voltage at terminal 6 decreases until it becomes less than the V_{CEsat} of Q_1. At this point the flow of drive current to the triac ceases and the timing cycle is ended. The 20-kilohm resistor between terminals 2 and 6 of the CA3094 is a feedback resistor. Diode-connected transistors Q_2 and Q_3 and their associated networks serve to compensate for nonlinearities in the discharge-circuit network by bleeding corrective current into the 20-kilohm feedback resistor. Thus, current flow in the meter is essentially linear with respect to the timing period. The time periods as a function of R_1 are indicated on the Time-Range Selection Switch in Fig. 24.

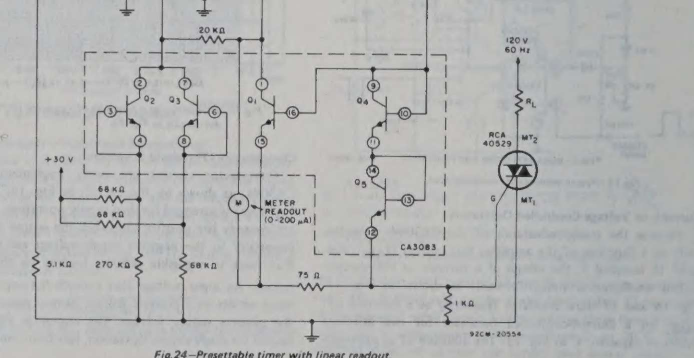


Fig.24—Presettable timer with linear readout.

Alarm Circuit

Fig. 25 shows an alarm circuit utilizing two "sensor" lines. In the "no-alarm" state, the potential at terminal 2 is lower than the potential at terminal 3, and terminal 5 (I_{ABC}) is driven with sufficient current through resistor R_5 to keep the output voltage "high". If either "sensor" line is opened, shorted to ground, or shorted to the other sensor line, the output goes "low" and activates some type of alarm system.

The back-to-back diodes connected between terminals 2 and 3 protect the CA3094 input terminals against excessive differential voltages.

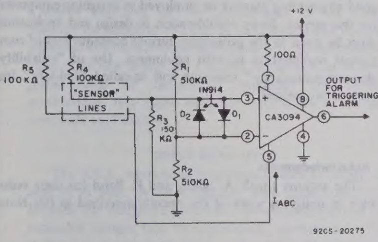


Fig.25–Alarm system.

Motor-Speed Controller System

Fig. 26 illustrates the use of the CA3094 in a motor-speed controller system. Circuitry associated with rectifiers D_1 and D_2 comprises a full-wave rectifier which develops a train of half-sinusoid voltage pulses to power the dc motor. The motor speed depends on the peak value of the half-sinusoids and the period of time (during each half-cycle) the SCR is conductive.

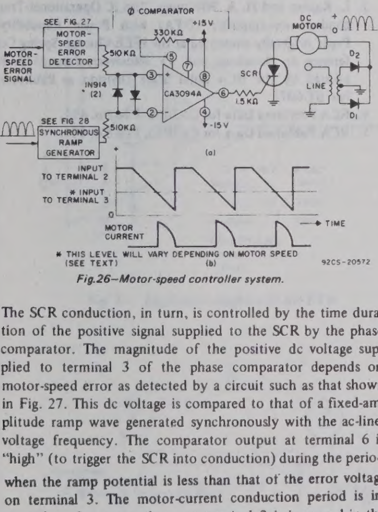


Fig.26–Motor-speed controller system.

The SCR conduction, in turn, is controlled by the time duration of the positive signal supplied to the SCR by the phase comparator. The magnitude of the positive dc voltage supplied to terminal 3 of the phase comparator depends on motor-speed error as detected by a circuit such as that shown in Fig. 27. This dc voltage is compared to that of a fixed-amplitude ramp wave generated synchronously with the ac-line-voltage frequency. The comparator output at terminal 6 is "high" (to trigger the SCR into conduction) during the period when the ramp potential is less than that of the error voltage on terminal 3. The motor-current conduction period is increased as the error voltage at terminal 3 is increased in the positive direction. Motor-speed accuracy of ±1 per cent is easily obtained with this system.

Motor-Speed Error Detector. Fig. 27(a) shows a motor-speed error detector suitable for use with the circuit of Fig. 26. A CA3080 operational transconductance amplifier is used as a voltage comparator. The reference for the comparator is established by setting the potentiometer R so that the voltage at terminal 3 is more positive than that at terminal 2 when the motor speed is too low. An error voltage E_1 is derived from a tachometer driven by the motor. When the motor speed is too low, the voltage at terminal 2 of the voltage comparator is less positive than that at terminal 3, and the output voltage at terminal 6 goes "high". When the motor speed is too high, the opposite input conditions exist, and the output voltage at terminal 6 goes "low". Fig. 27(b) also shows these conditions graphically, with a linear transition region between the "high" and "low" output levels. This linear transition region is known as "proportional bandwidth". The slope of this region is determined by the proportional bandwidth control to establish the error-correction response time.

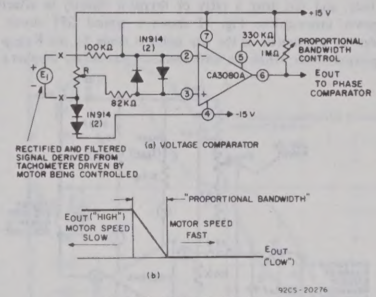


Fig. 27–Motor speed error detector.

Synchronous Ramp Generator. Fig. 28 shows a schematic diagram and signal waveforms for a synchronous ramp generator suitable for use with the motor-controller circuit of Fig. 26. Terminal 3 is biased at approximately +2.7 volts (above the negative supply voltage). The input signal E_{IN} at terminal 2 is a sample of the half-sinusoids (at line frequency) used to power the motor in Fig. 26. A synchronous ramp signal is produced by using the CA3094 to charge and discharge capacitor C_1 in response to the synchronous toggling of E_{IN}.

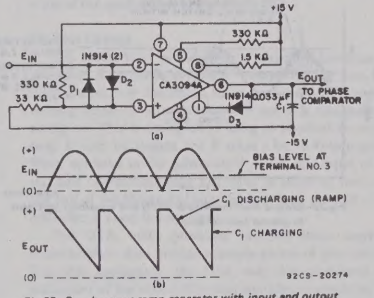


Fig.28–Synchronous ramp generator with input and output waveforms.

The charging current for C_1 is supplied by terminal 6. When terminal 2 swings more positive than terminal 3, transistors Q_{12} and Q_{13} in the CA3094 (Fig. 1) lose their base drive and become non-conductive. Under these conditions, C_1 discharges linearly through the external diode D_3 and the Q_{10}, D_6 path in the CA3094 to produce the ramp wave. The E_{out} signal is supplied to the phase comparator in Fig. 26.

Thyristor Firing Circuits

Temperature Controller. In the temperature control system shown in Fig. 29, the differential input of the CA3094 is connected across a bridge circuit comprised of a PTC (positive-temperature-coefficient) temperature sensor, two 75-kilohm resistors, and an arm containing the temperature set control. When the temperature is "low", the resistance of the PTC-type sensor is also low; therefore, terminal 3 is more positive than terminal 2 and an output current from terminal 6 of the CA3094 drives the triac into conduction. When the temperature is "high", the input conditions are reversed and the triac is cut off. Feedback from terminal 8 provides hysteresis to the control point to prevent rapid cycling of the system. The 1.5-kilohm resistor between terminal 8 and the positive supply limits the triac gate current and develops the voltage for the hysteresis feedback. The excellent power-supply-rejection and common-mode-rejection ratios of the CA3094 permit accurate repeatability of control despite appreciable power-supply ripple. The circuit of Fig. 29 is equally suitable for use with NTC (negative-temperature-coefficient) sensors provided the positions of the sensor and the associated resistor R are interchanged in the circuit. The diodes connected back-to-back across the input terminals of the CA3094 protect the device against excessive differential input signals.

Thyristor Control from AC-Bridge Sensor. Fig. 30 shows a line-operated thyristor-firing circuit controlled by a CA3094 that operates from an ac-bridge sensor. This circuit is particularly suited to certain classes of sensors that cannot be operated from dc. The CA3094 is inoperative when the high side of the ac line is negative because there is no I_{ABC} supply to terminal 5. When the sensor bridge is unbalanced so that terminal 2 is more positive than terminal 3, the output stage of the CA3094 is cut off when the ac line swings positive, and the output level at terminal 8 of the CA3094 goes "high". Current from the line flows through the 1N3193 diode to charge the 100-microfarad reservoir capacitor, and also provides current to drive the triac into conduction. During the succeeding negative swing of the ac line, there is sufficient remanent energy in the reservoir capacitor to maintain conduction in the triac.

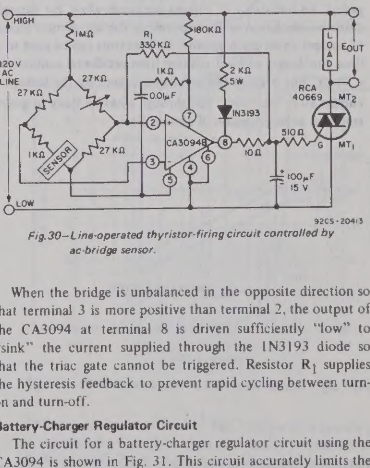


Fig.30–Line-operated thyristor-firing circuit controlled by ac-bridge sensor.

When the bridge is unbalanced in the opposite direction so that terminal 3 is more positive than terminal 2, the output of the CA3094 at terminal 8 is driven sufficiently "low" to "sink" the current supplied through the 1N3193 diode so that the triac gate cannot be triggered. Resistor R_1 supplies the hysteresis feedback to prevent rapid cycling between turn-on and turn-off.

Battery-Charger Regulator Circuit

The circuit for a battery-charger regulator circuit using the CA3094 is shown in Fig. 31. This circuit accurately limits the peak output voltage to 14 volts, as established by the zener

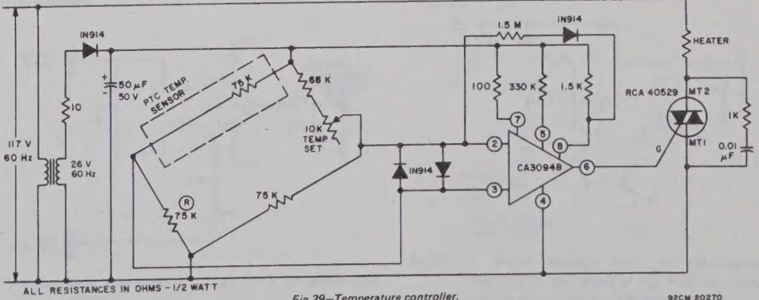


Fig.29–Temperature controller.

diode connected across terminals 3 and 4. When the output voltage rises slightly above 14 volts, signal feedback through a 100-kilohm resistor to terminal 2 reduces the current drive supplied to the 2N3054 pass transistor from terminal 6 of the CA3094. An incandescent lamp serves as the indicator of charging-current flow. Adequate limiting provisions protect the circuit against damage under load-short conditions. The advantage of this circuit over certain other types of regulator circuits is that the reference voltage supply doesn't drain the battery when the power supply is disconnected. This feature is important in portable service applications, such as in a trailer where a battery is kept "on-charge" when the trailer is parked and power is provided from an ac line.

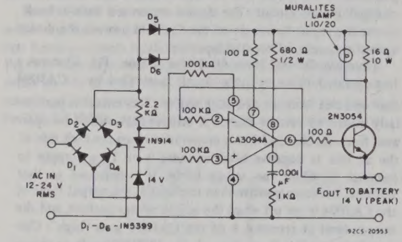
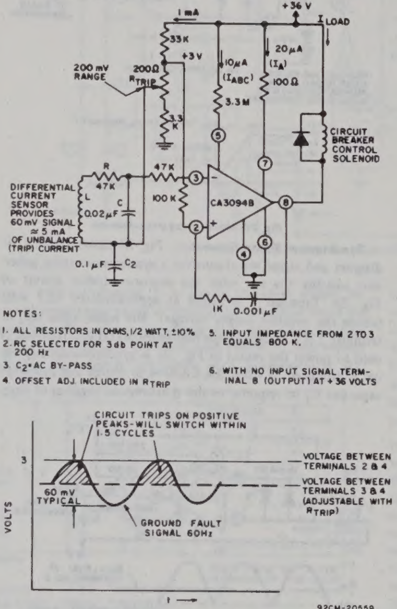


Fig.31—Battery-charger regulator circuit.

Ground-Fault Interrupters (GFI)

Ground-fault-interrupter systems are used to continuously monitor the balance of current between the high and neutral lines of power-distribution networks. Power is interrupted whenever the unbalance exceeds a preset value (e.g., 5 milliamperes). An unbalance of current can occur when, for example, defective insulation in the high side of the line permits leakage of current to an earth ground. GFI systems can be used to reduce the danger of electrocution from accidental contact with a "high" line because the unbalance caused by the leakage of current from the "high" line through a human body to ground results in an interruption of current flow.

The CA3094 is ideally suited for GFI applications because it can be operated from a single supply, has adequate sensitivity, and can drive a relay or thyristor directly to effect power interruption. Fig. 32 shows a typical GFI circuit. Vernier adjustment of the trip point is made by the R_{TRIP} potentiometer. When the differential current sensor supplies a signal that exceeds the selected trip-point voltage level (e.g., 60 millivolts), the CA3094 is toggled "on" and terminal 8 goes "low" to energize the circuit-breaker trip coil. Under quiescent conditions, the entire circuit consumes approximately 1 milliampere. The resistor R, connected to one leg of the current sensor, provides current limiting to protect the CA3094 against voltage spikes as large as 100 volts. Fig. 32 also shows the pertinent waveform for the GFI circuit.


+36 V
1 mA
I LOAD
33K
+3 V
20µA (IA)
10µA (IABC)
200 mV RANGE
200Ω RTRIP
100 Ω
3.3M
3.3 K
CIRCUIT BREAKER CONTROL SOLENOID
R 47K
47K
DIFFERENTIAL CURRENT SENSOR PROVIDES 60 mV SIGNAL ≈ 5 mA OF UNBALANCE (TRIP) CURRENT
L
C 0.02µF
100 K
CA3094B
0.1 µF C2
1K 0.001µF
CIRCUIT TRIPS ON POSITIVE PEAKS-WILL SWITCH WITHIN 1.5 CYCLES
3
VOLTAGE BETWEEN TERMINALS 2 & 4
VOLTAGE BETWEEN TERMINALS 3 & 4 (ADJUSTABLE WITH RTRIP)
60 mV TYPICAL
VOLTS
GROUND FAULT SIGNAL 60Hz
t →
92CM-20559

NOTES:

1. ALL RESISTORS IN OHMS, 1/2 WATT, ±10%
2. RC SELECTED FOR 3db POINT AT 200 Hz
3. C_2 = AC BY-PASS
4. OFFSET ADJ. INCLUDED IN R_{TRIP}
5. INPUT IMPEDANCE FROM 2 TO 3 EQUALS 800 K.
6. WITH NO INPUT SIGNAL TERMINAL 8 (OUTPUT) AT +36 VOLTS

Fig.32—Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.

Because hazards of severe electrical shock are a potential danger to the individual user in the event of malfunctions in GFI apparatus, it is mandatory that the highest standards of good engineering practice be employed in designing equipment for this service. Every consideration in design and application must be given to the potentially serious consequences of component malfunction in such equipment. Use of "reliability-through-redundancy" concepts and so-called "fail-safe" features is encouraged.

Acknowledgments

The authors thank A. Sheng and R. Baird for their assistance in designing some of the circuits described in this Note.

References

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2. Applications of the CA3080 and CA3080A High Performance Operational Transconductance Amplifiers, RCA Application Note ICAN-6668.
3. L. Kaplan and H. A. Wittlinger, "An IC Operational-Transconductance-Amplifier (OTA) with Power Capability". Paper originally presented at the IEEE Chicago Spring Conference on Broadcast and TV Receivers, June 1972. Reprinted by the RCA Solid State Division as Publication No. ST-6077.
4. RCA Published Data for CA3085, File No. 491.
5. RCA Published Data for CA3083, File No. 481.

An IC Operational-Transconductance-Amplifier (OTA) With Power Capability

by L. Kaplan and H. Wittlinger

In 1969, RCA introduced the first triple operational-transconductance-amplifier or OTA. The wide acceptance of this new circuit concept prompted the development of the single, highly linear operational-transconductance-amplifier, the CA3080. Because of its extremely linear transconductance characteristics with respect to amplifier bias current, the CA3080 gained wide acceptance as a gain-control block. The CA3094 improved on the performance of the CA3080 through the addition of a pair of transistors; these transistors extended the current-carrying capability to 300 milliamperes, peak. This new device, the CA3094, is useful in an extremely broad range of circuits in consumer and industrial applications; this paper describes only a few of the many consumer applications.

WHAT IS AN OTA?

The OTA, operational-transconductance-amplifier, concept is as basic as the transistor; once understood, it will broaden the designer's horizons to new boundaries and make realizable designs that were previously unobtainable. Fig. 1 shows an equivalent diagram of the OTA. The differential input circuit is the same as that found on many modern operational amplifiers. The remainder of the OTA is composed of current mirrors as shown in Fig. 2. The geometry of these mirrors is such that the current gain is unity. Thus, by highly degenerating the current mirrors, the output current is precisely defined by the differential-input amplifier. Fig. 3 shows the output-current transfer-characteristic of the amplifier. The shape of this characteristic remains constant and is independent of supply voltage. Only the maximum current is modified by the bias current.

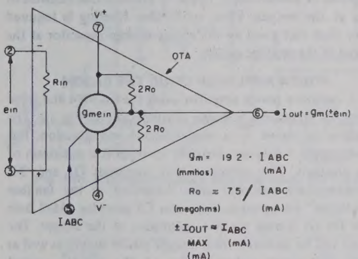


Fig. 1— Equivalent diagram of the OTA.

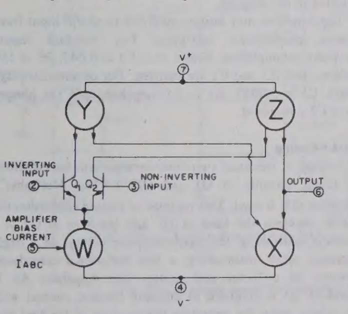


Fig. 2— Current mirrors W, X, Y, and Z used in the OTA.

The major controlling factor in the OTA is the input amplifier bias current I_{ABC}; as explained in Fig. 1, the total output current and gm are controlled by this current. In addition, the input bias current, input resistance, total supply current, and output resistance are all proportional to this amplifier bias current. These factors provide the key to the performance of this most flexible device, an idealized differential amplifier, i.e., a circuit in which differential input to single-ended output conversion can be realized. With this knowledge of the basics of the OTA, it is possible to explore some of the applications of the device.

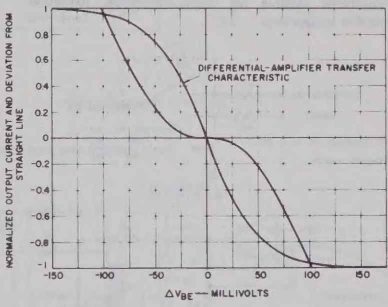


Fig. 3— The output-current transfer-characteristic of the OTA is the same as that of an idealized differential amplifier.

DC Gain Control

The methods of providing dc gain-control functions are numerous. Each has its advantage – simplicity, low cost, high level control, low distortion. Many manufacturers who have nothing better to offer propose the use of a four-quadrant multiplier. This is analogous to using an elephant to carry a twig. It may be elegant but it takes a lot to keep it going! When operated in the gain-control mode, one input of the standard transconductance multiplier is offset so that only one half of the differential input is used; thus, one-half of the multiplier is being thrown away.

The OTA, while providing excellent linear amplifier characteristics, does provide a simple means of gain control. For this application the OTA may be considered the realization of the ideal differential amplifier in which the full differential amplifier gm is converted to a single-ended output. Because the differential amplifier is ideal, its gm is directly proportional to the operating current of the differential-amplifier; in the OTA the maximum output current is equal to the amplifier bias current I_{ABC}. Thus, by varying the amplifier bias current, the amplifier gain may be varied: $A = G_m R_L$ where R_L is the output load resistance. Fig. 4 shows the basic configuration of the OTA dc gain-control circuit.[1]

As long as the differential input signal to the OTA remains under 50-millivolts peak-to-peak, the deviation from a linear transfer will remain under 5 percent. Of course, the total harmonic distortion will be considerably less than this value. Signal excursions beyond this point only result in an undesired "compressed" output. The reason for this compression can be seen in the transfer characteristic of the differential amplifier in Fig. 3. Also shown in Fig. 3 is a curve depicting the departure from a linear line of this transfer characteristic.

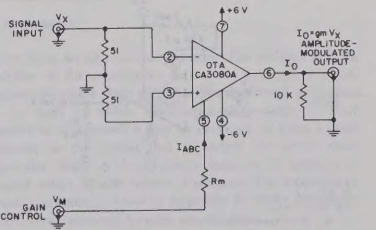
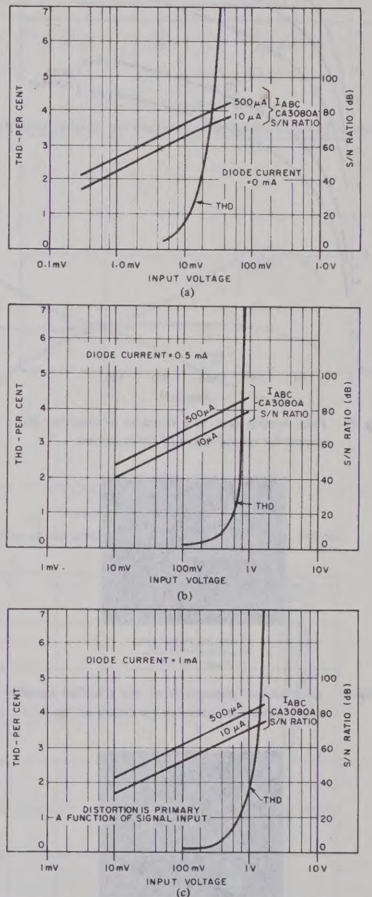


Fig. 4— Basic configuration of the OTA dc gain-control circuit.

The actual performance of the circuit shown in Fig. 4 is plotted in Fig. 5. Both signal-to-noise ratio and total harmonic distortion are shown as a function of signal input. Figs. 5(b) and (c) show how the signal-handling capability of the circuit is extended through the connection of diodes on the input as shown in Fig. 6.[2] Fig. 7 shows total system gain as a function of amplifier bias current for several values of diode current. Fig. 8 shows an oscilloscope photograph of the CA3080 transfer characteristic as applied to the circuit of Fig. 4. The oscilloscope photograph of Fig. 9 was obtained with the circuit shown in Fig. 6. Note the improvement in



(a)

(b)

(c)

Fig. 5— Performance curves for the circuits of Figs. 4 and 6.

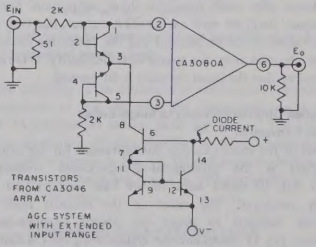

EIN
2K
51
2K
1
2
3
4
5
6
7
8
9
11
12
13
14
②
③
CA3080A
⑥
EO
10 K
DIODE CURRENT
+
V-
TRANSISTORS FROM CA3046 ARRAY
AGC SYSTEM WITH EXTENDED INPUT RANGE

Fig. 6— A circuit showing how the signal-handling capability of the circuit of Fig 4 can be extended through the connection of diodes on the input.

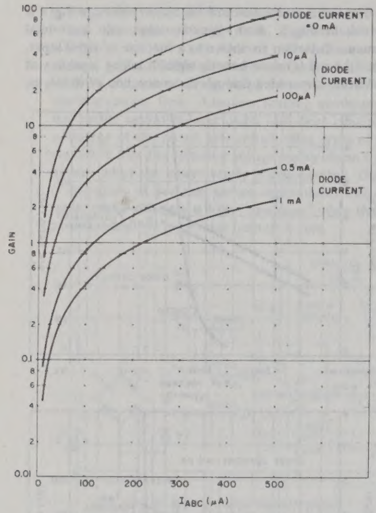


Fig. 7– Total system gain as a function of amplifier bias current for several values of diode current.

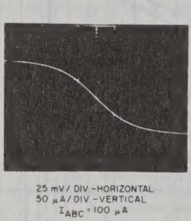


Fig. 8– Oscilloscope photograph of the CA3080 transfer characteristic as applied to the circuit of Fig. 4.

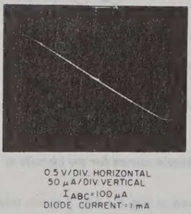


Fig. 9– Oscilloscope photograph of the CA3080 transfer characteristic as applied to the circuit of Fig. 6.

linearity of the transfer characteristic. Reduced input impedance does result from this shunt connection. Similar techniques could be used on the OTA output, but then the output signal would be reduced and the correction circuitry further removed from the source of non-linearity. It must be emphasized that the input circuitry is differential.

Simplified Differential-Input to Single-Ended Output Conversion

One of the more exacting configurations for operational amplifiers is the differential-to-single-ended conversion circuit. Fig. 10 shows some of the basic circuits that are usually employed. The ratios of the resistors must be precisely matched to assure the desired common-mode rejection. Fig. 11 shows another system using the CA3080 to obtain this conversion without the use of precision resistors. Differential input signals must be kept under ±26-millivolts for better than 5-percent non-linearity. The common-mode range is that of the CA3080 differential amplifier. In addition, the gain characteristic follows the standard differential-amplifier Gm-temperature coefficient of $-0.3\%/^{o}C$. Although the system of Fig. 11 does not provide the precise gain control obtained with the standard operational-amplifier approach, it does provide a good simple compromise suitable for many differential transducer-amplifier applications.

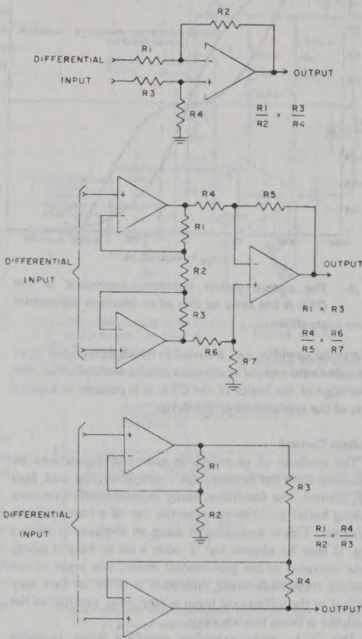


Fig. 10– Some typical differential-to-single-ended conversion circuits.

THE CA3094

The RCA CA3094 offers a unique combination of characteristics that suit it ideally to use as a programmable gain block for audio power amplifiers. It is a transconductance amplifier in which gain and open-loop bandwidth can be controlled between wide limits. The device has a large reserve of output-current capability, and breakdown and power-dissipation ratings sufficiently high to allow it to drive a complementary pair of transistors. For example, a 12-watt power-amplifier stage (8-ohm load) can be driven with peak currents of 35 milliamperes (assuming a minimum output-transistor beta of 50) and supply voltages of ±18 volts. In this application, the RCA CA3094A is operated substantially below its supply-voltage rating of 44-volts max. and its dissipation rating of 1.6-watts max. Also in this application, a high value of open-loop gain suggests the possibility of precise adjustment of frequency-response characteristics by adjustment of impedances in the feedback networks.

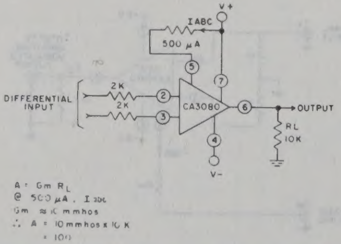


Fig. 11– A differential-to-single-ended conversion circuit without precision resistors.

Implicit Tone Controls

In addition to low distortion, the large amount of loop gain and flexibility of feedback arrangements available when using the CA3094 make it possible to incorporate the tone controls into the feedback network that surrounds the entire amplifier system. Consider the gain requirements of a phonograph playback system that uses a typical high-quality magnetic cartridge.^{3} A desirable system gain would result in from 2 to 5 watts of output at a recorded velocity of 1 cm/s. Magnetic pickups have outputs typically ranging from 4 to 10 millivolts at 5 cm/s. To get the desired output, the total system needs about 72 dB of voltage gain at the reference frequency.

Fig. 12 is a block diagram of a system that uses a passive or "losser"-type of tone-control circuit that is inserted ahead of the gain control. Fig. 13 shows a system in which the tone controls are implicit in the feedback circuits of the power amplifier. Both systems assume the same noise input voltage at the equalizer and main-amplifier inputs. The feedback system shows a small improvement (3.8 dB) in signal-to-noise ratio at maximum gain but a dramatic improvement (20 dB) at the zero gain position. For purposes of comparison, the assumption is made that the tone controls are set "flat" in both cases.

Cost Advantages

In addition to the savings resulting from reduced parts count and circuit size, the use of the CA3094 leads to further savings in the power-supply system. Typical values of power-supply rejection and common-mode rejection are 90 and 100 dB, respectively. An amplifier with 40 dB of gain and 90 dB of power-supply rejection would require 316 millivolts of power-supply ripple to produce one millivolt of hum at the output. Thus, no further filtering is required other than that given by the energy-storage capacitor at the output of the rectifier system.

POWER AMPLIFIER USING THE CA3094

A complete power amplifier using the CA3094 and three additional transistors is shown schematically in Fig. 14. The amplifier is shown in a single-channel configuration, but power-supply values are designed to support a minimum of two channels. The output section comprises Q1 and Q2, complementary epitaxial units connected in the familiar "bootstrap" arrangement. Capacitor C3 provides added base drive for Q1 during positive excursions of the output. The circuit can be operated from a single power supply as well as from a split supply as shown in Fig. 15. The changes required for 14.4-volt operation with a 3.2-ohm speaker are also indicated in the diagram.

The amplifier may also be modified to accept input from ceramic phonograph cartridges. For standard inputs (equalizer preamplifiers, tuners, etc.) C1 is 0.047, R1 is 250 kilohms, and R2 and C2 are omitted. For ceramic-cartridge inputs, C1 is 0.0047, R1 is 2.5 megohms, and the jumper across C2 is removed.

Output Biasing

Instead of the usual two-diode arrangement for establishing idling currents in Q1 and Q2, a "V_{be} Multiplier", transistor Q3, is used. This method of biasing establishes the voltage between the base of Q1 and the base of Q2 at a constant multiple of the base-to-emitter voltage of a single transistor while maintaining a low variational impedance between its collector and emitter (see Appendix A). If transistor Q3 is mounted in intimate thermal contact with the output units, the operating temperature of the heat sink forces the V_{be} of Q3 up and down inversely with heat-sink temperature. The voltage bias between the bases of Q1 and Q2 varies inversely with heat-sink temperature and tends to keep the idling current in Q1 and Q2 constant.

A bias arrangement that can be accomplished at lower cost than those already described replaces the V_{be} multiplier with a 1N5391 diode in series with an 8.2-ohm resistor. This arrangement does not provide the degree of bias stability of the V_{be} multiplier, but is adequate for many applications.

Tone-Controls

The tone controls, the essential elements of the feedback system, are located in two sets of parallel paths. The bass

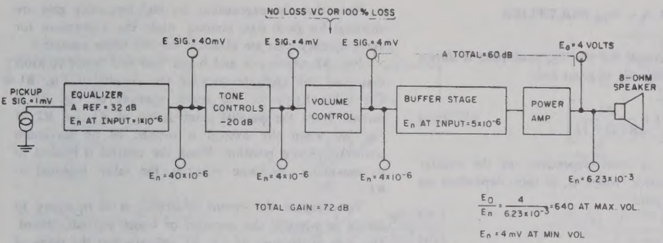


Fig. 12– Block diagram of a system using a "losser"-type tone-control circuit.

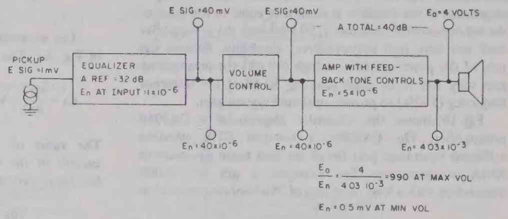


Fig. 13– A system in which tone controls are implicit in the feedback circuit of the power amplifier.

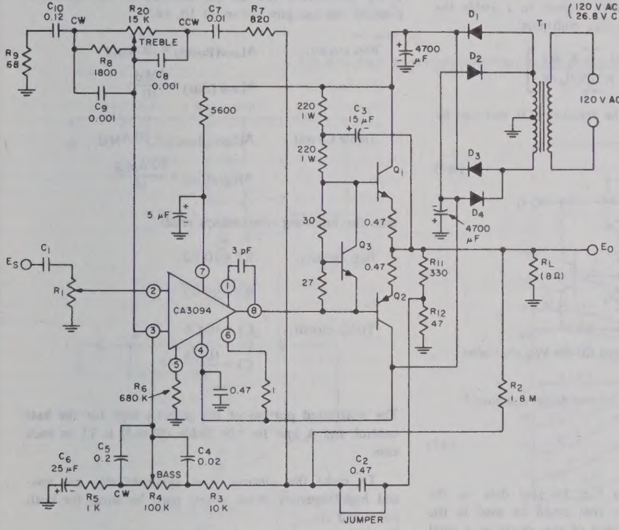


Fig. 14– A complete power amplifier using the CA3094 and three additional transistors.

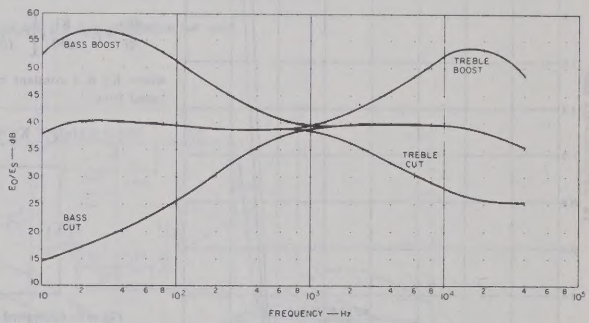


Fig. 16– The measured response of the amplifier at extremes of tone-control rotation.

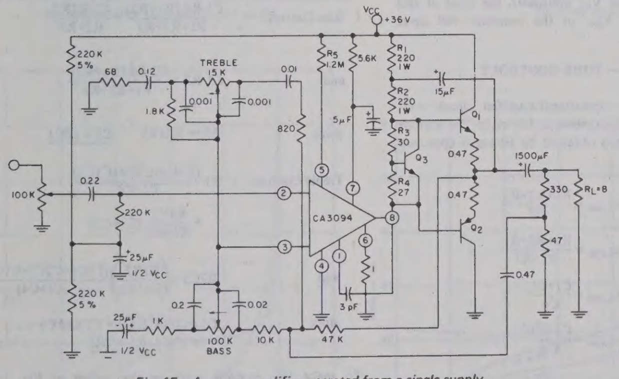


Fig. 15– A power amplifier operated from a single supply.

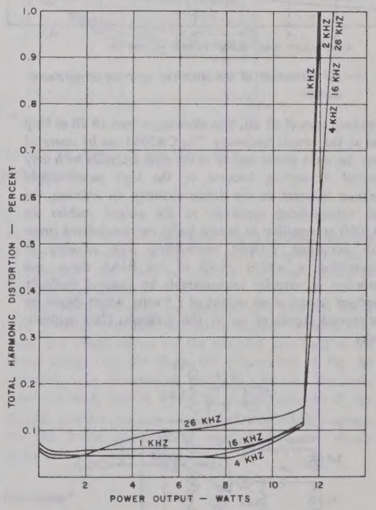


Fig. 17– Total harmonic distortion of the amplifier with an unregulated power supply.

network includes R3, R4, R5, C4, and C5. C6 blocks the dc from the feedback network so that the dc gain from input to the feedback takeoff point is unity. The residual dc-output-voltage at the speaker terminals is then $I_{ABC}\, R_I \frac{R_{11}+R_{12}}{R_{12}}$ where R_I is the source resistance. The input bias current is then $\frac{I_{ABC}}{2\beta} = -\frac{(V_{cc} - V_{be})}{2\beta R6}$. The treble network consists of R7, R8, R9, R10, C7, C8, C9, and C10. Resistors R7 and R9 limit the maximum available cut and boost, respectively. The boost limit is useful in curtailing heating due to finite turn-off time in the output units. The limit is also desirable when there are tape recorders nearby. The cut limit aids the stability of the amplifier by cutting the loop gain at higher frequencies where phase shifts become significant.

In cases in which absolute stability under all load conditions is required, it may be necessary to insert a small inductor in the output lead to isolate the circuit from capacitive loads. A 3-microhenry inductor (1 ampere) in parallel with a 22-ohm resistor is adequate. The derivation of circuit constants is shown in Appendix B. Curves of control action versus electrical rotation are also given.

Performance

Fig. 16 is a plot of the measured response of the complete amplifier at the extremes of tone-control rotation. A comparison of Fig. 16 with the computed curves of Fig. B4 (Appendix B) shows good agreement. The total harmonic distortion of the amplifier with an unregulated power supply is shown in Fig. 17; IM distortion is plotted in Fig. 18. Hum and noise are typically 700 microvolts at the output, or 83-dB down.

COMPANION RIAA PREAMPLIFIER

Many available preamplifiers are capable of providing the drive for the power amplifier of Fig. 14. Yet the unique characteristics of the amplifier – its power supply, input impedance, and gain – make possible the design of an RIAA preamplifier that can exploit these qualities. Since the input impedance of the amplifier is essentially equal to the value of the volume-control resistance (250 kilohms), the preamplifier need not have high output-current capability. Because the gain of the power amplifier is high (40 dB) the preamplifier gain only has to be approximately 30 dB at the reference frequency (1 kHz) to provide optimum system gain.

Fig. 19 shows the schematic diagram of a CA3080 preamplifier. The CA3080, a low-cost OTA, provides sufficient open-loop gain for all the bass boost necessary in RIAA compensation. For example, a gm of 10,000 micromhos with a load resistance of 250 kilohms provides an open-loop gain of 68 dB, thus allowing at least 18 dB of loop gain at the lowest frequency. The CA3080 can be operated from the same power supply as the main amplifier with only minimal decoupling because of the high power-supply rejection inherent in the device circuitry. In addition, the high voltage-swing capability at the output enables the CA3080 preamplifier to handle badly over-modulated (overcut) recordings without overloading. The accuracy of equalization is within ±1 dB of the RIAA curve, and distortion is virtually unmeasurable by classical methods. Overload occurs at an output of 7.5 volts, which allows for undistorted inputs of up to 186 millivolts (260 millivolts peak).

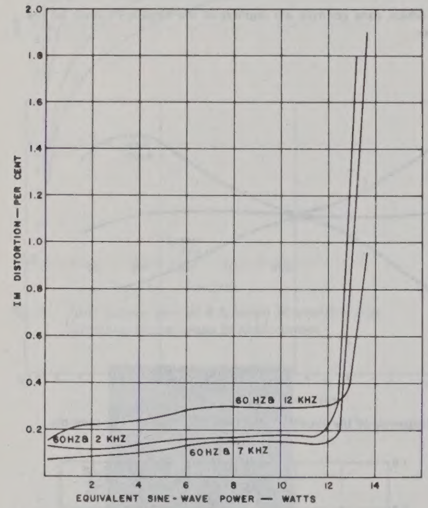


Fig. 18– IM distortion of the amplifier with an unregulated supply.

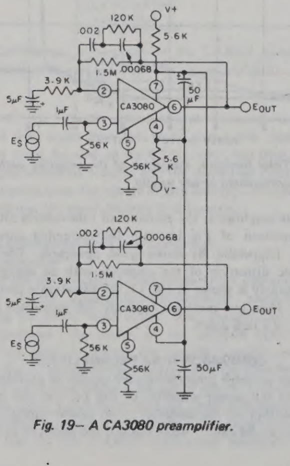


Fig. 19– A CA3080 preamplifier.

APPENDIX A – V_{be} MULTIPLIER

The equivalent circuit for the V_{be} multiplier is shown in Fig. A1. The voltage E_1 is given by:

$$E_1 = \frac{R1I}{\beta+1} + V_{be}\left[1 + \frac{R1}{R2(\beta+1)}\right] \qquad (A1)$$

The value of V_{be} is itself dependent on the emitter current of the transistor, which is, in turn, dependent on the input current I since:

$$I_e = I - \frac{V_{be}}{R2} \qquad (A2)$$

The derivative of Eq. A1 with respect to I yields the incremental impedance of the V_{be} multiplier:

$$\frac{dE_1}{dI} = Z = \frac{R1}{\beta+1} + \left[1 + \frac{BR1}{(\beta+1)R2}\right]\left[\frac{K_3R2}{R2I_e+K_3}\right] \qquad (A3)$$

where K_3 is a constant of the transistor Q1 and can be found from:

$$V_{be} = K_3 \ln I_e - K_2 \qquad (A4)$$

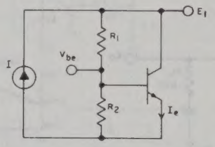


Fig. A1– Equivalent circuit for the V_{be} multiplier.

Eq. A4 is but another form of the diode equation:4

$$I_e = I_s\left(e^{\frac{qV_{be}}{KT}} - 1\right) \qquad (A5)$$

Using the values shown in Fig. 14 plus data on the 2N5494 (a typical transistor that could be used in the circuit), the dynamic impedance of the circuit at a total current of 40 milliamperes is found to be 4.6 ohms. In the actual design of the V_{be} multiplier, the value of IR2 must be greater than V_{be} or the transistor will never become forward biased.

APPENDIX B – TONE CONTROLS

Fig. B1 shows four operational-amplifier circuit configurations and the gain expressions for each. The asymptotic low-frequency gain is obtained by letting S approach zero in each case:

Bass Boost: $A_{Low} = \frac{R1+R2+R3}{R2}$

Bass Cut: $A_{Low} = \frac{R1+R2+R3}{R2+R3}$

Treble Boost: $A_{Low} = \frac{C1+C4}{C4}$

Treble Cut: $A_{Low} = \frac{C1+C4}{C4}$

The asymptotic high-frequency gain is obtained by letting S increase without limit in each expression:

Bass boost: $A_{High} = \frac{R1+R2}{R2}$

Bass cut: $A_{High} = \frac{R1+R2}{R2}$

Treble boost: $A_{High} = 1 + C1\left(\frac{C3+C4}{C3C4}\right)$

Treble cut: $A_{High} = \frac{C2 + \frac{C1C4}{C1+C4}}{C1+C2}$

Note that the expressions for high-frequency gain are identical for both bass circuits, while the expressions for low-frequency gain are identical for the treble circuits.

Fig. B2 shows cut and boost bass and treble controls that have the characteristics of the circuits of Fig. B1. The value R_{EFF} in the treble controls of Fig. B1 is derived from the parallel combination of R1 and R2 of Fig. B2 when the control is rotated to its maximum counterclockwise position. When the control is rotated to its maximum clockwise position, the value is equal to R1.

To compute the circuit constants, it is necessary to decide in advance the amounts of boost and cut desired. The gain expressions of Fig. B1 indicate that the slope of the amplitude versus frequency curve in each case will be 6 dB per octave (20 dB per decade). If the ratios of boosted and cut gain are set at 10, i.e.:

Bass circuit: $A_{Low(Boost)} = 10\,A_{Mid}$

$A_{Low\,(Cut)} = \frac{A_{Mid}}{10}$

Treble Circuit: $A_{High\,(Boost)} = 10\,A_{Mid}$

$A_{High(Cut)} = \frac{10\,A_{Mid}}{10}$

then the following relationships result:

Bass circuit: $R1 = 10\,R2$

$R3 = 99\,R2$

Treble circuit: $C1 = 10\,C4$

$C2 = \frac{10\,C4}{99}$

The unaffected portion of the gain (A high for the bass control and A low for the treble control) is 11 in each case.

To make the controls work symmetrically, the low- and high-frequency break points must be equal for both boost and cut.
Thus:

Bass Control: $\frac{C1\,R3\,(R1+R2)}{R1+R2+R3} = \frac{C2\,R2R3}{R2+R3}$

and $C1\,R3 = \frac{C2\,R3\,(R1+R2)}{R1+R2+R3}$

since $R3 \simeq R2+R3$, $\underline{C2 = 10C1}$

Treble Control: $R1\,\frac{(C1C4+C3C4+C1C3)}{C1+C4}$

$= \frac{R1R2}{R1+R2}(C1+C2)$

and $R2C3 = \left(\frac{R1R2}{R1+R2}\right)\frac{(C1C4+C2C4+C1C2)}{(C1+C4)}$

since $C1 \simeq 100C2$, $C2 = C3$ and $C1 = 10C4$, $\underline{R1 = 9R2}$

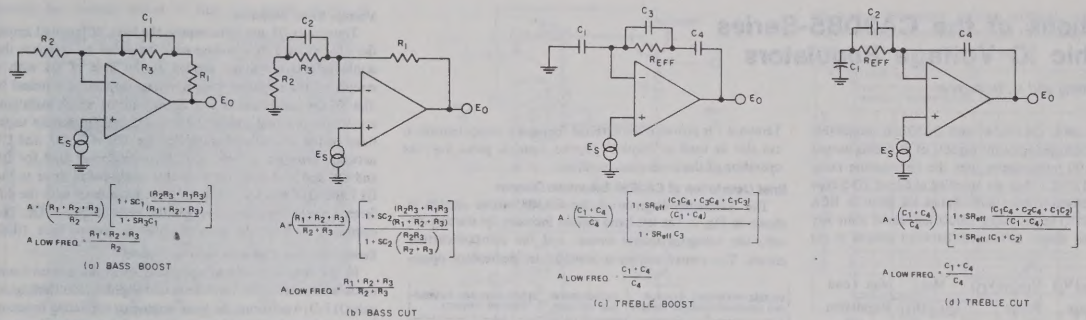
To make the controls work in the circuit of Fig. 14, breaks were set at 1000 Hz:

for the base control $0.1C1R3 = \frac{1}{2\pi \times 1000}$

and for the treble control $R1C3 = \frac{1}{2\pi \times 1000}$

Response and Control Rotation

In a practical design, it is desirable to make "flat" response correspond to the 50-percent rotation position of the control, and to have an aural sensation of smooth variation of response on either side of the mechanical center. It is easy to show that the "flat" position of the bass control occurs when the wiper arm is advanced to



(a) BASS BOOST

$$A = \left(\frac{R_1 + R_2 + R_3}{R_2}\right)\left[\frac{1 + SC_1\frac{(R_2R_3 + R_1R_3)}{(R_1 + R_2 + R_3)}}{1 + SR_3C_1}\right]$$

$$A_{LOW\ FREQ} = \frac{R_1 + R_2 + R_3}{R_2}$$

(b) BASS CUT

$$A = \left(\frac{R_1 + R_2 + R_3}{R_2 + R_3}\right)\left[\frac{1 + SC_2\frac{(R_2R_3 + R_1R_3)}{(R_1 + R_2 + R_3)}}{1 + SC_2\left(\frac{R_2R_3}{R_2 + R_3}\right)}\right]$$

$$A_{LOW\ FREQ} = \frac{R_1 + R_2 + R_3}{R_2 + R_3}$$

(c) TREBLE BOOST

$$A = \left(\frac{C_1 + C_4}{C_4}\right)\left[\frac{1 + SR_{eff}\frac{(C_1C_4 + C_3C_4 + C_1C_3)}{(C_1 + C_4)}}{1 + SR_{eff}C_3}\right]$$

$$A_{LOW\ FREQ} = \frac{C_1 + C_4}{C_4}$$

(d) TREBLE CUT

$$A = \left(\frac{C_1 + C_4}{C_4}\right)\left[\frac{1 + SR_{eff}\frac{(C_1C_4 + C_2C_4 + C_1C_2)}{(C_1 + C_4)}}{1 + SR_{eff}(C_1 + C_2)}\right]$$

$$A_{LOW\ FREQ.} = \frac{C_1 + C_4}{C_4}$$

Fig. B1– Four operational-amplifier circuit configurations and the gain expressions for each.

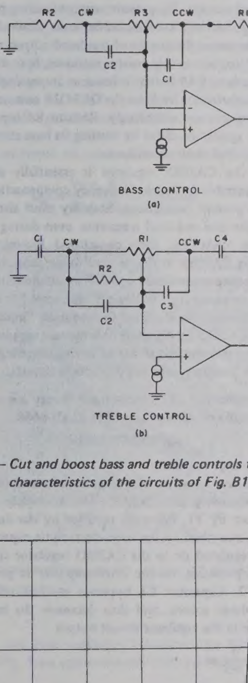


Fig. B2– Cut and boost bass and treble controls that have the characteristics of the circuits of Fig. B1.

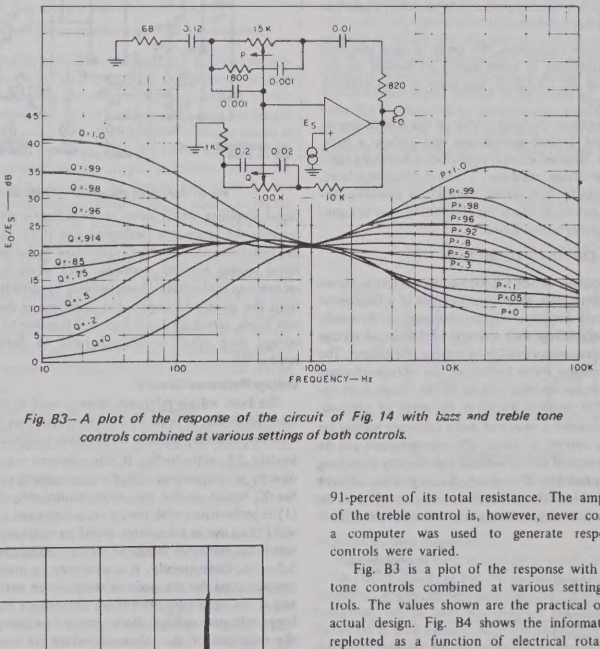


Fig. B3– A plot of the response of the circuit of Fig. 14 with bass and treble controls combined at various settings of both controls.

91-percent of its total resistance. The amplitude response of the treble control is, however, never completely "flat"; a computer was used to generate response curves as controls were varied.

Fig. B3 is a plot of the response with bass and treble tone controls combined at various settings of both controls. The values shown are the practical ones used in the actual design. Fig. B4 shows the information of Fig. B3 replotted as a function of electrical rotation. The ideal taper for each control would be the complement of the 100-Hz plot for the bass control and the 10-kHz response for the treble control. The mechanical center should occur at the crossover point in each case.

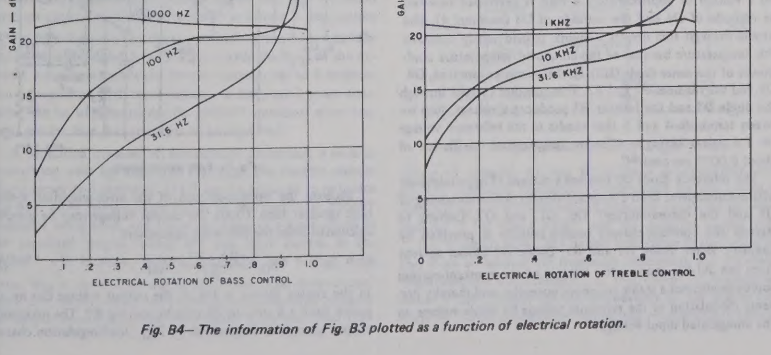


Fig. B4– The information of Fig. B3 plotted as a function of electrical rotation.

References*

1. "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers," H. A. Wittlinger, RCA Application Note ICAN-6668
2. "A New Wide-band Amplifier Technique," B. Gilbert, IEEE Journal of Solid State Circuits, Vol. SC-3, No. 4, December, 1968.
3. "Trackability," James A. Kogar, *Audio*, December 1966
4. *RCA Linear Integrated Circuits Manual*, RCA Technical Series IC-42

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*RCA publications available through RCA Solid State Division, Box 3200, Somerville, N.J., 08876.

ICAN-6157

Applications of the CA3085-Series Monolithic IC Voltage Regulators

by A. C. N. Sheng and L. R. Avery

The RCA-CA3085, CA3085A, and CA3085B monolithic IC's are positive-voltage regulators capable of providing output currents up to 100 milliamperes over the temperature range from −55° to +125°C. They are supplied in 8-lead TO-5 type packages; their characteristics and ratings are given in RCA Data File No. 491. The following tabulation shows some key characteristics and salient differences between devices in the CA3085 Series.

Type	$V_{IN}(V_I)$ Range V	$V_{OUT}(V_O)$ Range V	Max. $I_{OUT}(I_O)$ mA	Max. Load Regulation % V_O
CA3085	7.5–30	1.8–26	12*	0.1
CA3085A	7.5–40	1.7–36	100	0.15
CA3085B	7.5–50	1.7–46	100	0.15

* This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

In addition to these differences, the range of some specified performance parameters is more tightly controlled in the CA3085B than in the CA3085A, and more in the CA3085A than in the CA3085.

This Note describes the basic circuit of the CA3085-series devices and some typical applications that include a high-current regulator, constant-current regulators, a switching regulator, a negative-voltage regulator, a dual-tracking regulator, high-voltage regulators, and various methods of providing current limiting. A circuit in which the CA3085 is used as a general-purpose amplifier is also shown.

CIRCUIT DESCRIPTION

The block diagram of the CA3085-series circuits is shown in Fig. 1. Fundamentally, the circuit consists of a frequency-compensated error-amplifier which compares an internally generated reference voltage with a sample of the output voltage and controls a series-pass amplifier to regulate the output. The starting circuit assures stable latch-in of the voltage-reference circuitry. The current-limiting portion of the circuit is an optional feature that protects the IC in the event of overload.

Terminal 5 provides a source of stable reference voltage for auxiliary use; a current of about 250 microamperes can be supplied to an external circuit without significantly disturbing reference-voltage stability. If necessary, filtering of the inherent noise of the reference-voltage circuit can be accomplished by connecting a suitable bypass capacitor between terminals 5 and 4.

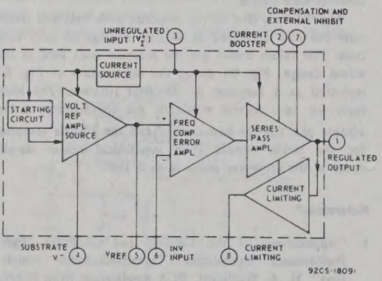

Fig. 1– Block diagram of CA3085 series.

Terminal 6 (the "inverting input" in accordance with operational-amplifier terminology) is the input through which a sample of the regulated output voltage is applied.

The collector of the series-pass output transistor is brought out separately at terminal 2 ("current booster") to provide base drive for an external p-n-p transistor; this approach is one method of regulating currents greater than 100 milliamperes.

Because the voltage regulator is essentially an operational amplifier having considerable feedback, frequency compensation is necessary in some circuits to prevent oscillations. Terminal 7 is provided for external frequency compensation; it can also be used to "inhibit" (strobe, squelch, pulse, key) the operation of the series-pass amplifier.

Brief Description of CA3085 Schematic Diagram

The schematic diagram of the CA3085-series circuits is shown in Fig. 2. The left-hand section includes the starting circuit, the voltage-reference circuit, and the constant-current circuit. The center section is basically an elementary operational amplifier which serves as the voltage-error amplifier. It controls the series-pass Darlington pair (Q13, Q14) shown in the right-hand section. When controlled by an appropriate external sensing network, transistor Q15 serves to provide protective current-limiting characteristics by diverting base drive from the series-pass circuit. For operation at the highest current levels, terminals 2 and 3 are tied together to eliminate the voltage drop which would otherwise be developed across resistor R5.

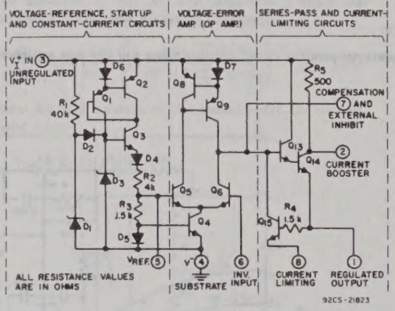
VOLTAGE-REFERENCE, STARTUP AND CONSTANT-CURRENT CIRCUITS
VOLTAGE-ERROR AMP. (OP AMP.)
SERIES-PASS AND CURRENT-LIMITING CIRCUITS
V_I^+ IN ③
UNREGULATED INPUT
R1 40k
D6
Q2
Q1
D2
Q3
D4
D3
R2 4k
R3 1.5k
D1
D5
VREF ⑤
Q8
D7
Q9
Q5
Q6
Q4
V⁻ ④
SUBSTRATE
⑥ INV. INPUT
R5 500
COMPENSATION ⑦ AND EXTERNAL INHIBIT
Q13
Q14
② CURRENT BOOSTER
R4 1.5k
Q15
⑧ CURRENT LIMITING
① REGULATED OUTPUT
ALL RESISTANCE VALUES ARE IN OHMS
92CS-21823

Fig. 2– Schematic diagram of CA3085 series.

Voltage-Reference Circuits

The basic voltage-reference element used in the CA3085 is zener diode D3. It provides a nominal reference voltage of 5.5 volts and exhibits a positive temperature coefficient of approximately 2.5 millivolts/°C. If this reference voltage were used directly in conjunction with the error-amplifier (Q5, Q6, etc.), the IC would exhibit two major undesirable characteristics: (1) its performance with temperature variations would be poor, and (2) its use as a regulator would be restricted to circuits in which the minimum regulated output voltages are in excess of 5.5 volts. Consequently, it is necessary to provide means of compensating for the positive temperature coefficient of D3 and at the same time provide for obtaining a stable source of lower reference voltage. Both temperature compensation and the reduction of the reference voltage are accomplished by means of the series divider network consisting of the base-emitter junction of Q3, diode D4, resistors R2 and R3, and diode 5.

The voltage developed across D3 drives the divider network and a voltage of approximately 4 volts is developed between the cathode of D4 and the cathode of D5 (terminal 4). The current through this divider network is held nearly constant with temperature because of the combined temperature coefficients of the zener diode (D3), Q3 base-emitter junction, D4 D5, and the resistors R2 and R3. This constant current through the diode D5 and the resistor R3 produces a voltage drop between terminals 4 and 5 that results in the reference voltage (≈ 1.6 volts) having an effective temperature coefficient of about 0.0035 per cent/°C.

The reference diode D3 receives a current of approximately 620 microamperes from a constant-current circuit consisting of Q3 and the current-mirror* D6, Q1, and Q2. Current to startup the constant-current source initially is provided by auxiliary zener diode D1 and R1. Diode D2 blocks current from the R1-D1 source after latch-in of the constant-current source establishes a stable reference potential, and thereby prevents modulation of the reference voltage by ripple voltage on the unregulated input voltage.

Voltage-Error Amplifier

Transistors Q5 and Q6 comprise the basic differential amplifier that is used as a voltage-error amplifier to compare the stable reference voltage applied at the base of Q5 with a sample of the regulator output voltage applied at terminal 6. The D5-Q4 combination is a current-mirror which maintains essentially constant-current flow to Q5 and Q6 despite variations in the unregulated input voltage. The Q8, Q9, and D7 network provides a "mirrored" active collector load for Q5 and Q6 and also provides a variable single-ended drive to the Q13 and Q14 series-pass transistors in accordance with the difference signal developed between the bases of Q5 and Q6. The open-loop gain of the error-amplifier is greater than 1000.

Series-Pass and Current-Limiting Circuits

In the normal mode of operation, or in the current-boost mode when terminals 2 and 3 are tied together, the Darlington pair Q13-Q14 performs the basic series-pass regulating function between the unregulated input voltage and the regulated output voltage at terminal 1. In the current-limiting mode transistor Q15 provides current-limiting to protect the CA3085 and/or limit the load current. To provide current-limiting protection, a resistor (e.g., 5 ohms) is connected between terminals 1 and 8; terminal 8 becomes the source of regulated output voltage. As the voltage drop across this resistor increases, base drive is supplied to transistor Q15 so that it becomes increasingly conductive and diverts base drive from the Q13-Q14 pass transistor to reduce output current accordingly. Resistor R4 is provided to protect Q15 against overdrive by limiting its base current under transient and load-short conditions.

Because the CA3085 regulator is essentially an op-amp having considerable feedback, frequency compensation may be required to prevent oscillations. Stability must also be maintained despite line and load transients, even during operation into reactive loads (e.g., filter capacitors). Provisions are included in the CA3085 so that a small-value capacitor may be connected between terminals 6 and 7 to compensate the regulator, when necessary, by "rolling-off" the amplifier frequency-response. Terminal 7 is also used to externally "inhibit" operation of the CA3085 by diverting base current supplied to Q13-Q14, thereby permitting the use of keying, strobing, programming, and/or auxiliary overload-protection circuits.

APPLICATIONS

A Simple Voltage Regulator

Fig. 3 shows the schematic diagram of a simple regulated power supply using the CA3085. The ac supply voltage is stepped down by T1, full-wave rectified by the diode bridge circuit, and smoothed by the large electrolytic capacitor C1 to provide unregulated dc to the CA3085 regulator circuit. Frequency compensation of the error-amplifier is provided by capacitor C2. Capacitor C3 bypasses residual noise in the reference-voltage source, and thus decreases the incremental noise-voltage in the regulator circuit output.

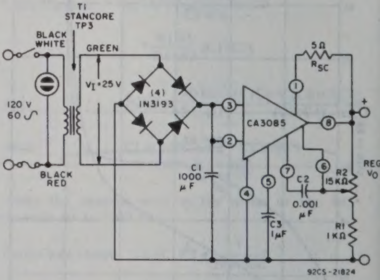

Fig. 3– Basic power supply.

Because the open-loop gain of the error-amplifier is very high (greater than 1000), the output voltage may be directly calculated from the following expression:

$$V_O = \frac{(R2 + R1)}{R1} V_{ref} \qquad (1)$$

In the circuit shown in Fig. 3, the output voltage can be adjusted from 1.8 volts to 20 volts by varying R2. The maximum output current is determined by R_{SC}; load-regulation characteristics for various values of R_{SC} are shown in Fig. 4.

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* The fundamentals of current-mirror theory are reviewed in the Appendix of Application Note ICAN-6668.

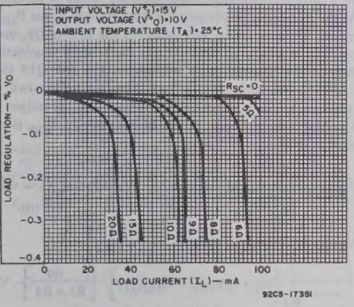


Fig. 4— Load regulation characteristics for circuit of Fig. 3.

When this circuit is used to provide high output currents at low output voltages, care must be exercised to avoid excessive IC dissipation. In the circuit of Fig. 3, this dissipation control can be accomplished by increasing the primary-to-secondary transformer ratio (a reduction in V_I) or by using a dropping resistor between the rectifier and the CA3085 regulator. Fig. 5 gives data on dissipation limitation (V_I-V_O vs. I_O) for CA3085-series circuits.

The short-circuit current is determined as follows:

$$I_{SC} = \frac{V_{BE}}{R_{SC}} \approx \frac{0.7}{R_{SC}} \text{ amperes} \tag{2}$$

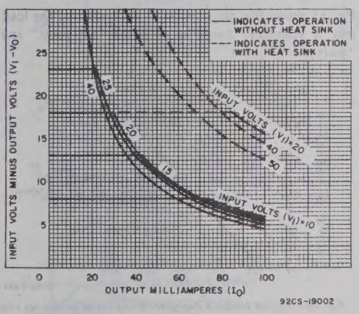


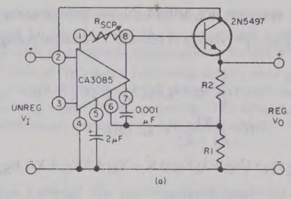
Fig. 5— Dissipation limitation (V_I – V_O vs. I_O) for CA3085 series circuits.

The line- and load-regulation characteristics for the circuit shown in Fig. 3 are approximately 0.05 per cent of the output voltage.

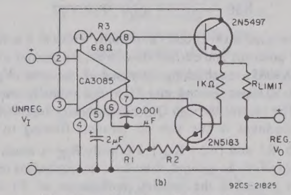
High-Current Voltage Regulator

When regulated voltages at currents greater than 100 milliamperes are required, the CA3085 can be used in conjunction with an external n-p-n pass-transistor as shown in the circuits of Fig. 6. In these circuits the output current available from the regulator is increased in accordance with the h_{FE} of the external n-p-n pass-transistor. Output currents up to 8 amperes can be regulated with these circuits. A Darlington power transistor can be substituted for the 2N5497 transistor when currents greater than 8 amperes are to be regulated.

A simplified method of short-circuit protection is used in connection with the circuit of Fig. 6(a). The variable resistor R_{SCP} serves two purposes: (1) it can be adjusted to optimize the base drive requirements (h_{FE}) of the particular 2N5497 transistor being used, and (2) in the event of a short-circuit in the regulated output voltage the base drive current in the 2N5497 will increase, thereby increasing the voltage drop across R_{SCP}. As this voltage-drop increases the short-circuit protection system within the CA3085 correspondingly reduces the output current available at terminal 8, as described previously. It should be noted that the degree of short-circuit protection depends on the value of R_{SCP}, i.e., design compromise is required in choosing the value of R_{SCP} to provide the desired base drive for the 2N5497 while maintaining the desired short-circuit protection. Fig. 6(b) shows an alternate circuit in which an additional transistor (2N5183) and two resistors have been added as an auxiliary short-circuit protection feature. Resistor R3 is used to establish the desired base drive for the 2N5497, as described above. Resistor R_{limit} now controls the short-circuit output current because, in the event of a short-circuit, the voltage drop developed across its terminals increases sufficiently to increase the base drive to the 2N5183 transistor. This increase in base drive results in reduced output from the CA3085 because collector current flow in the 2N5183 diverts base drive from the Darlington output stage of the CA3085 (see Fig. 2) through terminal 7. The load regulation of this circuit is typically 0.025 per cent with 0 to 3-ampere load-current variation; line regulation is typically 0.025 per cent/volt change in input voltage.



(a) with simplified short-circuit protection



(b) with auxiliary short-circuit protection

Fig. 6— High-current voltage regulator using n-p-n pass transistor.

Voltage Regulator with Low V_I-V_O Difference

In the voltage regulators described in the previous section, it is necessary to maintain a minimum difference of about 4 volts between the input and output voltages. In some applications this requirement is prohibitive. The circuit shown in Fig. 7 can deliver an output current in the order of 2 amperes with a V_I-V_O difference of only one volt.

It employs a single external p-n-p transistor having its base and emitter connected to terminals 2 and 3, respectively, of the CA3085. In this circuit, the emitter of the output transistor (Q14 in Fig. 2) in the CA3085 is returned to the negative supply rail through an external resistor (R_{SCP}) and two series-connected diodes (D1, D2). These forward-biased diodes maintain Q6 in the CA3085 within linear-mode operation. The choice of resistors R1 and R2 is made in accordance with Eq. (1). Adequate frequency compensation for this circuit is provided by the 0.01-microfarad capacitor connected between terminal 7 of the CA3085 and the negative supply rail.

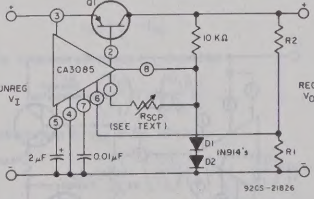


Fig. 7— Voltage regulator for low V_I – V_O difference.

Fig. 8, which shows the output impedance of the circuit of Fig. 7 as a function of frequency, illustrates the excellent ripple-rejection characteristics of this circuit at frequencies below 1 kHz. Lower output impedances at the higher frequencies can be provided by connecting an appropriate capacitor across the output voltage terminals. The addition of a capacitor will, however, degrade the ability of the system to react to transient-load conditions.

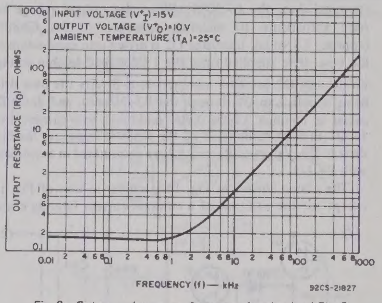


Fig. 8— Output resistance vs. frequency for circuit of Fig. 7.

High-Voltage Regulator

Fig. 9 shows a circuit that uses the CA3085 as a voltage-reference and regulator control device for high-voltage power supplies in which the voltages to be regulated are well above the input-voltage ratings of the CA3085-series circuits. The external transistors Q1 and Q2 require voltage ratings in excess of the maximum input voltage to be regulated. Series-pass transistor Q2 is controlled by the collector current of Q1, which in turn is controlled by the normally regulated current output supplied by the CA3085. The input voltage for the CA3085 regulator at terminal 3 is supplied through dropping resistor R3 and the clamping zener diode D1. The values for resistor R1 and R2 are determined in accordance with Eq. (1).

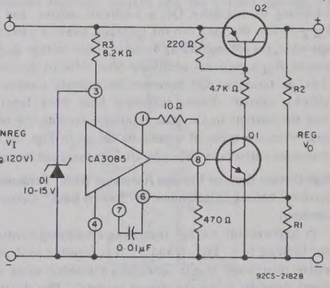


Fig. 9— High-voltage regulator.

Negative-Voltage Regulator

The CA3085 is used as a negative-supply voltage regulator in the circuit shown in Fig. 10. Transistor Q3 is the series-pass transistor. It should be noted that the CA3085 is effectively connected across the load-side of the regulated system. Diode D1 is used initially in a "circuit-starter" function; transistor Q2 "latches" D1 out of its starter-circuit function so that the CA3085 can assume its role in controlling the pass-transistor Q3 by means of Q1.

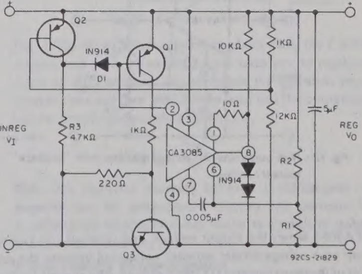


Fig. 10— Negative-voltage regulator.

Operation of the circuit is as follows: current through R3 and D1 provides base drive for Q1, which in turn provides base drive for the pass-transistor Q3. By this means operating potential for the CA3085 is developed between the collector of Q3 (terminal 4 of the CA3085) and the positive supply-rail (terminal 3 of the CA3085). When the output voltage has risen sufficiently to maintain operation of the CA3085 (approx. 7.5 volts), transistor Q2 is driven into conduction by the base drive supplied from the 1 kilohm-12 kilohm voltage divider. As Q2 becomes conductive, it diverts the base drive being supplied to Q1 through the R3-D1 path, and diode D1 ceases to conduct. Under these conditions, base-current drive to Q1 through terminal 2 of the CA3085 regulates the base drive to Q3. Values of R1 and R2 are determined in accordance with Eq. (1).

The circuit shown in Fig. 11 is similar to that of Fig. 10, except for the addition of a constant-current limiting circuit consisting of transistor Q4, a 1-kilohm resistor, and resistor R_{SCP}. When the load current increases above a particular design value, the corresponding increase in the voltage drop across resistor R_{SCP} provides additional base drive to transistor Q4. Thus, as transistor Q4 becomes increasingly conductive, its collector current diverts sufficient base drive from Q3 to limit the current in the pass transistor feeding the regulated load. With the types of transistors shown in Figs. 10 and 11, maximum currents in the order of 5 amperes can be regulated.

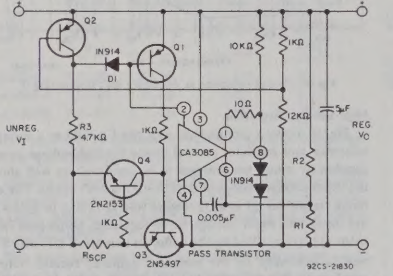


Fig. 11– Negative-voltage regulator with constant-current limiting circuit.

High-Output-Current Voltage Regulator With "Foldback" Current-Limiting (Also known as "Switch-Back" Current-Limiting)

In high-current voltage regulators employing constant-current limiting (e.g., Figs. 6 and 7), it is possible to develop excessive dissipation in the series-pass transistor when a short-circuit develops across the output terminals. This situation can be avoided by the use of the "foldback" current-limiting circuitry as shown in Fig. 12. In this circuit, terminal 8 of the CA3085 senses the output voltage, and terminal 1 is tied to a tap on a voltage-divider network connected between the emitter of the pass-transistor (Q3) and ground. The current-foldback trip-point is established by the value of resistor R_{SC}.

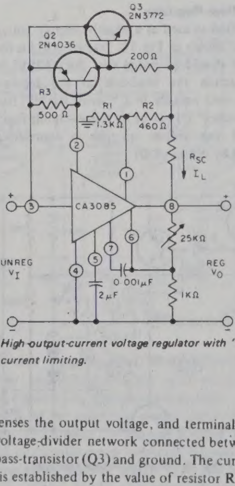


Fig. 12– High-output-current voltage regulator with "foldback" current limiting.

The protective tripping action is accomplished by forward-biasing Q15 in the CA3085 (see Fig. 2). Conditions for tripping-circuit operation are defined by the following expressions:

$$V_{BE(Q15)} = \text{(voltage at terminal 1)}-\text{(output voltage)}$$

$$= \left[(V_O + I_L R_{SC})\frac{R1}{R1 + R2}\right] - V_O \qquad (3)$$

$$\text{If } \frac{R1}{R1 + R2} = K, \text{ then}$$

$$V_{BE(Q15)} = (V_O + I_L R_{SC})\,K - V_O = KV_O + KI_L R_{SC} - V_O$$

and therefore

$$R_{SC} = \frac{V_O + V_{BE(Q15)} - KV_O}{KI_L} \qquad (4)$$

Under load short-circuit conditions, terminal 8 is forced to ground potential and current flows from the emitter of Q14 in the CA3085, establishing terminal 1 at one V_{BE}-drop [≅ 0.7 V] above ground and Q15 in a partially conducting state. The current through Q14 necessary to establish this one-V_{BE} condition is the sum of currents flowing to ground through R1 and [R2 + R_{SC}]. Normally R_{SC} is much smaller than R2 and can be ignored; therefore, the equivalent resistance R_{eq} to ground is the parallel combination of R1 and R2. The Q14 current is then given by:

$$I_{Q14} = \frac{V_{BE(Q15)}}{R_{eq}} = \frac{V_{BE(Q15)}}{\frac{R1R2}{R1 + R2}} = \frac{0.7\ [\,1.3 + 0.46\,]}{1.3 \times 0.46} = 2.06 \text{ milliamperes}$$

This current provides a voltage between terminals 2 and 3 as follows:

$$V_{2-3} = I_{Q14} \times 250 \text{ ohms} = 2.06 \times 10^{-3} \times 250 = 0.515 \text{ volt}$$

The effective resistance between terminals 2 and 3 is 250 ohms because the external 500-ohm resistor R3 is in parallel with the internal 500-ohm resistor R5. It should be understood that the V_{2-3} potential of 0.515 volt is insufficient to maintain the external p-n-p transistor Q2 in conduction, and, therefore, Q3 has no base drive. Thus the output current is reduced to zero by the protective circuitry. Fig. 13 shows the foldback characteristic typical of the circuit of Fig. 12.

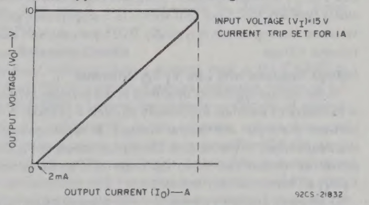


Fig. 13– Typical "foldback" current-limiting characteristic for circuit of Fig. 12.

An alternative method of providing "foldback" current-limiting is shown in Fig. 14. The operation of this circuit is similar to that of Fig. 12 except that the foldback-control transistor Q2 is external to the CA3085 to permit added flexibility in protection-circuit design.

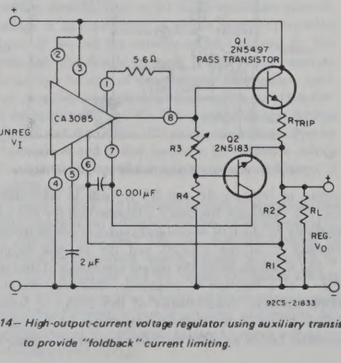


Fig. 14– High-output-current voltage regulator using auxiliary transistor to provide "foldback" current limiting.

Under low load conditions Q2 is effectively reverse-biased by a small amount, depending upon the values of R3 and R4. As the load current increases the voltage drop across R_{trip} increases, thereby raising the voltage at the base of Q1, and Q2 starts to conduct. As Q2 becomes increasingly conductive it diverts base current from transistors Q13 and Q14 in the CA3085, and thus reduces base drive to the external pass-transistor Q1 with a consequent reduction in the output voltage. The point at which current-limiting occurs, I_{trip}, is calculated as follows:

$$V_{BE(Q1)} = \text{voltage at terminal 8} - V_O \text{(assuming a low value for } R_{trip})$$

$$V_{BE(Q2)} = \text{voltage at terminal 8}\left(\frac{R4}{R3 + R4}\right) - V_O$$

$$= \left[V_O + I_L R_{trip} + V_{BE(Q1)}\right]\left[\frac{R4}{R3 + R4}\right] - V_O$$

if $K = \frac{R4}{R3 + R4}$, then the trip current is given by:

$$I_{trip} = \frac{V_{BE(Q2)} - K\left[V_O + V_{BE(Q1)}\right] + V_O}{KR_{trip}} \qquad (7)$$

In the circuit in Fig. 12 the load current goes to zero when a short circuit occurs. In the circuit of Fig. 14 the load current is significantly reduced but does not go to zero. The value for I_{SC} is computed as follows:

$$V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)}\right] R1 = V_{BE(Q1)} + I_{SC} R_{trip}$$

$$I_{SC} = \frac{V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)}\right] R1 - V_{BE(Q1)}}{R_{trip}} \qquad (8)$$

Fig. 15 shows that the transfer characteristic of the load current is essentially linear between the "trip-point" and the "short-circuit" point.

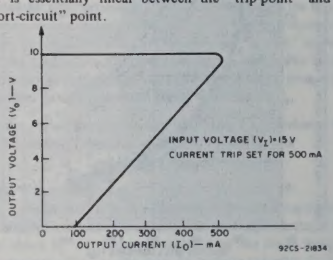


Fig. 15– Typical foldback current-limiting characteristic for circuit of Fig. 14.

High-Voltage Regulator Employing Current "Snap-Back" Protection

In high-voltage regulators (e.g., see Fig. 9), "foldback" current-limiting cannot be used safely because the high voltage across the pass transistor can cause second breakdown despite the reduction in current flow. To adequately protect the pass transistor in this type of high-voltage regulator, the so-called "snap-back" method of current limiting can be employed to reduce the current to zero in a few microseconds, and thus prevent second-breakdown destruction of the device.

The circuit diagram of a high-voltage regulator employing current "snap-back" protection is shown in Fig. 16. The basic regulator circuit is similar to that shown in Fig. 9. The additional circuitry in the circuit of Fig. 16 quickly interrupts base drive to the pass transistor in event of load fault. The point of current-trip is established as follows:

$$I_{trip} = \frac{V_{BE(Q1)}}{R_{SC}} \qquad (9)$$

Thus, when a sufficient voltage drop is developed across R_{SC}, transistor Q1 becomes conductive and current flows into the base of Q2 so that it also becomes conductive. Transistor Q3, in turn, is driven into conduction, thereby latching the Q2-Q3 combination (basic SCR action) so that it diverts (through terminal 7) base drive from the output stage (Q13, Q14) in the CA3085. By this means, base drive is diverted from Q4 and the pass transistor Q5. To restore regulator operation, normally closed switch S1 is momentarily opened and unlatches Q2-Q3.

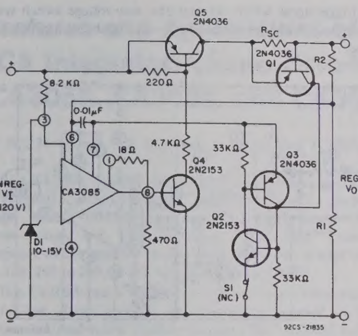
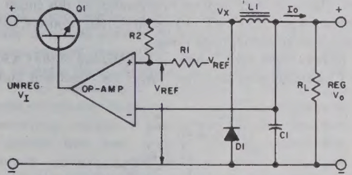


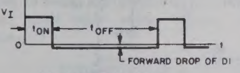
Fig. 16— High-voltage regulator incorporating current "snap-back" protection.

Switching Regulator

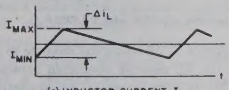
When large input-to-output voltage differences are necessary, the regulators described above are inefficient because they dissipate significant power in the series-pass transistor. Under these conditions, high-efficiency operation can be achieved by using a switching-type regulator of the generic type shown in Fig. 17(a). Transistor Q1 acts as a keyed switch and operates in either a saturated or cut-off condition to minimize dissipation. When transistor Q1 is conductive, diode D1 is reverse-biased and current in the inductance L1 increases in accordance with the following relationship:



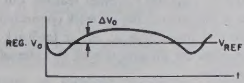
(a) SELF-OSCILLATING SWITCHING REGULATOR



(b) VOLTAGE AT POINT V_X



(c) INDUCTOR CURRENT I_{L1}



(d) OUTPUT VOLTAGE

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Fig. 17— Switching regulator and associated waveforms.

$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt \qquad (10)$$

where V is the voltage across the inductance L1. The current through the inductance charges the capacitor C1 and supplies current to the load. The output voltage rises until it slightly exceeds the reference voltage V_{ref}. At this point the op-amp removes base drive to Q1 and the unregulated input voltage V_I is "switched off". The energy stored in the inductor L1 now causes the voltage at V_x to swing in the negative direction and current flows through diode D1, while continuing to supply current into the load R_L. As the current in the inductor falls below the load current, the capacitor C1 begins to discharge and V_O decreases. When V_O falls slightly below the value of V_{ref}, the op-amp turns on Q1 and the cycle is repeated. It should be apparent that the output voltage oscillates about V_{ref} with an amplitude determined by R1 and R2. Actually, the value of V_{ref} varies from being slightly more positive than V_{ref}' when Q1 is conducting, to being slightly more negative than V_{ref}' when D1 is conducting. The voltage and current waveforms are shown in Fig. 17(b), (c), and (d).

Design Example: The following specifications are used in decomputations for a switching regulator:

$V_I = 30$ V, $V_O = 5$ V, $I_O = 500$ mA,
switching frequency = 20 kHz,
output ripple = 100 mV.

If it is assumed that transistor Q1 is in steady-state saturated operation with a low voltage-drop, the current in the inductor is given by Eq. 10, as follows:

$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt = \left(\frac{V_I - V_O}{L1}\right) t_{on} \qquad (11)$$

When transistor Q1 is off, the current in the inductor is given by:

$$i_L \cong \frac{(V_O + V_{D1})\ t_{off}}{L1} \qquad (12)$$

From Eq. 11,

$$L_1 = \frac{(V_I - V_O)}{i_L} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \qquad (13)$$

If i_{max} is 1.3 I_L, then during t_{on} the current in the inductor (i_L) will be 0.5 A x 1.3 = 0.65 A; therefore, $\Delta i_L = 0.15$ A

Substitution in Eq. 13 yields

$$L_1 = \frac{(30-5)}{0.15} \cdot \frac{1}{(20 \times 10^3)} \cdot \frac{5}{30} = 1.4 \text{ mH} \qquad (14)$$

Current discharge from the capacitor C1 is given by:

$$i_c = C\frac{dv}{dt} \qquad (15)$$

Thus, $\Delta i_c = C\frac{\Delta v}{\Delta t}$, or $C = \frac{\Delta i_c\ \Delta t}{\Delta v}$

Since $i_c = i_L$ and $\Delta t = t_{off}$, then

$$C = \frac{\Delta i_L\ t_{off}}{\Delta v}$$

Substitution for the value of i_L from Eq. 13 yields

$$C = \frac{\left(\frac{V_I - V_O}{L1}\right) \cdot \frac{1}{f} \cdot \left(\frac{V_O}{V_I}\right) \cdot t_{off}}{\Delta v} \qquad (16)$$

The total period $T = t_{off} + t_{on}$, and $T = \frac{1}{f}$. Therefore,

$$t_{off} = \frac{1}{f} - t_{on} \qquad (17)$$

For optimum efficiency t_{on} should be

$$\cong \left(\frac{V_O}{V_I}\right) T \cong \left(\frac{V_O}{V_I}\right)\frac{1}{f} \qquad (18)$$

Substitution for t_{on} in Eq. 18 yields

$$t_{off} = \frac{1}{f} - \left(\frac{V_O}{V_I}\right)\frac{1}{f} = \frac{1}{f}\left(1 - \frac{V_O}{V_I}\right) \qquad (19)$$

Substitution for t_{off} in Eq. 16 yields

$$C = \frac{\frac{(V_I - V_O)}{L_1} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \cdot \frac{1}{f} \cdot \left(1 - \frac{V_O}{V_I}\right)}{\Delta v}$$

Substitution of numerical values in Eq. 20 produces the following value for C:

$$C = \frac{\frac{30-5}{1.4 \times 10^{-3}} \cdot \frac{1}{20 \times 10^3} \cdot \frac{5}{30} \cdot \frac{1}{20 \times 10^3} \cdot \left(1 - \frac{5}{30}\right)}{10^{-1}} = 63\ \mu F$$

A switching-regulator circuit using the CA3085 is shown in Fig. 18. The values of L and C (1.5 millihenries and 50 microfarads, respectively) are commercially available components having values approximately equal to the computed values in the previous design example.

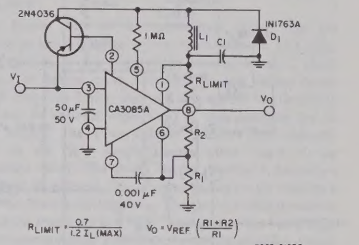
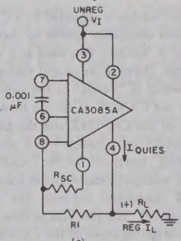


Fig. 18— Typical switching regulator circuit.

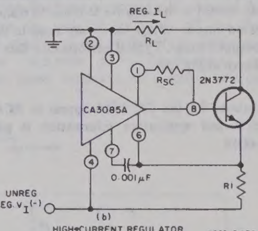
Current Regulators

The CA3085 series of voltage regulators can be used to provide a constant source or sink current. A regulated-current supply capable of delivering up to 100 milliamperes is shown in Fig. 19(a). The regulated load current is controlled by R1 because the current flowing through this resistor must establish a voltage difference between terminals 6 and 4 that is equal to the internal reference voltage developed between terminals 5 and 4. The actual regulated current, reg I_L, is the sum of the quiescent regulator current and the current through R1, i.e.,

$$\text{reg } I_L = I_{quiescent} + I_{R1}$$



(a)
CURRENT REGULATOR



(b)
HIGH-CURRENT REGULATOR

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Fig. 19— Constant current regulators.

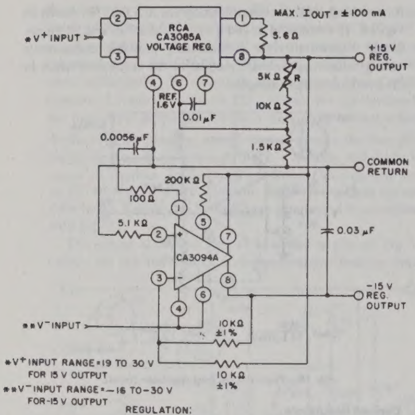
Fig. 19(b) shows a high-current regulator using the CA3085 in conjunction with an external n-p-n transistor to regulate currents up to 3 amperes. In this circuit the quiescent regulator current does not flow through the load and the output current can be directly programmed by R1, i.e.,

$$\text{Reg } I_L = \frac{V_{ref}}{R1}$$

With this regulator currents between 1 milliampere and 3 amperes can be programmed directly. At currents below 1 milliampere inaccuracies may occur as a result of leakage in the external transistor.

A Dual-Tracking Voltage Regulator

A dual-tracking voltage regulator using a CA3085 and a CA3094A* is shown in Fig. 20. The CA3094A is basically an op-amp capable of supplying 100 milliamperes of output current.



*V+ INPUT RANGE = 19 TO 30 V FOR 15 V OUTPUT

**V- INPUT RANGE = -16 TO -30 V FOR -15 V OUTPUT

REGULATION:

MAX. LINE = $\dfrac{\Delta V_{OUT}}{[V_{OUT}(\text{INITIAL})]\,\Delta V_{IN}} \times 100 = 0.075\%/V$

MAX. LOAD = $\dfrac{\Delta V_{OUT}}{V_{OUT}(\text{INITIAL})} \times 100 = 0.075\%\ V_{OUT}$

(I_L FROM 1 TO 50 mA)

92CM-20560

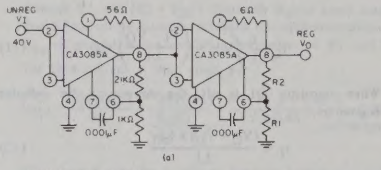
Fig. 20– Dual-voltage tracking regulator.

The positive output voltage is regulated by a CA3085 operating in a configuration essentially similar to that described in connection with Fig. 3. Resistor R is used as a vernier adjustment of output voltage. The negative output voltage is regulated by the CA3094A, which is "slaved" to the regulated positive voltage supplied by the CA3085. It should be noted that the non-inverting input of the CA3094A and the negative supply terminal of the CA3085 are connected to a common ground reference. The "slaving" potential for the CA3094A is derived from an accurate 1:1 voltage-divider network comprised of two 10-kilohm resistors connected between the +15-volt and –15-volt output terminals. The junction of these two resistors is connected to the inverting input of the CA3094A. The voltage at this junction is compared with the voltage at the non-inverting input, and the CA3094A then automatically adjusts the output current at the negative terminal to maintain a negative regulated output voltage essentially equal to the regulated positive output voltage. Typical performance data for this circuit are shown in Fig. 20.

The basic circuit of Fig. 20 can be modified to regulate dissimilar positive and negative voltages (e.g., +15 V, –5 V) by appropriate selection of resistor ratios in the voltage-divider network discussed previously. As an example, to provide tracking of the +15 V and –5 V regulated voltages with the circuit of Fig. 20, it is only necessary to replace the 10-kilohm resistor connected between terminals 3 and 8 of the CA3094A with a 3.3-kilohm resistor.

Regulators With High Ripple Rejection

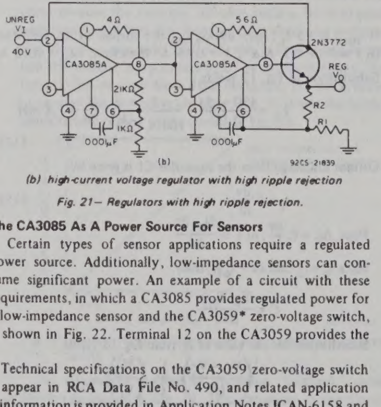
When the reference-voltage source in the CA3085 is adequately filtered, the typical ripple rejection provided by the circuit is 56 dB. It is possible to achieve higher ripple-rejection performance by cascading two stages of the CA3085, as shown in Fig. 21. The voltage-regulator circuit in Fig. 21(a) provides 90 dB of ripple rejection. The output voltage is adjustable over the range from 1.8 to 30 volts by appropriate adjustment of resistors R1 and R2. Higher regulated output currents up to 1 ampere can be obtained with this circuit by adding an external n-p-n transistor as shown in Fig. 21(b).



(a)

90 dB RIPPLE REJECTION
LINE REG <0.0001%/V_I
LOAD REG <0.1% V_O FOR LOAD CURRENTS UP TO 50 mA
V_O RANGE FROM 1.8 V TO 30 V

(a) voltage regulator with high ripple rejection



(b) high-current voltage regulator with high ripple rejection

Fig. 21– Regulators with high ripple rejection.

The CA3085 As A Power Source For Sensors

Certain types of sensor applications require a regulated power source. Additionally, low-impedance sensors can consume significant power. An example of a circuit with these requirements, in which a CA3085 provides regulated power for a low-impedance sensor and the CA3059* zero-voltage switch, is shown in Fig. 22. Terminal 12 on the CA3059 provides the ac trigger-signal which actuates the zero-voltage switch synchronously with the power line to control the load-switching triac.

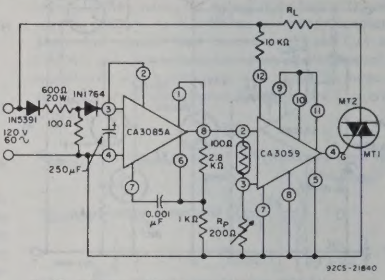


Fig. 22– Voltage regulator for sensor and zero-voltage switch.

The CA3085 As A General-Purpose Amplifier

As described above, the CA3085 series regulators contain a high-gain linear amplifier having a current-output capability up to 100 milliamperes. The premium type (CA3085B) can operate at supply voltages up to 50 volts. When equipped with an appropriate radiator or heat-sink, the TO-5 package of these devices can dissipate up to 1.6 watts at 55°C. A very stable internal voltage-reference source is used to bias the high-gain amplifier and/or provide an external voltage-reference despite extreme temperature or supply-voltage variations. These factors, plus economics, prompt consideration of this circuit for general-purpose uses, such as amplifiers, relay controls, signal-lamp controls, and thyristor firing.

As an example, Fig. 23 shows the application of the CA3085 in a general-purpose amplifier. Under the conditions shown, the circuit has a typical gain of 70 dB with a flat response to at least 100 kHz without the RC network connected between terminals 6 and 7. The RC network is useful as a tone control or to "roll-off" the amplifier response for other reasons. Current limiting is not used in this circuit. The network connected between terminals 8 and 6 provides both dc and ac feedback. This circuit is also applicable for directly driving an external discrete n-p-n power transistor.

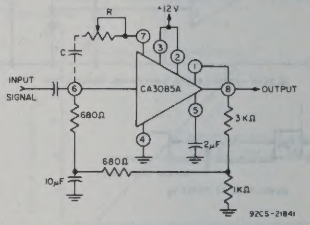


Fig. 23– General purpose amplifier using CA3085A.

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* Specifications for the CA3094A appear in RCA Data File No. 598 and application information is presented in ICAN-6048.

* Technical specifications on the CA3059 zero-voltage switch appear in RCA Data File No. 490, and related application information is provided in Application Notes ICAN-6158 and ICAN-6268.

Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)

by A.C.N. Sheng, G.J. Granieri, J. Yellin, and T. McNulty

RCA-CA3058, CA3059 and CA3079 zero-voltage switches are monolithic integrated circuits designed primarily for use as trigger circuits for thyristors in many highly diverse ac power-control and power-switching applications. These integrated-circuit switches operate from an ac input voltage of 24, 120, 208 to 230, or 277 volts at 50, 60, or 400 Hz.

The CA3059 and CA3079 are supplied in a 14-terminal dual-in-line plastic package. The CA3058 is supplied in a 14-terminal dual-in-line ceramic package. The electrical and physical characteristics of each type are detailed in RCA Data Bulletin File No. 490.

RCA zero-voltage switches (ZVS) are particularly well suited for use as thyristor trigger circuits. These switches trigger the thyristors at zero-voltage points in the supply-voltage cycle. Consequently, transient load-current surges and radio-frequency interference (RFI) are substantially reduced. In addition, use of the zero-voltage switches also reduces the rate of change of on-state current (di/dt) in the thyristor being triggered, an important consideration in the operation of thyristors. These switches can be adapted for use in a variety of control functions by use of an internal differential comparator to detect the difference between two externally developed voltages. In addition, the availability of numerous terminal connections to internal circuit points greatly increases circuit flexibility and further expands the types of ac power-control applications to which these integrated circuits may be adapted. The excellent versatility of the zero-voltage switches is demonstrated by the fact that these circuits have been used to provide transient-free temperature control in self-cleaning ovens, to control gun-muzzle temperature in low-temperature environments, to provide sequential switching of heating elements in warm-air furnaces, to switch traffic signal lights at street intersections, and to effect other widely different ac power-control functions.

FUNCTIONAL DESCRIPTION

RCA zero-voltage switches are multistage circuits that employ a diode limiter, a zero-crossing (threshold) detector, an on-off sensing amplifier (differential comparator), and a Darlington output driver (thyristor gating circuit) to provide the basic switching action. The dc operating voltages for these stages is provided by an internal power supply that has sufficient current capability to drive external circuit elements, such as transistors and other integrated circuits. An important feature of the zero-voltage switches is that the output trigger pulses can be applied directly to the gate of a triac or a silicon controlled rectifier (SCR). The CA3058 and CA3059 also feature an interlock (protection) circuit that inhibits the application of these pulses to the thyristor in the event that the external sensor should be inadvertently opened or shorted. An external inhibit connection (terminal No. 1) is also available so that an external signal can be used to inhibit the output drive. This feature is not included in the CA3079; otherwise, the three integrated-circuit zero-voltage switches are electrically identical.

Over-all Circuit Operation

Fig. 1 shows the functional interrelation of the zero-voltage switch, the external sensor, the thyristor being triggered, and the load elements in an on-off type of ac power-control system. As shown, each of the zero-voltage switches incorporates four functional blocks as follows:

(1) Limiter-Power Supply – Permits operation directly from an ac line.

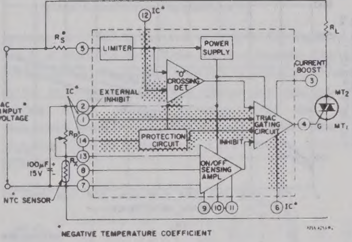
(2) Differential On/Off Sensing Amplifier – Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.

(3) Zero-Crossing Detector – Synchronizes the output pulses of the circuit at the time when the ac cycle is at a zero-voltage point and thereby eliminates radio-frequency inteference (RFI) when used with resistive loads.

(4) Triac Gating Circuit – Provides high-current pulses to the gate of the power-controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (shown in Fig. 1):

(1) A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

Fig. 1 – Functional block diagrams of the zero-voltage switches CA3058, CA3059, and CA3079.

(2) Thyristor firing may be inhibited through the action of an internal diode gate connected to terminal 1.

(3) High-power dc-comparator operation is provided by overriding the action of the zero-crossing detector. This override is accomplished by connecting terminal 12 to terminal 7. Gate current to the thyristor is continuous when terminal 13 is positive with respect to terminal 9.

Fig. 2 shows the detailed circuit diagram for the integrated-circuit zero-voltage switches. (The diagrams shown in Figs. 1 and 2 are representative of all three RCA zero-voltage switches, i.e., the CA3058, CA3059, and CA3079; the shaded areas indicate the circuitry that is not included in the CA3079.)

The limiter stage of the zero-voltage switch clips the incoming ac line voltage to approximately ±8 volts. This signal is then applied to the zero-voltage-crossing detector, which generates an output pulse each time the line voltage passes through zero. The limiter output is also applied to a rectifying diode and an external capacitor, C_F, that comprise the dc power supply. The power supply provides approximately 6 volts as the V_{CC} supply to the other stages of the zero-voltage switch. The on-off sensing amplifier is basically a differential comparator. The thyristor gating circuit contains a driver for direct triac triggering. The gating circuit is enabled when all the inputs are at a "high" voltage, i.e., the line voltage must be approximately zero volts, the sensing-amplifier output must be "high," the external voltage to terminal 1 must be a logical "0", and, for the CA3058 and CA3059, the output of the fail-safe circuit must be "high." Under these conditions, the thyristor (triac or SCR) is triggered when the line voltage is essentially zero volts.

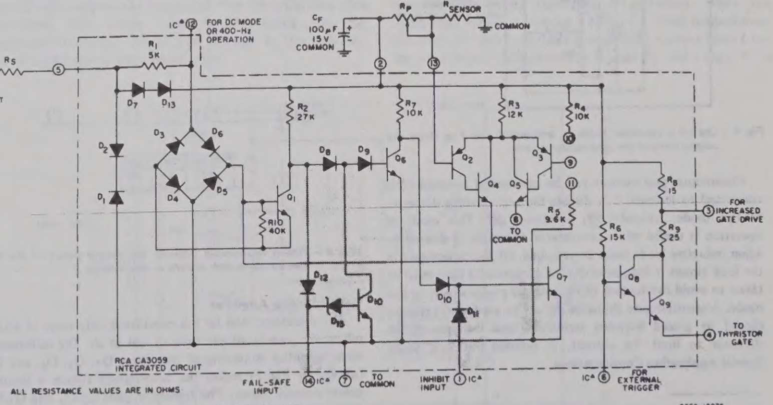
Thyristor Triggering Circuits

The diodes D_1 and D_2 in Fig. 2 form a symmetrical clamp that limits the voltages on the chip to ±8 volts; the diodes D_7 and D_{13} form a half-wave rectifier that develops a positive voltage on the external storage capacitor, C_F.

The output pulses used to trigger the power-switching thyristor are actually developed by the zero-crossing detector and the thyristor gating circuit. The zero-crossing detector consists of diodes D_3 through D_6, transistor Q_1, and the associated resistors shown in Fig. 2. Transistors Q_1 and Q_6 through Q_9 and the associated resistors comprise the thyristor gating circuit and output driver. These circuits generate the output pulses when the ac input is at a zero-voltage point so that RFI is virtually eliminated when the zero-voltage switch and thyristor are used with resistive loads.

The operation of the zero-crossing detector and thyristor gating circuit can be explained more easily if the on state (i.e., the operating state in which current is being delivered to the thyristor gate through terminal 4) is considered as the operating condition of the gating circuit. Other circuit elements in the zero-voltage switch inhibit the gating circuit unless certain conditions are met, as explained later.

In the on state of the thyristor gating circuit, transistors Q_8 and Q_9 are conducting, transistor Q_7 is off, and transistor Q_6 is on. Any action that turns on transistor Q_7 removes the drive from transistor Q_8 and thereby turns off the thyristor. Transistor Q_7 may be turned on directly by application of a minimum of ±1.2 volts at 10 microamperes to the external-inhibit input, terminal 1. (If a voltage of more than



ALL RESISTANCE VALUES ARE IN OHMS

NOTE: CIRCUITRY, WITHIN SHADED AREAS, NOT INCLUDED IN CA3079

*IC = INTERNAL CONNECTION -- DO NOT USE (TERMINAL RESTRICTION APPLIES ONLY TO CA3079)

Fig. 2 – Schematic diagram of zero-voltage switches CA3058, CA3059, and CA3079.

1.5 volts is available, an external resistance must be added in series with terminal 1 to limit the current to 1 milliampere.) Diode D_{10} isolates the base of transistor Q_7 from other signals when an external-inhibit signal is applied so that this signal is the highest priority command for normal operation. (Although grounding of terminal 6 creates a higher-priority inhibit function, this level is not compatible with normal DTL or TTL logic levels.) Transistor Q_7 may also be activated by turning off transistor Q_6 to allow current flow from the power supply through resistor R_7 and diode D_{10} into the base of Q_7. Transistor Q_6 is normally maintained in conduction by current that flows into its base through resistor R_2 and diodes D_8 and D_9 when transistor Q_1 is off.

Transistor Q_1 is a portion of the zero-crossing detector. When the voltage at terminal 5 is greater than +3 volts, current can flow through resistor R_1, diode D_6, the base-to-emitter junction of transistor Q_1, and diode D_4 to terminal 7 to turn on Q_1. This action inhibits the delivery of a gate-drive output signal at terminal 4. For negative voltages at terminal 5 that have magnitudes greater than 3 volts, the current flows through diode D_5, the emitter-to-base junction of transistor Q_1, diode D_3, and resistor R_1, and again turns on transistor Q_1. Transistor Q_1 is off only when the voltage at terminal 5 is less than the threshold voltage of approximately ±2 volts. When the integrated-circuit zero-voltage switch is connected as shown in Fig. 1, therefore, the output is a narrow pulse which is approximately centered about the zero-voltage time in the cycle, as shown in Fig. 3. In some applications, however, particularly those that use either slightly inductive or low-power loads, the thyristor load current does not reach the latching-current value* by the end of this pulse. An external capacitor C_X connected between terminal 5 and 7, as shown in Fig. 4, can be used to delay the pulse to accommodate such loads. The amount of pulse stretching and delay is shown in Figs. 5(a) and 5(b).

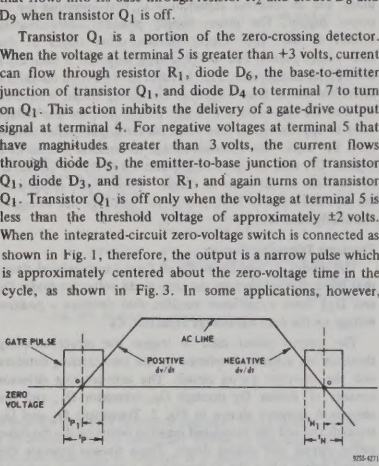


Fig. 3 – Waveform showing output-pulse duration of the zero-voltage switch.

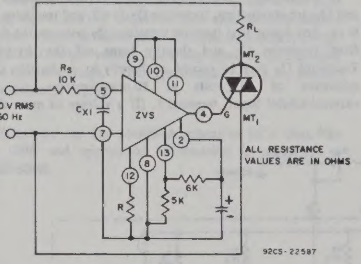


Fig. 4 – Use of a capacitor between terminals 5 and 7 to delay the output pulse of the zero-voltage switch.

Continuous gate current can be obtained if terminal 12 is connected to terminal 7 to disable the zero-crossing detector. In this mode, transistor Q_1 is always off. This mode of operation is useful when comparator operation is desired or when inductive loads must be switched. (If the capacitance in the load circuit is low, most RFI is eliminated.) Care must be taken to avoid overloading of the internal power supply in this mode. A sensitive-gate thyristor should be used, and a resistor should be placed between terminal 4 and the gate of the thyristor to limit the current, as pointed out later under **Special Application Considerations.**

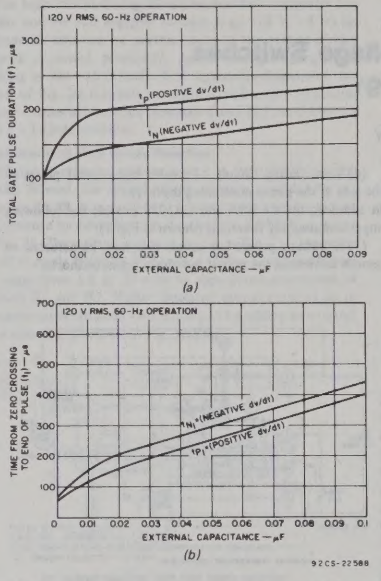
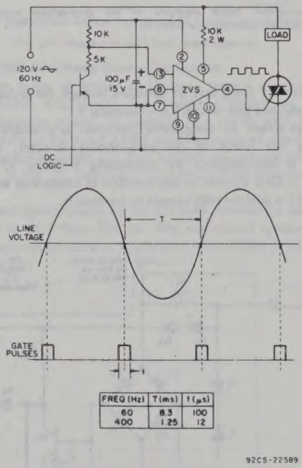


Fig. 5 – Curves showing effect of external capacitance on (a) the total output-pulse duration, and (b) the time from zero crossing to the end of the pulse.

Fig. 6 indicates the timing relationship between the line voltage and the zero-voltage- switch output pulses. At 60 Hz, the pulse is typically 100 microseconds wide; at 400 Hz, the pulse width is typically 12 microseconds. In the basic circuit shown, when the dc logic signal is "high", the output is disabled; when it is "low", the gate pulses are enabled.



FREQ (Hz)	T (ms)	t (μs)
60	8.3	100
400	1.25	12

Fig. 6 – Timing relationship between the output pulses of the RCA zero-voltage switch and the ac line voltage.

On-Off Sensing Amplifier

The discussion thus far has considered only cases in which pulses are present all the time or not at all. The differential sense amplifier consisting of transistors Q_2, Q_3, Q_4, and Q_5 (shown in Fig. 2) makes the zero-voltage switch a flexible power-control circuit. The transistor pairs Q_2-Q_4 and Q_3-Q_5 form a high-beta composite p-n-p transistors in which the emitters of transistors Q_4 and Q_5 act as the collectors of the composite devices. These two composite transistors are connected as a differential amplifier with resistor R_3 acting as a constant-current source. The relative current flow in the two "collectors" is a function of the difference in voltage between the bases of transistors Q_2 and Q_3. Therefore, when terminal 13 is more positive than terminal 9, little or no current flows in the "collector" of the transistor pair Q_2-Q_4. When terminal 13 is negative with respect to terminal 9, most of the current flows through that path, and none in terminal 8. When current flows in the transistor pair Q_2-Q_4, the path is from the supply through R_3, through the transistor pair Q_2-Q_4, through the base-emitter junction of transistor Q_1, and finally through the diode D_4 to terminal 7. Therefore, when V_{13} is equal to or more negative than V_9, transistor Q_1 is on, and the output is inhibited.

In the circuit shown in Fig. 1, the voltage at terminal 9 is derived from the supply by connection of terminals 10 and 11 to form a precision voltage divider. This divider forms one side of a transducer bridge, and the potentiometer R_p and the negative-temperature-coefficient (NTC) sensor form the other side. At low temperatures, the high resistance of the sensor causes terminal 13 to be positive with respect to terminal 9 so that the thyristor fires on every half-cycle, and power is applied to the load. As the temperature increases, the sensor resistance decreases until a balance is reached, and V_{13} approaches V_9. At this point, the transistor pair Q_2-Q_4 turns on and inhibits any further pulses. The controlled temperature is adjusted by variation of the value of the potentiometer R_p. For cooling service, either the positions of R_p and the sensor may be reversed or terminals 9 and 13 may be interchanged.

The low bias current of the sensing amplifier permits operation with sensor impedances of up to 0.1 megohm at balance without introduction of substantial error (i.e., greater than 5 per cent). The error may be reduced if the internal bridge elements, resistors R_4 and R_5, are not used, but are replaced with resistances which equal the sensor impedance. The minimum value of sensor impedance is restricted by the current drain on the internal power supply. Operation of the zero-voltage switch with low-impedance sensors is discussed later under **Special Application Considerations.** The voltage applied to terminal 13 must be greater than 1.8 volts at all times to assure proper operation.

Protection Circuit

A special feature of the CA3058 and CA3059 zero-voltage switches is the inclusion of an interlock type of circuit. This circuit removes power from the load by interrupting the thyristor gate drive if the sensor either shorts or opens. However, use of this circuit places certain constraints upon the user. Specifically, effective protection-circuit operation is dependent upon the following conditions:

(1) The circuit configuration of Fig. 1 is used, with an internal supply, no external load on the supply, and terminal 14 connected to terminal 13.

(2) The value of potentiometer R_p and of the sensor resistance must be between 2000 ohms and 0.1 megohm.

(3) The ratio of sensor resistance and R_p must be greater than 0.33 and less than 3.0 for all normal conditions. (If either of these ratios is not met with an unmodified sensor, a series resistor or a shunt resistor must be added to avoid undesired activation of the circuit.)

The protective feature may be applied to other systems when operation of the circuit is understood. The protection circuit consists of diodes D_{12} and D_{15} and transistor Q_{10}. Diode D_{12} activates the protection circuit if the sensor shown in Fig. 1 shorts or its resistance drops too low in value, as follows: Transistor Q_6 is on during an output pulse so that the junction of diodes D_8 and D_{12} is 3 diode drops (approximately 2 volts) above terminal 7. As long as V_{14} is more positive or only 0.15 volt negative with respect to that point, diode D_{12} does not conduct, and the circuit operates normally. If the voltage at terminal 14 drops to 1 volt, the anode of diode D_8 can have a potential of only 1.6 to 1.7 volts, and current does not flow through diodes D_8 and D_9 and transistor Q_6. The thyristor then turns off.

The actual threshold is approximately 1.2 volts at room temperature, but decreases 4 millivolts per degree C at higher temperatures. As the sensor resistance increases, the voltage at terminal 14 rises toward the supply voltage. At a voltage of approximately 6 volts, the zener diode D_{15} breaks down and turns on transistor Q_{10}, which then turns off transistor Q_6 and the thyristor. If the supply voltage is not at least 0.2 volt more positive than the breakdown voltage of diode D_{15}, activation of the protection circuit is not possible. For this reason, loading the internal supply may cause this circuit to malfunction, as may selection of the wrong external supply voltage. Fig. 7 shows a guide for the proper operation of the protection circuit when an external supply is used with a typical integrated-circuit zero-voltage switch.

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* The latching current is the minimum current required to sustain conduction immediately after the thyristor is switched from the off to the on state and the gate signal is removed.

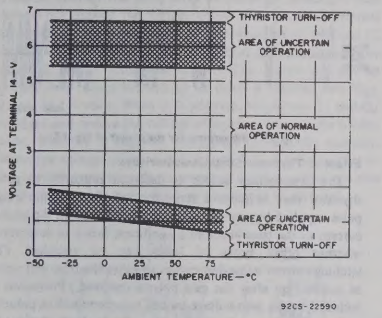


Fig. 7 – Operating regions for built-in protection circuits of a typical zero-voltage switch.

SPECIAL APPLICATION CONSIDERATIONS

As pointed out previously, the RCA integrated-circuit zero-voltage switches (CA3058, CA3059, and CA3079) are exceptionally versatile units that can be adapted for use in a wide-variety of power-control applications. Full advantage of this versatility can be realized, however, only if the user has a basic understanding of several fundamental considerations that apply to certain types of applications of the zero-voltage switches.

Operating-Power Options

Power to the zero-voltage switch may be derived directly from the ac line, as shown in Fig. 1, or from an external dc power supply connected between terminals 2 and 7, as shown in Fig. 8. When the zero-voltage switch is operated directly from the ac line, a dropping resistor R_S of 5,000 to 10,000 ohms must be connected in series with terminal 5 to limit the current in the switch circuit. The optimum value for this resistor is a function of the average current drawn from the internal dc power supply, either by external circuit elements or by the thyristor trigger circuits, as shown in Fig. 9. The chart shown in Fig. 1 indicates the value and dissipation rating of the resistor R_S for ac line voltages of 24, 120, 208 to 230, and 277 volts.

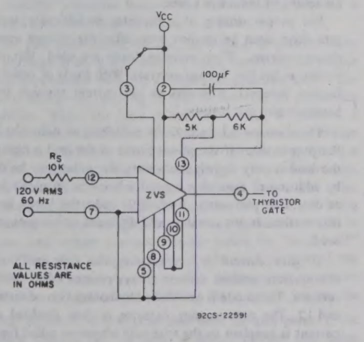


Fig. 8 – Operation of the zero-voltage switch from an external dc power supply connected between terminals 2 and 7.

Half-Cycling Effect

The method by which the zero-voltage switch senses the zero crossing of the ac power results in a half-cycling phenomenon at the control point. Fig. 10 illustrates this phenomenon. The zero-voltage switch senses the zero-voltage

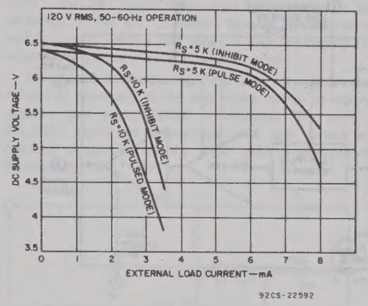


Fig. 9 – DC supply voltage as a function of external load current for several values of dropping resistance R_S.

crossing every half-cycle, and an output, for example pulse No. 4, is produced to indicate the zero crossing. During the remaining 8.3 milliseconds, however, the differential amplifier in the zero-voltage switch may change state and inhibit any further output pulses. The uncertainity region of the differential amplifier, therefore, prevents pulse No. 5 from triggering the triac during the negative excursion of the ac line voltage.

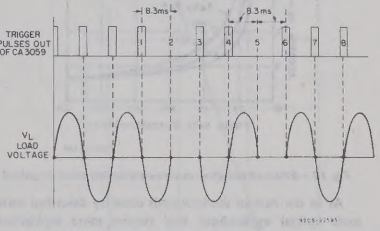
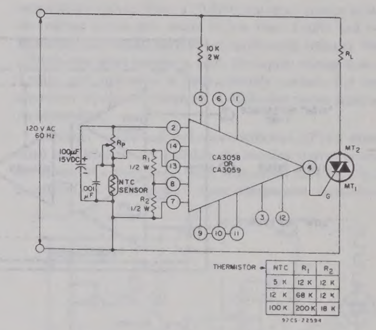


Fig. 10 – Half-cycling phenomenon in the zero-voltage switch.

When a sensor with low sensitivity is used in the circuit, the zero-voltage switch is very likely to operate in the linear mode. In this mode, the output trigger current may be sufficient to trigger the triac on the positive-going cycle, but insufficient to trigger the device on the negative-going cycle of the triac supply voltage. This effect introduces a half-cycling phenomenon, i.e., the triac is turned on during the positive half-cycle and turned off during the negative half-cycle.

Several techniques may be used to cope with the half-cycling phenomenon. If the user can tolerate some hystersis in the control, then positive feedback can be added around the differential amplifier. Fig. 11 illustrates this technique. The tabular data in the figure lists the recommended values of resistors R_1 and R_2 for different sensor impedances at the control point.



NTC	R_1	R_2
5 K	12 K	12 K
12 K	68 K	12 K
100 K	200 K	18 K

Fig. 11 – CA3058 or CA3059 on-off controller with hysteresis.

If a significant amount (greater than ±10%) of controlled hysteresis is required, then the circuit shown in Fig. 12 may be employed. In this configuration, external transistor Q_1 can be used to provide an auxiliary timed-delay function.

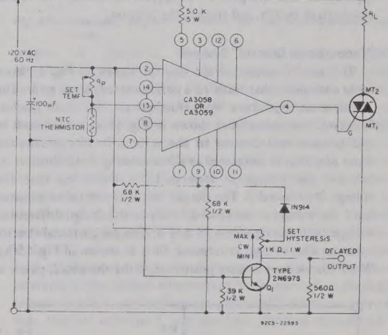


Fig. 12 – CA3058 or CA3059 on-off controller with controlled hysteresis.

For applications that require complete elimination of half-cycling without the addition of hysteresis, the circuit shown in Fig. 13 may be employed. This circuit uses a CA3098E integrated-circuit programmable comparator with a zero-voltage switch. A block diagram of CA3098E is shown in Fig. 14. Because the CA3098E contains an integral flip-flop, its output will be in either a "0" or "1" state. Consequently the zero-voltage switch cannot operate in the linear mode, and spurious half-cycling operation is prevented. When the signal-input voltage at terminal 8 of the CA3098E is equal to or less than the "low" reference voltage (LR), current flows from the power supply through resistor R_1 and R_2, and a logic "0" is

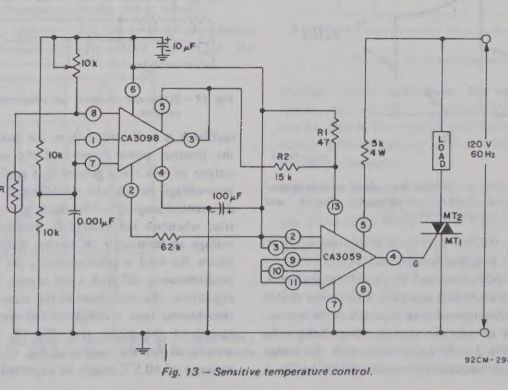


Fig. 13 – Sensitive temperature control.

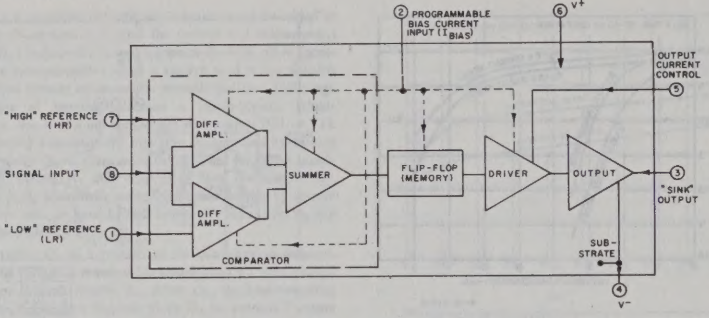


Fig. 14 – Block diagram of CA3098 programmable Schmitt trigger.

applied to terminal 13 of the zero-voltage switch. This condition turns off the triac. The triac remains off until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop so that a logic "1" is applied to terminal 13 of the zero-voltage switch, and triggers the triac on.

"Proportional Control" Systems

The on-off nature of the control shown in Fig. 1 causes some overshoot that leads to a definite steady-state error. The addition of hysteresis adds further to this error factor. However, the connections shown in Fig. 15(a) can be used to add proportional control to the system. In this circuit, the sense amplifier is connected as a free-running multivibrator. At balance, the voltage at terminal 13 is much less than the voltage at terminal 9. The output will be inhibited at all times until the voltage at terminal 13 rises to the design differential voltage between terminals 13 and 9; then proportional control resumes. The voltage at terminal 13 is as shown in Fig. 15(b). When this voltage is more positive than the threshold, power is applied to the load so that the duty cycle is approximately 50 per cent. With a 0.1 megohm sensor and values of R_p = 0.1 megohm, R_2 = 10,000 ohms, and C_{EXT} = 10 microfarads, a period greater than 3 seconds is achieved. This period should be much shorter than the thermal time constant of the system. A change in the value of any of these elements changes the period, as shown in Fig. 16. As the resistance of the sensor changes, the voltage on terminal 13 moves relative to V_9. A cooling sensor moves V_{13} in a positive direction. The triac is on for a larger portion of the pulse cycle and increases the average power to the load.

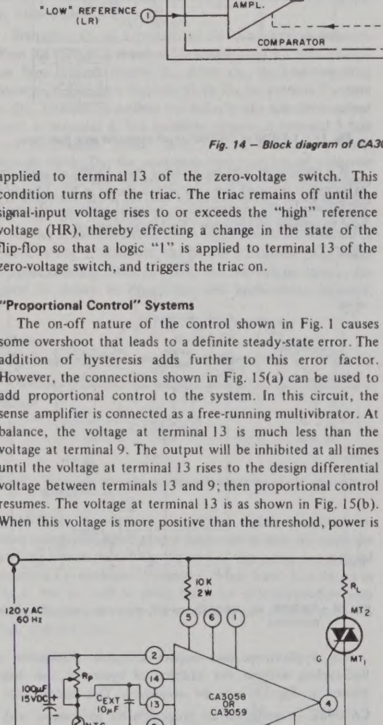


Fig. 15 – Use of the CA3058 or CA3059 in a typical heating control with proportional control: (a) schematic diagram, and (b) waveform of voltage at terminal 13.

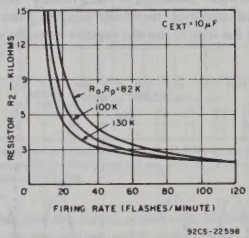


Fig. 16 – Effect of variations in time-constant elements on period.

As in the case of the hysteresis circuitry described earlier, some special applications may require more sophisticated systems to achieve either very precise regions of control or very long periods.

Zero-voltage switching control can be extended to applications in which it is desirable to have constant control of the temperature and a minimization of system hysteresis. A closed-loop top-burner control in which the temperature of the cooking utensil is sensed and maintained at a particular value is a good example of such an application; the circuit for this control is shown in Fig. 17. In this circuit, a unijunction oscillator is outboarded from the basic control by means of the internal power supply of the zero-voltage switch. The output of this ramp generator is applied to terminal 9 of the zero-voltage switch and establishes a varied reference to the differential amplifier. Therefore, gate pulses are applied to the triac whenever the voltage at terminal 13 is greater than the voltage at terminal 9. A varying duty cycle is established in which the load is predominantly on with a cold sensor and predominantly off with a hot sensor. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system but longer than the period of the 60-Hz line. Fig. 18, which contains various waveforms for the system of Fig. 17, indicates that a typical variance of ±0.5°C might be expected at the sensor contact to the utensil. Overshoot of the set temperature is minimized with this approach, and scorching of any type is minimized.

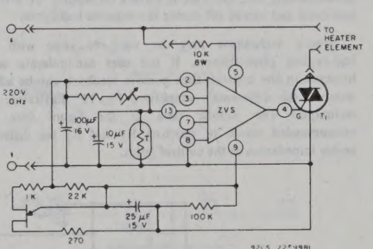


Fig. 17 – Schematic diagram of proportional zero-voltage-switching control.

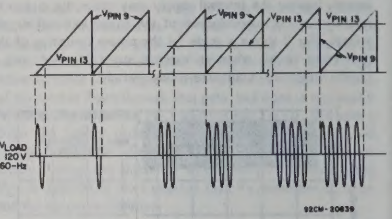


Fig. 18 – Waveforms for the circuit of Fig. 17.

Effect of Thyristor Load Characteristics

The zero-voltage switch is designed primarily to gate a thyristor that switches a resistive load. Because the output pulse supplied by the switch is of short duration, the latching current of the triac becomes a significant factor in determining whether other types of loads can be switched. (The latching-current value determines whether the triac will remain in conduction after the gate pulse is removed.) Provisions are included in the zero-voltage switch to accommodate inductive loads and low-power loads. For example, for loads that are less than approximately 4 amperes rms or that are slightly inductive, it is possible to retard the output pulse with respect to the zero-voltage crossing by insertion of the capacitor C_x from terminal 5 to terminal 7. The insertion of capacitor C_x permits switching of triac loads that have a slight inductive component and that are greater than approximately 200 watts (for operation from an ac line voltage of 120 volts rms). However, for loads less than 200 watts (for example, 70 watts), it is recommended that the user employ the T2300B* sensitive-gate triac with the zero-voltage switch because of the low latching-current requirement of this triac.

For loads that have a low power factor, such as a solenoid valve, the user may operate the zero-voltage switch in the dc mode. In this mode, terminal 12 is connected to terminal 7, and the zero-crossing detector is inhibited. Whether a "high" or "low" voltage is produced at terminal 4 is then dependent only upon the state of the differential comparator within the integrated-circuit zero-voltage switch, and not upon the zero crossing of the incoming line voltage. Of course, in this mode of operation, the zero-voltage switch no longer operates as a zero-voltage switch. However, for many applications that involve the switching of low-current inductive loads, the amount of RFI generated can frequently be tolerated.

For switching of high-current inductive loads, which must be turned on at zero line current, the triggering technique employed in the dual-output over-under temperature controller and the transient-free switch controller described subsequently in this Note is recommended.

Switching of Inductive Loads

For proper driving of a thyristor in full-cycle operation, gate drive must be applied soon after the voltage across the device reverses. When resistive loads are used, this reversal occurs as the line voltage reverses. With loads of other power factors, however, it occurs as the current through the load becomes zero and reverses.

There are several methods for switching an inductive load at the proper time. If the power factor of the load is high (i.e., if the load is only slightly inductive), the pulse may be delayed by addition of a suitable capacitor between terminals 5 and 7, as described previously. For highly inductive loads, however, this method is not suitable, and different techniques must be used.

If gate current is continuous, the triac automatically commutates because drive is always present when the voltage reverses. This mode is established by connection of terminals 7 and 12. The zero-crossing detector is then disabled so that current is supplied to the triac gate whenever called for by the sensing amplifier. Although the RFI-eliminating function of the zero-voltage switch is inhibited when the zero-crossing detector is disabled, there is no problem if the load is highly inductive because the current in the load cannot change abruptly.

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* Formerly RCA 40526

Circuits that use a sensitive-gate triac to shift the firing point of the power triac by approximately 90 degrees have been designed. If the primary load is inductive, this phase shift corresponds to firing at zero current in the load. However, changes in the power factor of the load or tolerances of components will cause errors in this firing time.

The circuit shown in Fig. 19 uses a CA3086 integrated-circuit transistor array to detect the absence of load current by sensing the voltage across the triac. The internal zero-crossing detector is disabled by connection of terminal 12 to terminal 7, and control of the output is made through the external inhibit input, terminal 1. The circuit permits an output only when the voltage at point A exceeds two V_{BE} drops, or 1.3 volts. When A is positive, transistors Q_3 and Q_4 conduct and reduce the voltage at terminal 1 below the inhibit state. When A is negative, transistors Q_1 and Q_2 conduct. When the voltage at point A is less than ±1.3 volts, neither of the transistor pairs conducts; terminal 1 is then pulled positive by the current in resistor R_3, and the output in inhibited.

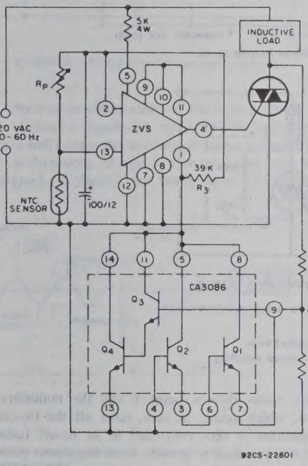


Fig. 19 – Use of the CA3058 or CA3059 together with CA3086 for switching inductive loads.

The circuit shown in Fig. 19 forms a pulse of gate current and can supply high peak drive to power traics with low average current drain on the internal supply. The gate pulse will always last just long enough to latch the thyristor so that there is no problem with delaying the pulse to an optimum time. As in other circuits of this type, RFI results if the load is not suitably inductive because the zero-crossing detector is disabled and initial turn-on occurs at random.

The gate pulse forms because the voltage at point A when the thyristor is on is less than 1.3 volts: therefore, the output of the zero-voltage switch is inhibited, as described above. The resistor divider R_1 and R_2 should be selected to assure this condition. When the triac is on, the voltage at point A is approximately one-third of the instantaneous on-state voltage (v_T) of the thyristor. For most RCA thyristors, v_T (max) is less than 2 volts, and the divider shown is a conservative one. When the load current passes through zero, the triac commutates and turns off. Because the circuit is still being driven by the line voltage, the current in the load attempts to reverse, and voltage increases rapidly across the "turned-off" triac. When this voltage exceeds 4 volts, one portion of the CA3086 conducts and removes the inhibit signal to permit application of gate drive. Turning the triac on causes the voltage across it to drop and thus ends the gate pulse. If the latching current has not been attained, another gate pulse forms, but no discontinuity in the load current occurs.

Provision of Negative Gate Current

Triacs trigger with optimum sensitivity when the polarity of the gate voltage and the voltage at the main terminal 2 are similar (I^+ and II^- modes). Sensitivity is degraded when the polarities are opposite (I^- and III^+ modes). Although RCA triacs are designed and specified to have the same sensitivity in both I^- and III^+ modes, some other types have very poor sensitivity in the III^+ condition. Because the zero-voltage switch supplies positive gate pulses, it may not directly drive some higher-current triacs of these other types.

The circuit shown in Fig. 20(a) uses the negative-going voltage at terminal 3 of the zero-voltage switch to supply a negative gate pulse through a capacitor. The curve in Fig. 20(b) shows the approximate peak gate current as a function of gate voltage V_G. Pulse width is approximately 80 microseconds.

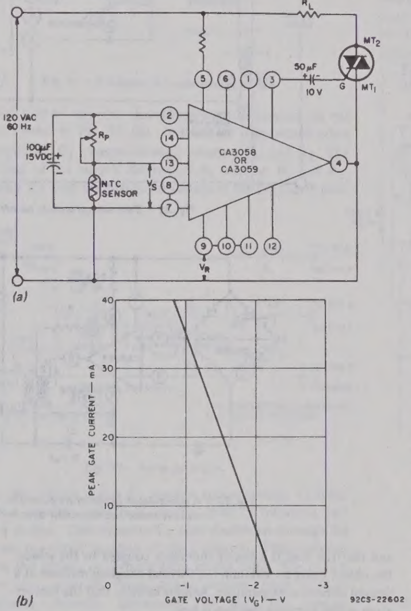


Fig. 20 – Use of the CA3058 or CA3059 to provide negative gate pulses: (a) schematic diagram; (b) peak gate current (at terminal 3) as a function of gate voltage.

Operation with Low-Impedance Sensors

Although the zero-voltage switch can operate satisfactorily with a wide range of sensors, sensitivity is reduced when sensors with impedances greater than 20,000 ohms are used. Typical sensitivity is one per cent for a 5000-ohm sensor and increases to three per cent for a 0.1-megohm sensor.

Low-impedance sensors present a different problem. The sensor bridge is connected across the internal power supply and causes a current drain. A 5000-ohm sensor with its associated 5000-ohm series resistor draws less than 1 milliampere. On the other hand, a 300-ohm sensor draws a current of 8 to 10 milliampers from the power supply.

Fig. 21 shows the 600-ohm load line of a 300-ohm sensor on a redrawn power-supply regulation curve for the zero-voltage switch. When a 10,000-ohm series resistor is used, the voltage across the circuit is less than 3 volts and both sensitivity and output current are significantly reduced. When a 5000-ohm series resistor is used, the supply voltage is nearly 5 volts, and operation is approximately normal. For more consistent operation, however, a 4000-ohm series resistor is recommended.

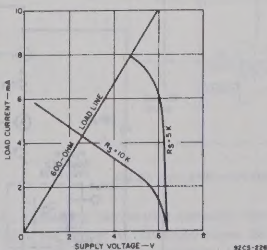


Fig. 21 – Power-supply regulation of the CA3058 or CA3059 with a 300-ohm sensor (600-ohm load) for two values of series resistor.

Although positive-temperature-coefficient (PTC) sensors rated at 5 kilohms are available, the existing sensors in ovens are usually of a much lower value. The circuit shown in Fig. 22 is offered to accommodate these inexpensive metal-wound sensors. A schematic diagram of the RCA CA3080 integrated-circuit operational transconductance amplifier used in Fig. 22, is shown in Fig. 23. With an amplifier bias current, I_{ABC}, of 100 microamperes, a forward transconductance of 2 milliohms is achieved in this configuration. The CA3080 switches when the voltage at terminal 2 exceeds the voltage at terminal 3. This action allows the sink current, I_s, to flow from terminal 13 of the zero-voltage switch (the input impedance to terminal 13 of the zero-voltage switch is approximately 50 kilohms); gate pulses are no longer applied to the triac because Q_2 of the zero-voltage switch is on. Hence, if the PTC sensor is cold, i.e., in the low resistance state, the load is energized. When the temperature of the PTC sensor increases to the desired temperature, the sensor enters the high resistance state, the voltage on terminal 2 becomes greater than that on terminal 3, and the triac switches the load off.

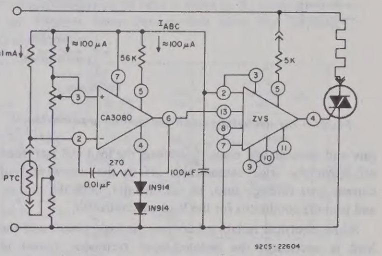


Fig. 22 – Schematic diagram of circuit for use with low-resistance sensor.

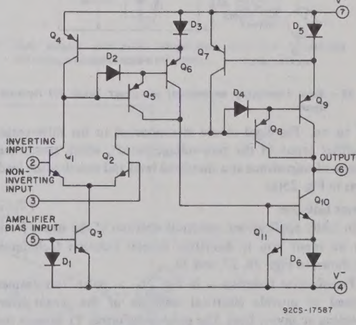


Fig. 23 – Schematic diagram of the CA3080.

Further cycling depends on the voltage across the sensor. Hence, very low values of sensor and potentiometer resistance can be used in conjunction with the zero-voltage switch power supply without causing adverse loading effects and impairing system performance.

Interfacing Techniques

Fig. 24 shows a system diagram that illustrates the role of the zero-voltage switch and thyristor as an interface between the logic circuitry and the load. There are several basic interfacing techniques. Fig. 25(a) shows the **direct input** technique. When the logic output transistor is switched from the on state (saturated) to the off state, the load will be turned on at the next zero-voltage crossing by means of the interfacing zero-voltage switch and the triac. When the logic output transistor is switched back to the on state, zero-crossing pulses from the zero-voltage switch to the triac

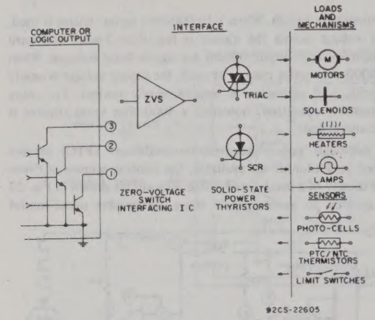


Fig. 24 – The zero-voltage switch and thyristor as an interface.

gate will immediately cease. Therefore, the load will be turned off when the triac commutates off as the sine-wave load current goes through zero. In this manner, both the turn-on and turn-off conditions for the load are controlled.

When electrical isolation between the logic circuit and the load is necessary, the **isolated-input** technique shown in Fig. 25(b) is used. In the technique shown, optical coupling is used to achieve the necessary isolation. The logic output transistor switches the light-source portion of the isolator. The light-sensor portion changes from a high impedance to a low impedance when the logic output transistor is switched from off to on. The light sensor is connected to the differential amplifier input of the zero-voltage switch, which senses the change of impedance at a threshold level and switches the load on as in Fig. 25(a).

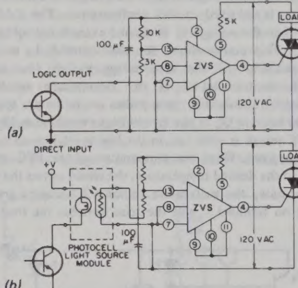


Fig. 25 – Basic interfacing techniques: (a) direct input; (b) isolated input.

Sensor Isolation

In many applications, electrical isolation of the sensor from the ac input line is desirable. Several isolation techniques are shown in Figs. 26, 27, and 28.

Transformer Isolation – In Fig. 26, a pulse transformer is used to provide electrical isolation of the sensor from incoming ac power lines. The pulse transformer T_1 isolates the sensor from terminal No. 1 of the triac Y_1, and transformer T_2 isolates the CA3058 or CA3059 from the power lines. Capacitor C_1 shifts the phase of the output pulse at terminal No. 4 in order to retard the gate pulse delivered to triac Y_1 to compensate for the small phase-shift introduced by transformer T_1.

Many applications require line isolation but not zero-voltage switching. A line-isolated temperature controller for use with inductive or resistive loads that does not include zero-voltage switching is shown in Fig. 27.

In temperature monitoring or control applications the sensor may be a temperature-dependent element such as a resistor, thermistor, or diode. The load may be a lamp, bell, horn, recorder or other appropriate device connected in a feedback relationship to the sensor.

For the purpose of the following explanation, assume that the sensor is a resistor having a negative temperature coefficient

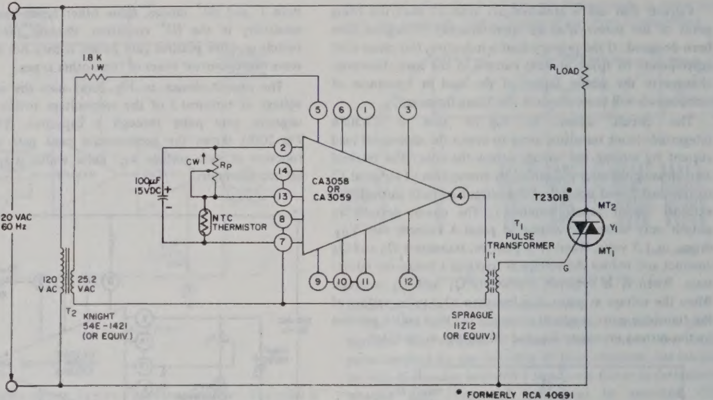


Fig. 26 – Zero-voltage switch, on-off controller with an isolated sensor.

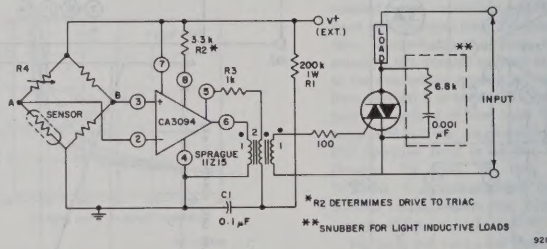


Fig. 27 – A line-isolated temperature controller for use with inductive or resistive loads; this controller does not include zero-voltage switching.

and that the load is a heater thermally coupled to the sensor, the object being to maintain the thermal-coupling medium at a desired reference temperature. Assume initially that the temperature at the coupling medium is low.

The operating potentials applied to the bridge circuit produce a common-mode potential, V_{CM}, at the input terminals of the CA3094. Assuming the bridge to have been initially balanced (by adjustment of R4), the potential at point A will increase when temperature is low since it was assumed that the sensor has a negative temperature coefficient. The potential at the noninverting terminal, being greater than that at the inverting terminal at the amplifier, causes the multivibrator to oscillate at approximately 10 kHz. The oscillations are transformer-coupled through a current-limiting resistor to the gate of the thyristor, and trigger it into conduction.

When the thyristor conducts, the load receives ac input power, which tends to increase the temperature of the sensor. This temperature increase decreases the potential at point A to a value below that at point B and the multivibrator is disabled, which action, in turn, turns off the thyristor. The temperature is thus controlled in an on-off fashion.

Capacitor C_1 is used to provide a low impedance path to ground for feedback-induced signals at terminal No. 5 while blocking the direct current bias provided by resistor R1. Resistor R2 provides current limiting. Resistor R3 limits the secondary current of the transformer to prevent excessive current flow to the control terminal of the CA3094.

Photocoupler Isolation – In Fig. 28, a photocoupler provides electrical isolation of the sensor logic from the incoming ac power lines. When a logic "1" is applied at the input of the photocoupler, the triac controlling the load will be turned on whenever the line voltage passes through zero. When a logic "0" is applied to the photocoupler, the triac will turn off and remain off until a logic "1" appears at the input of the photocoupler.

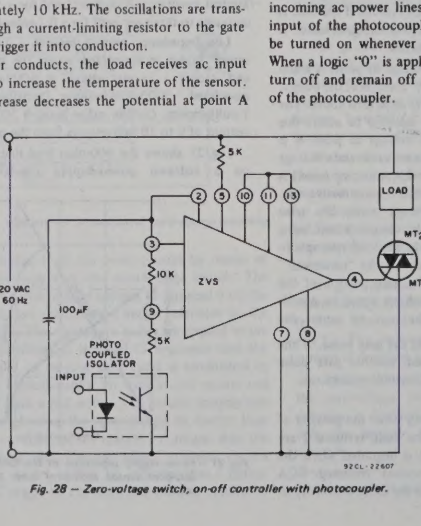


Fig. 28 – Zero-voltage switch, on-off controller with photocoupler.

EMPERATURE CONTROLLERS

Fig. 29 shows a triac used in an on-off mperature-controller configuration. The triac is turned on at ro voltage whenever the voltage V_s exceeds the reference ltage V_r. The transfer characteristic of this system, shown in g. 30(a), indicates significant thermal overshoots and ndershoots, a well-known characteristic of such a system. The fferential or hysteresis of this system, however, can be rther increased, if desired, by the addition of positive edback.

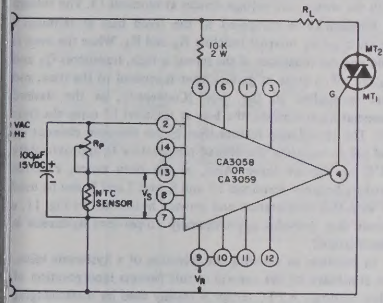
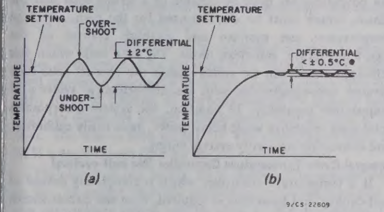


Fig. 29 – CA3058 or CA3059 on-off temperature controller.



(a) (b)

g. 30 – Transfer characteristics of (a) on-off and (b) proportional control systems.

For precise temperature-control applications, the oportional-control technique with synchronous switching is nployed. The transfer curve for this type of controller is own in Fig. 30(b). In this case, the duty cycle of the power ipplied to the load is varied with the demand for heat quired and the thermal time constant (inertia) of the system. or example, when the temperature setting is increased in an ı-off type of controller, full power (100 per cent duty cycle) supplied to the system. This effect results in significant mperature excursions because there is no anticipatory circuit reduce the power gradually before the actual set mperature is achieved. However, in a proportional control chnique, less power is supplied to the load (reduced duty /cle) as the error signal is reduced (sensed temperature proaches the set temperature).

Before such a system is implemented, a time base is chosen that the on-time of the triac is varied within this time base. he ratio of the on-to-off time of the triac within this time terval depends on the thermal time constant of the system ıd the selected temperature setting. Fig. 31 illustrates the rinciple of proportional control. For this operation, power is ıpplied to the load until the ramp voltage reaches a value eater than the dc control signal supplied to the opposite side f the differential amplifier. The triac then remains off for the mainder of the time-base period. As a result, power is proportioned" to the load in a direct relation to the heat emanded by the system.

For this application, a simple ramp generator can be alized with a minimum number of active and passive omponents. A ramp having good linearity is not required for roportional operation because of the nonlinearity of the thermal system and the closed-loop type of control. In the circuit shown in Fig. 32, the ramp voltage is generated when the capacitor C_1 charges through resistors R_0 and R_1. The time base of the ramp is determined by resistors R_2 and R_3, capacitor C_2, and the breakover voltage of the D3202U* diac.

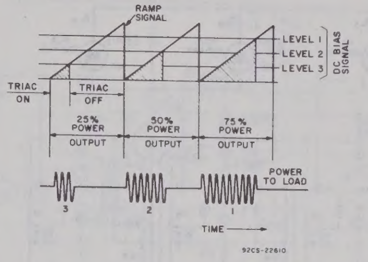


Fig. 31 – Principles of proportional control.

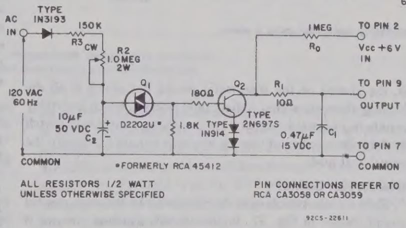


Fig. 32 – Ramp generator.

When the voltage across C_2 reaches approximately 32 volts, the diac switches and turns on the 2N697S transistor and 1N914 diodes. The capacitor C_1 then discharges through the collector-to-emitter junction of the transistor. This discharge time is the retrace or flyback time of the ramp. The circuit shown can generate ramp times ranging from 0.3 to 2.0 seconds through adjustment of R_2. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system, but long with respect to the period of the 60-Hz line voltage. Fig. 33 shows a triac connected for the proportional mode.

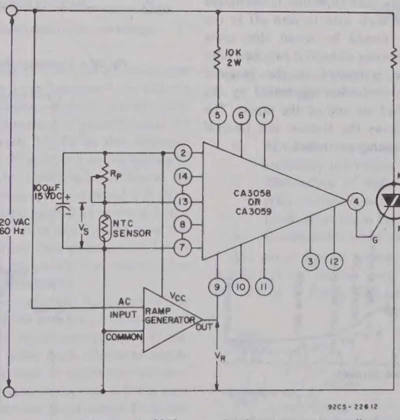
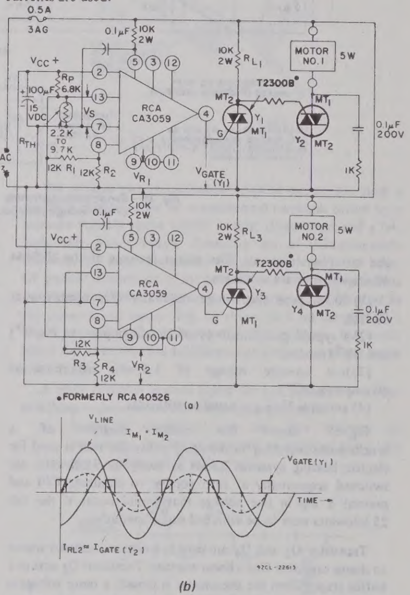


Fig. 33 – CA3058 or CA3059 proportional temperature controller.

Fig. 34(a) shows a dual-output temperature controller that drives two triacs. When the voltage V_s developed across the temperature-sensing network exceeds the reference voltage V_{R1}, motor No. 1 turns on. When the voltage across the network drops below the reference voltage V_{R2}, motor No. 2 turns on. Because the motors are inductive, the currents I_{M1} lag the incoming line voltage. The motors, however, are switched by the triacs at zero current, as shown in Fig. 34(b).

The problem of driving inductive loads such as these motors by the narrow pulses generated by the zero-voltage switch is solved by use of the sensitive-gate RCA-40526 triac. The high sensitivity of this device (3 milliamperes maximum) and low latching current (approximately 9 milliamperes) permit synchronous operation of the temperature-controller circuit. In Fig. 34(a), it is apparent that, though the gate pulse V_g of triac Y_1 has elapsed, triac Y_2 is switched on by the current through R_{L1}. The low latching current of the RCA-40526 triac results in dissipation of only 2 watts in R_{L1}, as opposed to 10 to 20 watts when devices that have high latching currents are used.



(a)

(b)

Fig. 34 – Dual output, over-under temperature controller (a) circuit, (b) voltage and current waveforms.

Electric-Heat Application

For electric-heating applications, the RCA-2N5444 40-ampere triac and the zero-voltage switch constitute an optimum pair. Such a combination provides synchronous switching and effectively replaces the heavy-duty contactors which easily degrade as a result of pitting and wearout from

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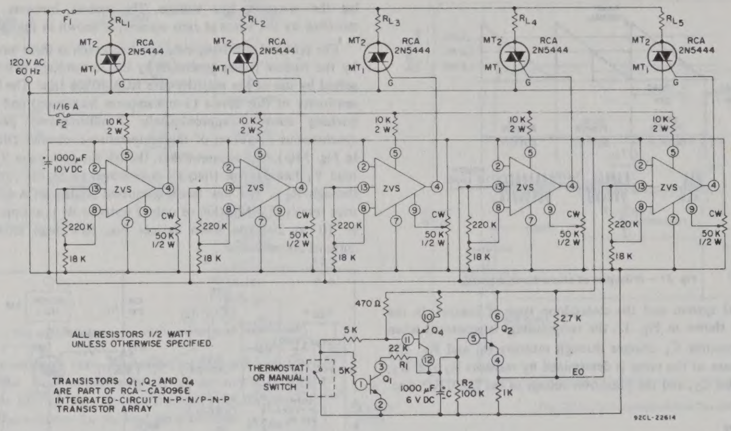
Formerly RCA 45412



ALL RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED

TRANSISTORS Q_1, Q_2 AND Q_4 ARE PART OF RCA-CA3096E INTEGRATED-CIRCUIT N-P-N/P-N-P TRANSISTOR ARRAY

Fig. 35 – Synchronous-switching heat-staging controller using a series of zero-voltage switches.

the switching transients. The salient features of the 2N5444 40-ampere triac are as follows:

(1) 300-ampere single-surge capability (for operation at 60-Hz),

(2) a typical gate sensitivity of 20 milliamperes in the $I(^+)$ and $III(^+)$ modes,

(3) low on-state voltage of 1.5 volts maximum at 40 amperes, and

(4) available V_{DROM} equal to 600 volts.

Fig. 35 shows the circuit diagram of a synchronous-switching heat-staging controller that is used for electric heating systems. Loads as heavy as 5 kilowatts are switched sequentially at zero voltage to eliminate RFI and prevent a dip in line voltage that would occur if the full 25 kilowatts were to be switched simultaneously.

Transistor Q_1 and Q_4 are used as a constant-current source to charge capacitor C in a linear manner. Transistor Q_2 acts as a buffer stage. When the thermostat is closed, a ramp voltage is provided at output E_o. At approximately 3-second intervals, each 5-kilowatt heating element is switched onto the power system by its respective triac. When there is no further demand for heat, the thermostat opens, and capacitor C discharges through R_1 and R_2 to cause each triac to turn off in the reverse heating sequence. It should be noted that some half-cycling occurs before the heating element is switched fully on. This condition can be attributed to the inherent dissymmetry of the triac and is further aggravated by the slow-rising ramp voltage applied to one of the inputs. The timing diagram in Fig. 36 shows the turn-on and turn-off sequence of the heating system being controlled.

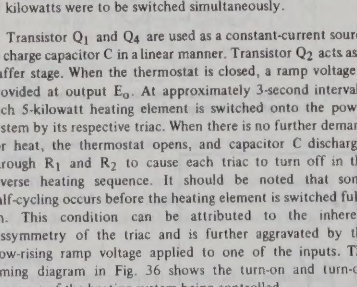


Fig. 36 – Ramp-voltage waveform for the heat-staging controller.

Seemingly, the basic method shown in Fig. 35 could be modified to provide proportional control in which the number of heating elements switched into the system, under any given thermal load, would be a function of the BTU's required by the system or the temperature differential between an indoor and outdoor sensor within the total system environment. That is, the closing of the thermostat would not switch in all the heating elements within a short time interval, which inevitably results in undesired temperature excursions, but would switch in only the number of heating elements required to satisfy the actual heat load.

Oven/Broiler Control

Zero-voltage switching is demonstrated in the oven control circuit shown in Fig. 37. In this circuit, a sensor element is included in the oven to provide a closed-loop system for accurate control of the oven temperature.

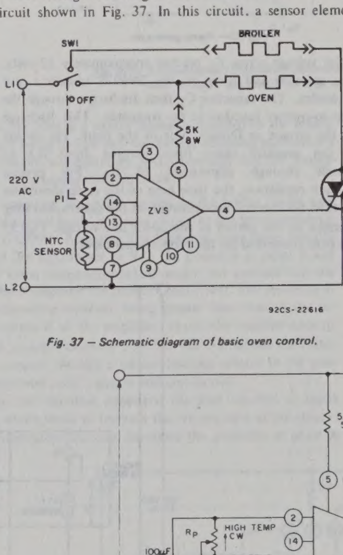


Fig. 37 – Schematic diagram of basic oven control.

As shown in Fig. 37, the temperature of the oven can be adjusted by means of potentiometer R_1, which acts, together with the sensor, as a voltage divider at terminal 13. The voltage at terminal 13 is compared to the fixed bias at terminal 9 which is set by internal resistors R_4 and R_5. When the oven is cold and the resistance of the sensor is high, transistors Q_2 and Q_4 are off, a pulse of gate current is applied to the triac, and heat is applied to the oven. Conversely, as the desired temperature is reached, the bias at terminal 13 turns the triac off. The closed-loop feature then cycles the oven element on and off to maintain the desired temperature to approximately ±2°C of the set value. Also, as has been noted, external resistors between terminals 13 and 8, and 7 and 8, can be used to vary this temperature and provide hysteresis. In Fig. 11, a circuit that provides approximately 10-per-cent hysteresis is demonstrated.

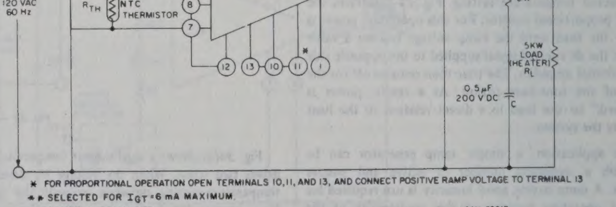
In addition to allowing the selection of a hysteresis value, the flexibility of the control circuit permits incorporation of other features. A PTC sensor is readily used by interchanging terminals 9 and 13 of the circuit shown in Fig. 37 and substituting the PTC for the NTC sensor. In both cases, the sensor element is directly returned to the system ground or common, as is often desired. Terminal 9 can be connected by external resistors to provide for a variety of biasing, e.g., to match a lower-resistance sensor for which the switching-point voltage has been reduced to maintain the same sensor current.

To accommodate the self-cleaning feature, external switching, which enables both broiler and oven units to be paralleled, can easily be incorporated in the design. Of course, the potentiometer must be capable of a setting such that the sensor, which must be characterized for the high, self-clean temperature, can monitor and establish control of the high-temperature, self-clean mode. The ease with which this self-clean mode can be added makes the over-all solid-state systems cost-competitive with electromechanical systems of comparable capability. In addition, the system incorporates solid-state reliability while being neater, more easily calibrated, and containing less-costly system wiring.

Integral-Cycle Temperature Controller (No half-cycling)

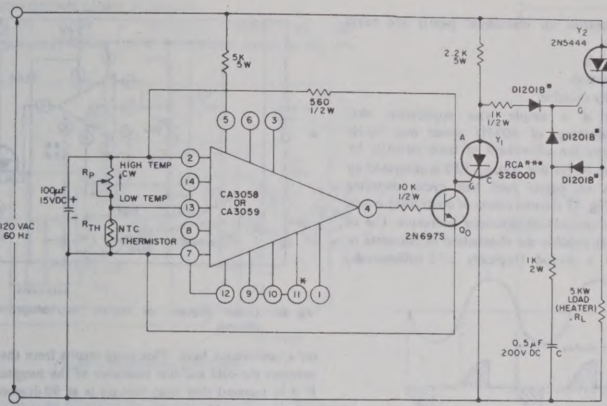
If a temperature controller which is completely devoid of half-cycling and hysteresis is required, then the circuit shown in Fig. 38 may be used. This type of circuit is essential for applications in which half-cycling and the resultant dc component could cause overheating of a power transformer on the utility lines.

In the integral-cycle controller, when the temperature being controlled is low, the resistance of the thermistor is high, and an output signal at terminal 4 of zero volts is obtained. The SCR (Y_1), therefore, is turned off. The triac (Y_2) is then triggered directly from the line on positive cycles of the ac voltage. When Y_2 is triggered and supplies power to the load R_L, capacitor C is charged to the peak of the input voltage



* FOR PROPORTIONAL OPERATION OPEN TERMINALS 10, 11, AND 13, AND CONNECT POSITIVE RAMP VOLTAGE TO TERMINAL 13
** SELECTED FOR I_{GT} = 6 mA MAXIMUM
▪ FORMERLY RCA 44003
● FORMERLY RCA 40655

Fig. 38 – Integral-cycle temperature controller in which half-cycling effect is eliminated.



* FOR PROPORTIONAL OPERATION OPEN TERMINALS 9,10 AND 11 AND CONNECT POSTIVE RAMP VOLTAGE TO TERMINAL 9
** SELECTED FOR I_{GT} = 6 mA MAXIMUM
• FORMERLY RCA 44003
• FORMERLY RCA 40655

92CM-22618

Fig. 39 – CA3058 or CA3059 integral-cycle temperature controller that features a protection circuit and no half-cycling effect.

When the ac line swings negative, capacitor C discharges through the triac gate to trigger the triac on the negative half-cycle. The diode-resistor-capacitor "slaving network" triggers the triac on negative half-cycle to provide only integral cycles of ac power to the load.

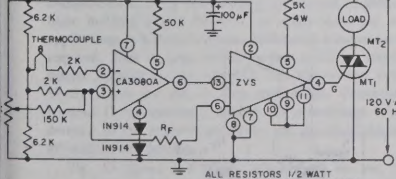
When the temperature being controlled reaches the desired value, as determined by the thermistor, then a positive voltage level appears at terminal 4 of the zero-voltage switch. The SCR then starts to conduct at the beginning of the positive input cycle to shunt the trigger current away from the gate of the triac. The triac is then turned off. The cycle repeats when the SCR is again turned OFF by the zero-voltage switch.

The circuit shown in Fig. 39 is similar to the configuration in Fig. 38 except that the protection circuit incorporated in the zero-voltage switch can be used. In this new circuit, the NTC sensor is connected between terminals 7 and 13, and transistor Q_o inverts the signal output at terminal 4 to nullify the phase reversal introduced by the SCR (Y_1). The internal power supply of the zero-voltage switch supplies bias current to transistor Q_o.

Of course, the circuit shown in Fig. 39 can readily be converted to a **true proportional integral-cycle temperature controller** simply by connection of a positive-going ramp voltage to terminal 9 (with terminals 10 and 11 open), as previously discussed in this Note.

Thermocouple Temperature Control

Fig. 40 shows the CA3080A operating as a pre-amplifier for the zero-voltage switch to form a zero-voltage switching circuit for use with thermocouple sensors.



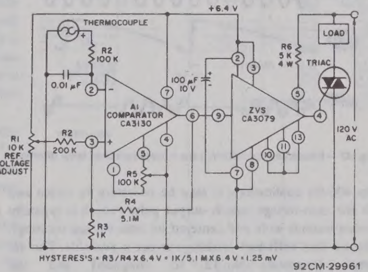
ALL RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED

92CS-22619

ig. 40 – Thermocouple temperature control with zero-voltage switching.

Thermocouple Temperature Control with Zero-Voltage Load Switching

Fig. 41 shows the circuit diagram of a thermocouple temperature control system using zero-voltage load switching. It should be noted that one terminal of the thermocouple is connected to one leg of the supply line. Consequently, the thermocouple can be "ground-referenced", provided the appropriate leg of the ac line is maintained at ground. The comparator, A_1 (a CA3130), is powered from a 6.4-volt source of potential provided by the zero-voltage-switch (ZVS) circuit (a CA3079). The ZVS, in turn, is powered off-line through a series-dropping resistor R6. Terminal 4 of the ZVS provides trigger-pulses to the gate of the load-switching triac in response to an appropriate control signal at terminal 9.



HYSTERES'S = R3/R4 X 6.4 V = 1K/5.1 M X 6.4 V = 1.25 mV

92CM-29961

Fig. 41 – Thermocouple temperature control with zero-voltage switching.

The CA3130 is an ideal choice for the type of comparator circuit shown in Fig. 41 because it can "compare" low voltages (such as those generated by a thermocouple) in the proximity of the negative supply rail. Adjustment of potentiometer R1 drives the voltage-divider network R3, R4 so that reference voltages over the range of 0 to 20 millivolts can be applied to noninverting terminal 3 of the comparator. Whenever the voltage developed by the thermocouple at terminal 2 is more positive than the reference voltage applied at terminal 3, the comparator output is toggled so as to sink current from terminal 9 of the ZVS; gate pulses are then no longer applied to the triac. As shown in Fig. 41, the circuit is provided with a control-point "hysteresis" of 1.25 millivolts.

Nulling of the comparator is performed by means of the following procedure: Set R1 at the low end of its range and short the thermocouple output signal appropriately. If the triac is in the conductive mode under these conditions, adjust nulling potentiometer R5 to the point at which triac conduction is interrupted. On the other hand, if the triac is in the nonconductive mode under the conditions above, adjust R5 to the point at which triac conduction commences. The thermocouple output signal should then be unshorted, and R1 can be set to the voltage threshold desired for control-circuit operation.

MACHINE CONTROL AND AUTOMATION

The earlier section on interfacing techniques indicated several techniques of controlling ac loads through a logic system. Many types of automatic equipment are not complex enough or large enough to justify the cost of a flexible logic system. A special circuit, designed only to meet the control requirements of a particular machine, may prove more economical. For example, consider the simple machine shown in Fig. 42; for each revolution of the motor, the belt is advanced a prescribed distance, and the strip is then punched. The machine also has variable speed capability.

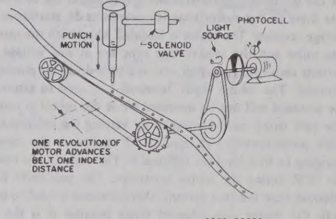


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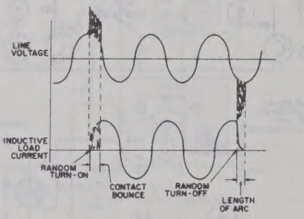
Fig. 42 – Step-and-punch machine.

The typical electromechanical control circuit for such a machine might consist of a mechanical cambank driven by a separate variable speed motor, a time delay relay, and a few logic and power relays. Assuming use of industrial-grade controls, the control system could get quite costly and large. Of greater importance is the necessity to eliminate transients generated each time a relay or switch energizes and deenergizes the solenoid and motor. Fig. 43 shows such transients, which might not affect the operation of this machine, but could affect the more sensitive solid-state equipment operating in the area.

A more desirable system would use triacs and zero-voltage switching to incorporate the following advantages:

a. Increased reliability and long life inherent in solid-state devices as opposed to moving parts and contacts associated with relays.



92CS-22621

Fig. 43 – Transients generated by relay-contact bounce and non-zero turn-off of inductive load.

b. Minimized generation of EMI/RFI using zero-voltage switching techniques in conjunction with thyristors.

c. Elimination of high-voltage transients generated by relay-contact bounce and contacts breaking inductive loads, as shown in Fig. 42.

d. Compactness of the control system.

The entire control system could be on one printed-circuit board, and an over-all cost advantage would be achieved. Fig. 44 is a timing diagram for the proposed solid-state

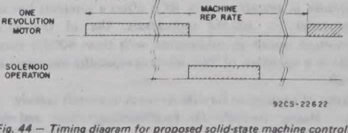


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Fig. 44 – Timing diagram for proposed solid-state machine control.

machine control, and Fig. 45 is the corresponding control schematic. A variable-speed machine repetition rate pulse is set up using either a unijunction oscillator or a transistor astable multivibrator in conjunction with a 10-millisecond one-shot multivibrator. The first zero-voltage switch in Fig. 45 is used to synchronize the entire system to zero-voltage crossing. Its output is inverted to simplify adaptation to the rest of the circuit. The center zero-voltage switch is used as an interface for the photo-cell, to control one revolution of the motor. The gate drive to the motor triac is continuous dc, starting at zero voltage crossing. The motor is initiated when both the machine rate pulse and the zero-voltage sync are at low voltage. The bottom zero-voltage switch acts as a time-delay for pulsing the solenoid. The inhibit input, terminal 1, is used to assure that the solenoid will not be operated while the motor is running. The time delay can be adjusted by varying the reference level (50K potentiometer) at terminal 13 relative to the capacitor charging to that level on terminal 9. The capacitor is reset by the SCR during the motor operation. The gate drive to the solenoid triac is direct current. Direct current is used to trigger both the motor and solenoid triacs because it is the most desirable means of switching a triac into an inductive load. The output of the zero-voltage switch will be continuous dc by connecting terminal 12 to common. The output under dc operation should be limited to 20 milliamperes. The motor triac is synchronized to zero crossing because it is a high-crurent inductive load and there is a chance of generating RFI. The solenoid is a very low current inductive load, so there would be little chance of generating RFI: therefore, the initial triac turn-on can be random, which simplifies the circuitry.

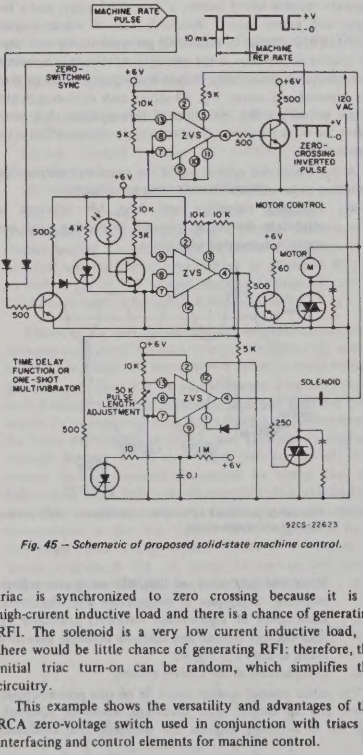


Fig. 45 – Schematic of proposed solid-state machine control.

This example shows the versatility and advantages of the RCA zero-voltage switch used in conjunction with triacs as interfacing and control elements for machine control.

400-Hz TRIAC APPLICATIONS

The increased complexity of aircraft control systems, and the need for greater reliability than electromechanical switching can offer, has led to the use of solid-state power switching in aircraft. Because 400-Hz power is used almost universally in aircraft systems, RCA offers a complete line of triacs rated for 400-Hz applications. Use of the RCA zero-voltage switch in conjunction with these 400-Hz triacs results in a minimum of RFI, which is especially important in aircraft.

Areas of application for 400-Hz triacs in aircraft include:

a. Heater controls for food-warming ovens and for windshield defrosters.
b. Lighting controls for instrument panels and cabin illumination
c. Motor controls
d. Solenoid controls
e. Power-supply switches

Lamp dimming is a simple triac application that demonstrates an advantage of 400-Hz power over 60-Hz power. Fig. 46 shows the adjustment of lamp intensity by phase control of the 60-Hz line voltage. RFI is generated by the step functions of power each half cycle, requiring extensive filtering. Fig. 47 shows a means of controlling power to the lamp by the zero-voltage-switching technique. Use of 400-Hz power makes possible the elimination of complete or half cycles within a period (typically 17.5 milliseconds) without noticeable flicker. Fourteen different levels of lamp intensity can be obtained in this manner. A line-synced ramp is set up with the desired period and applied to terminal No. 9 of the differential amplifier within the zero-voltage switch, as shown in Fig. 48. The other side of the differential amplifier (terminal No. 13) uses a variable reference level, set by the 50K potentiometer. A change of the potentiometer setting changes the lamp intensity.

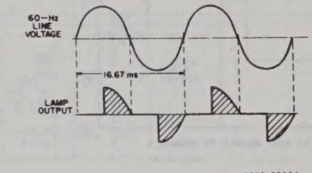


Fig. 46 – Waveforms for 60-Hz phase-controlled lamp dimmer.

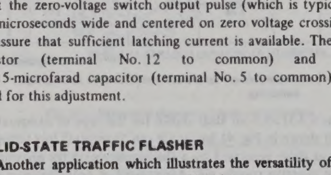


Fig. 47 – Waveforms for 400-Hz zero-voltage-switched lamp dimmer.

In 400-Hz applications it may be necessary to widen and shift the zero-voltage switch output pulse (which is typically 12 microseconds wide and centered on zero voltage crossing), to assure that sufficient latching current is available. The 4K resistor (terminal No. 12 to common) and the 0.015-microfarad capacitor (terminal No. 5 to common) are used for this adjustment.

SOLID-STATE TRAFFIC FLASHER

Another application which illustrates the versatility of the zero-voltage switch, when used with RCA thyristors, involves switching traffic-control lamps. In this type of application, it is essential that a triac withstand a current surge of the lamp load on a continuous basis. This surge results from the difference between the cold and hot resistance of the tungsten filament. If it is assumed that triac turn-on is at 90 degrees from the zero-voltage crossing, the first current-surge peak is approximately ten times the peak steady-state value or fifteen times the steady-state rms value. The second current-surge peak is approximately four times the steady-state rms value.

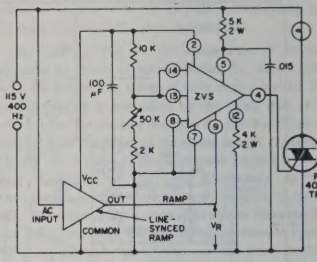


Fig. 48 – Circuit diagram for 400-Hz zero-voltage-switched lamp dimmer.

When the triac randomly switches the lamp, the rate of current rise di/dt is limited only by the source inductance. The triac di/dt rating may be exceeded in some power systems. In many cases, exceeding the rating results in excessive current concentrations in a small area of the device which may produce a hot spot and lead to device failure. Critical applications of this nature require adequate drive to the triac gate for fast turn-on. In this case, some inductance may be required in the load circuit to reduce the initial magnitude of the load current when the triac is passing through the active region. Another method may be used which involves the switching of the triac at zero line voltage. This method involves the supply of pulses to the triac gate only during the presence of zero voltage on the ac line.

Fig. 49 shows a circuit in which the lamp loads are switched at zero line voltage. This approach reduces the initial di/dt, decreases the required triac surge-current ratings, increases the operating lamp life, and eliminates RFI problems. This circuit consists of two triacs, a flip-flop (FF-1), the zero-voltage switch, and a diac pulse generator. The flashing rate in this circuit is controlled by potentiometer R, which provides between 10 and 120 flashes per minute. The state of FF-1 determines the triggering of triacs Y_1 or Y_2 by the output pulses at terminal 4 generated by the zero-crossing circuit. **Transistors Q_1 and Q_2 inhibit these pulses to the gates of the triacs until the triacs turn on by the logical "1" (V_{CC} high) state of the flip-flop.**

The arrangement described can also be used for a synchronous, sequential traffic-controller system by addition of one triac, one gating transistor, a "divide-by-three" logic circuit, and modification in the design of the diac pulse generator. Such a system can control the familiar red, amber, and green traffic signals that are found at many intersections.

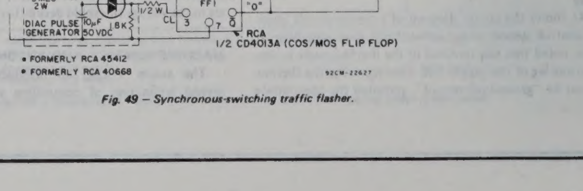


Fig. 49 – Synchronous-switching traffic flasher.

SYNCHRONOUS LIGHT FLASHER

Fig. 50 shows a simplified version of the synchronous-switching traffic light flasher shown in Fig. 49.

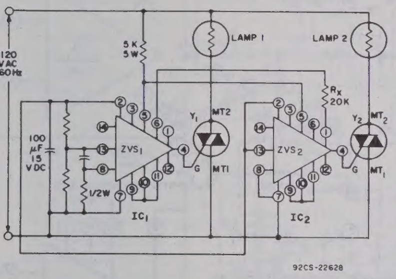


Fig. 50 – Synchronous light flasher.

Flash rate is set by use of the curve shown in Fig. 16. If a more precise flash rate is required, the ramp generator described previously may be used. In this circuit, ZVS_1 is the master control unit and ZVS_2 is slaved to the output of ZVS_1 through its inhibit terminal (terminal 1). When power is applied to lamp No. 1, the voltage of terminal 6 on ZVS_1 is high and ZVS_2 is inhibited by the current in R_x. When lamp No. 1 is off, ZVS_2 is not inhibited, and triac Y_2 can fire. The power supplies operate in parallel. The on-off sensing amplifier in ZVS_2 is not used.

TRANSIENT-FREE SWITCH CONTROLLERS

The zero-voltage switch can be used as a simple solid-state switching device that permits ac currents to be turned on or off with a minimum of electrical transients and circuit noise.

The circuit shown in Fig. 51 is connected so that, after the control terminal 14 is opened, the electronic logic waits until the power-line voltage reaches a zero crossing before power is applied to the load Z_L. Conversely, when the control terminals are shorted, the load current continues until it reaches a zero crossing. This circuit can switch a load at zero current whether it is resistive or inductive.

The circuit shown in Fig. 52 is connected to provide the opposite control logic to that of the circuit shown in Fig. 51. That is, when the switch is closed, power is supplied to the load, and when the switch is opened, power is removed from the load.

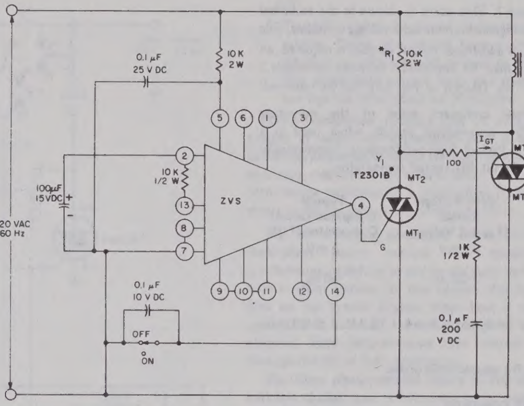
In both configurations, the maximum rms load current that can be switched depends on the rating of triac Y_2. If Y_2 is an RCA-2N5444 triac, an rms current of 40 amperes can be switched.

DIFFERENTIAL COMPARATOR FOR INDUSTRIAL USE

Differential comparators have found widespread use as limit detectors which compare two analog input signals and provide a go/no-go, logic 'one" or logic "zero" output, depending upon the relative magnitudes of these signals. Because the signals are often at very low voltage levels and very accurate discrimination is normally required between them, differential comparators in many cases employ differential amplifiers as a basic building block. However, in many industrial control applications, a high-performance differential comparator is not required. That is, high resolution, fast switching speed, and similar features are not essential. The zero-voltage switch is ideally suited for use in such applications. Connection of terminal 12 to terminal 7 inhibits the zero-voltage threshold detector of the zero-voltage switch, and the circuit becomes a differential comparator.

Fig. 53 shows the circuit arrangement for use of the zero-voltage switch as a differential comparator. In this application, no external dc supply is required, as is the case with most commercially available integrated-circuit comparators; of course, the output-current capability of the zero-voltage switch is reduced because the circuit is operating in the dc mode. The 1000-ohm resistor R_G, connected between terminal 4 and the gate of the triac, limits the output current to approximately 3 milliamperes.

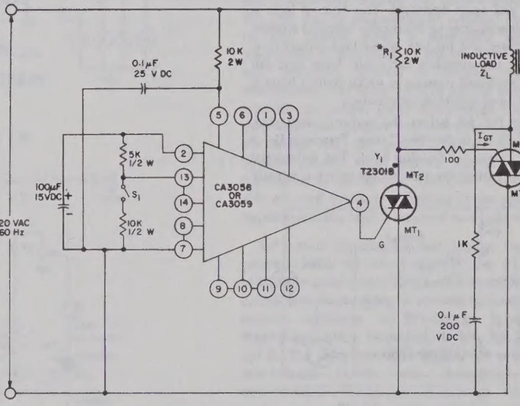
When the zero-voltage switch is connected in the dc mode, the drive current for terminal 4 can be determined from a curve of the external load current as a function of dc voltage



*IF Y_2, FOR EXAMPLE, IS A 40-AMPERE TRIAC, THEN R_1 MUST BE DECREASED TO SUPPLY SUFFICIENT I_{GT} FOR Y_2

• FORMERLY RCA 40691

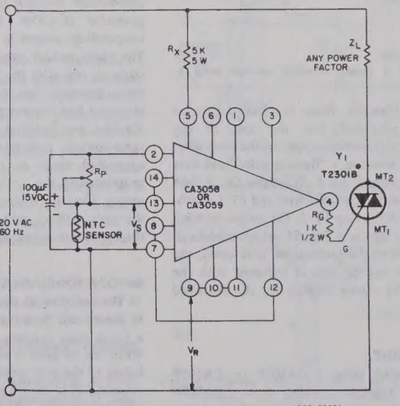
Fig. 51 – Zero-voltage switch transient-free switch controller in which power is supplied to the load when the switch is open.



*IF Y_2, FOR EXAMPLE, IS A 40-AMPERE TRIAC, R_1 MUST BE DECREASED TO SUPPLY SUFFICIENT I_{GT} FOR Y_2

• FORMERLY RCA 40691

Fig. 52 – Zero-voltage switch transient-free switch controller in which power is applied to the load when the switch is closed.



• FORMERLY RCA 40691

Fig. 53 – Differential comparator using the CA3058 or CA3059 integrated-circuit zero-voltage switch.

from terminals 2 and 7. This curve is shown in the technical bulletin for RCA integrated-circuit zero-voltage switches, File No. 490. Of course, if additional output current is required, an external dc supply may be connected between terminals 2 and 7, and resistor R_X (shown in Fig. 53) may be removed.

The chart below compares some of the operating characteristics of the zero-voltage switch, when used as a comparator, with a typical high-performance commercially available integrated-circuit differential comparator.

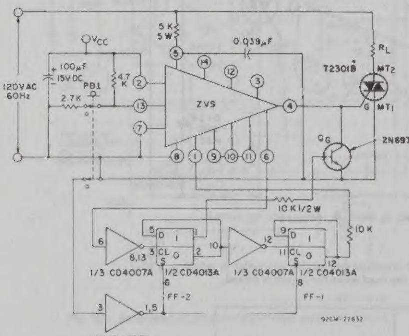
Parameters	Zero-Voltage Switch (Typical Values)	Typical Integrated-Circuit Comparator (710)
Sensitivity	30 mV	2 mV
Switching speed (rise time)	> 20 µs	90 ns
Output drive capability	*4.5 V at ≤ 4 mA	3.2 V at ≤ 5.0 mA

* Refer to Fig. 20; R_X equals 5000 ohms.

POWER ONE-SHOT CONTROL

Fig. 54 shows a circuit which triggers a triac for one complete half-cycle of either the positive or negative alternation of the ac line voltage. In this circuit, triggering is initiated by the push button PB-1, which produces triggering of the triac near zero voltage even though the button is randomly depressed during the ac cycle. The triac does not trigger again until the button is released and again depressed. This type of logic is required for the solenoid drive of electrically operated stapling guns, impulse hammers, and the like, where load-current flow is required for only one complete half-cycle. Such logic can also be adapted to keyboard consoles in which contact bounce produces transmission of erroneous information.

In the circuit of Fig. 54, before the button is depressed, both flip-flop outputs are in the "zero" state. Transistor Q_G is biased on by the output of flip-flop FF-1. The differential comparator which is part of the zero-voltage switch is initially biased to inhibit output pulses. When the push button is depressed, pulses are generated, but the state of Q_G determines the requirement for their supply to the triac gate. The first pulse generated serves as a "framing pulse" and does not trigger the triac but toggles FF-1. Transistor Q_G is then turned off. The second pulse triggers the triac and FF-1 which, in turn, toggles the second flip-flop FF-2. The output of FF-2 turns on transistor Q_7, as shown in Fig. 55, which inhibits all further output pulses. When the pushbutton is released, the circuit resets itself until the process is repeated with the button. Fig. 56 shows the timing diagram for the described operating sequence.



• FORMERLY RCA 40691

Fig. 54 – Block diagram of a power one-shot control using a zero-voltage switch.

PHASE CONTROL CIRCUIT

Fig. 57 shows a circuit using a CA3058 or CA3059 zero-voltage switch together with two CA3086 integrated-circuit transistor arrays to form a phase-control circuit. This circuit is specifically designed for speed control of ac induction motors, but may also be used as a light dimmer.

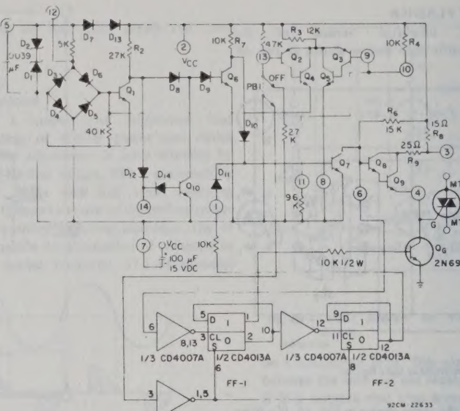


Fig. 55 – Circuit diagram for the power one-shot control.

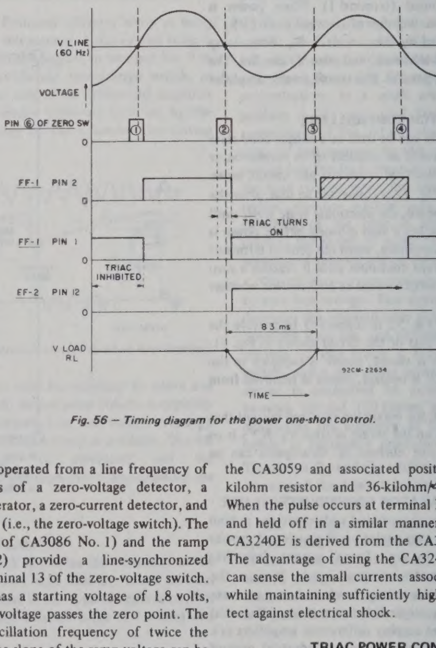


Fig. 56 – Timing diagram for the power one-shot control.

The circuit, which can be operated from a line frequency of 50-Hz to 400-Hz, consists of a zero-voltage detector, a line-synchronized ramp generator, a zero-current detector, and a line-derived control circuit (i.e., the zero-voltage switch). The zero-voltage detector (part of CA3086 No. 1) and the ramp generator (CA3086 No. 2) provide a line-synchronized ramp-voltage output to terminal 13 of the zero-voltage switch. The ramp voltage, which has a starting voltage of 1.8 volts, starts to rise after the line voltage passes the zero point. The ramp generator has an oscillation frequency of twice the incoming line frequency. The slope of the ramp voltage can be adjusted by variation of the resistance of the 1-megohm ramp-control potentiometer. The output phase can be controlled easily to provide 180° firing of the triac by programming the voltage at terminal 9 of the zero-voltage switch. The basic operation of the zero-voltage switch driving a thyristor with an inductive load was explained previously in the discussion on switching of inductive loads.

ON/OFF TOUCH SWITCH

The on/off touch switch shown in Fig. 58 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the on plate is touched, current flows between the two halves of the grid, causing a positive shift in the output voltage (terminal 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at terminal No. 7 of the CA3240E, the triac is turned on and held on by the CA3059 and associated positive feedback circuitry (51-kilohm resistor and 36-kilohm/42-kilohm voltage divider). When the pulse occurs at terminal No. 1, the triac is turned off and held off in a similar manner. Note that power for the CA3240E is derived from the CA3059 internal power supply. The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while maintaining sufficiently high circuit impedance to protect against electrical shock.

TRIAC POWER CONTROLS FOR THREE-PHASE SYSTEMS

This section describes recommended configurations for power-control circuits intended for use with both inductive and resistive balanced three-phase loads. The specific design requirements for each type of loading condition are discussed.

In the power-control circuits described, the integrated-circuit zero-voltage switch is used as the trigger circuit for the power triacs. The following conditions are also imposed in the design of the triac control circuits:

1. The load should be connected in a three-wire configuration with the triacs placed external to the load; eiter delta or wye arrangements may be used. Four-wire loads in wye configurations can be handled as three independent single-phase systems. Delta configurations in which a triac is connected within each phase rather than in the incoming lines can also be handled as three independent single-phase systems.
2. Only one logic command signal is available for the

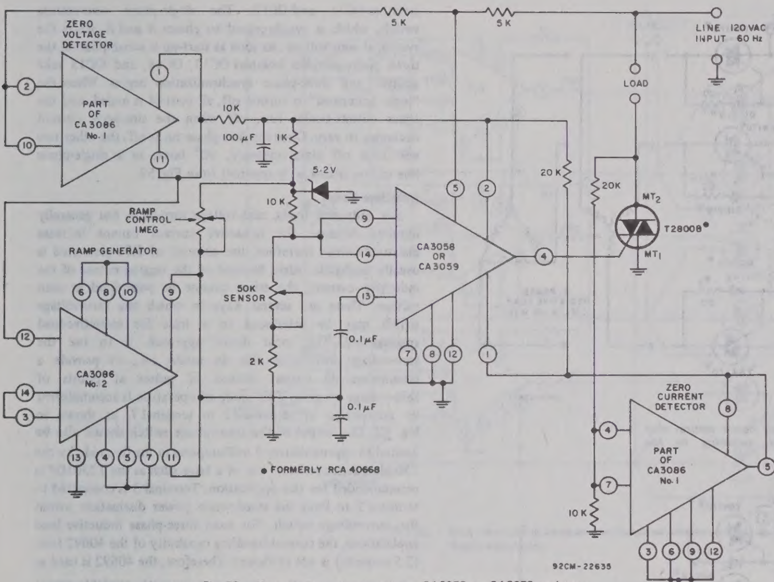


Fig. 57 – Phase Control circuit using a CA3058 or CA3059 and two CA3086 integrated-circuits.

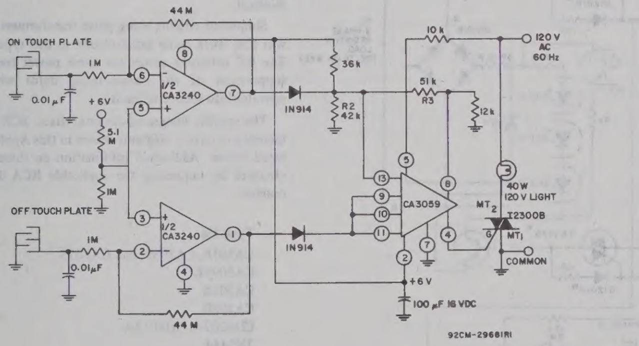


Fig. 58 – On-off touch switch.

control circuits. This signal must be electrically isolated from the three-phase power system.

3. Three separate triac gating signals are required.
4. For operation with resistive loads, the zero-voltage switching technique should be used to minimize any radio-frequency interference (RFI) that may be generated.

Isolation of DC Logic Circuitry

As explained earlier under **Special Application Considerations**, isolation of the dc logic circuitry* from the ac line, the triac, and the load circuit is often desirable even in many single-phase power-control applications. In control circuits for polyphase power systems, however, this type of isolation is essential, because the common point of the dc logic circuitry cannot be referenced to a common line in all phases.

In the three-phase circuits described in this section, photo-optic techniques (i.e., photo-coupled isolators) are used to provide the electrical isolation of the dc logic command signal from the ac circuits and the load. The photo-coupled isolators consist of an infrared light-emitting diode aimed at a silicon photo transistor, coupled in a common package. The light-emitting diode is the input section, and the photo transistor is the output section. The two components provide a voltage isolation typically of 1500 volts. Other isolation techniques, such as pulse transformers, magnetoresistors, or reed relays, can also be used with some circuit modifications.

Resistive Loads

Fig. 59 illustrates the basic phase relationships of a balanced three-phase resistive load, such as may be used in heater applications, in which the application of load power is controlled by zero-voltage switching. The following conditions are inherent in this type of application:

1. The phases are 120 degrees apart; consequently, all three phases cannot be switched on simultaneously at zero voltage.
2. A single phase of a wye configuration type of three-wire system cannot be turned on.
3. Two phases must be turned on for initial starting of the system. These two phases form a single-phase circuit which is out of phase with both of its component phases. The single-phase circuit leads one phase by 30 degrees and lags the other phase by 30 degrees.

These conditions indicate that in order to maintain a system in which no appreciable RFI is generated by the switching action from initial starting through the steady-state operating condition, the system must first be turned on, by zero-voltage switching, as a single-phase circuit and then must revert to synchronous three-phase operation.

Fig. 60 shows a simplified circuit configuration of a three-phase heater control that employs zero-voltage synchronous switching in the steady-state operating condition, with random starting. In this system, the logic command to turn on the system is given when heat is required, and the command to turn off the system is given when heat is not required. Time proportioning heat control is also possible through the use of logic commands.

The three photo-coupled inputs to the three zero-voltage switches change state simultaneously in response to a "logic command". The zero-voltage switches then provide a positive pulse, approximately 100 microseconds in duration, only at a zero-voltage crossing relative to their particular phase. A balanced three-phase sensing circuit is set up with the three zero-voltage switches each connected to a particular phase on their common side (terminal 7) and referenced at their high side (terminal 5), through the current-limiting resistors R4, R5, and R6, to an established artificial neutral point. This artificial neutral point is electrically equivalent to the inaccessible neutral point of the wye type of three-wire load and, therefore, is used to establish the desired phase relationships. The same artificial neutral point is also used to establish the proper phase relationships for a delta type of three-wire load. Because only one triac is pulsed on at a time, the diodes (D1, D2, and D3) are necessary to trigger the opposite-polarity triac, and, in this way, to assure initial latching-on of the system. The three resistors (R1, R2, and R3) are used for current limiting of the gate drive when the opposite-polarity triac is triggered on by the line voltage.

In critical applications that require suppression of all generated RFI, the circuit shown in Fig. 61 may be used. In addition to synchronous steady-state operating conditions, this circuit also incorporates a zero-voltage starting circuit. The start-up condition is zero-voltage synchronized to a single-phase, 2-wire, line-to-line circuit, comprised of phases A and B. The logic command engages the single-phase start-up zero-voltage switch and three-phase photo-coupled isolators OC13, OC14, OC15 through the photo-coupled

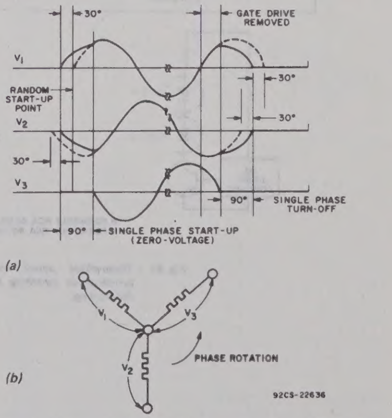


Fig. 59 – Voltage phase relationship for a three-phase resistive load when the application of load power is controlled by zero-voltage switching: (a) voltage waveforms, (b) load-circuit orientation of voltages. (The dashed lines indicate the normal relationship of the phases under steady-state conditions. The deviation at start-up and turn-off should be noted.)

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* The dc logic circuitry provides the low-level electrical signal that dictates the state of the load. For temperature controls, the dc logic circuitry includes a temperature sensor for feedback. The RCA integrated-circuit zero-voltage switch, when operated in the dc mode with some additional circuitry, can replace the dc logic circuitry for temperature controls.

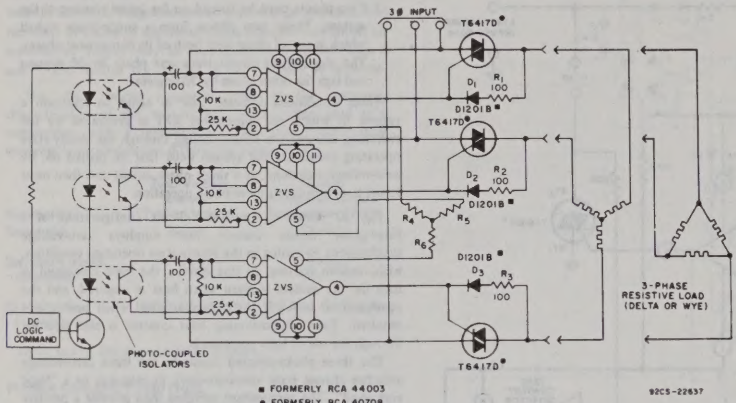

Fig. 60 – Simplified diagram of a three-phase heater control that employs zero-voltage synchronous switching in the steady-state operating conditions.

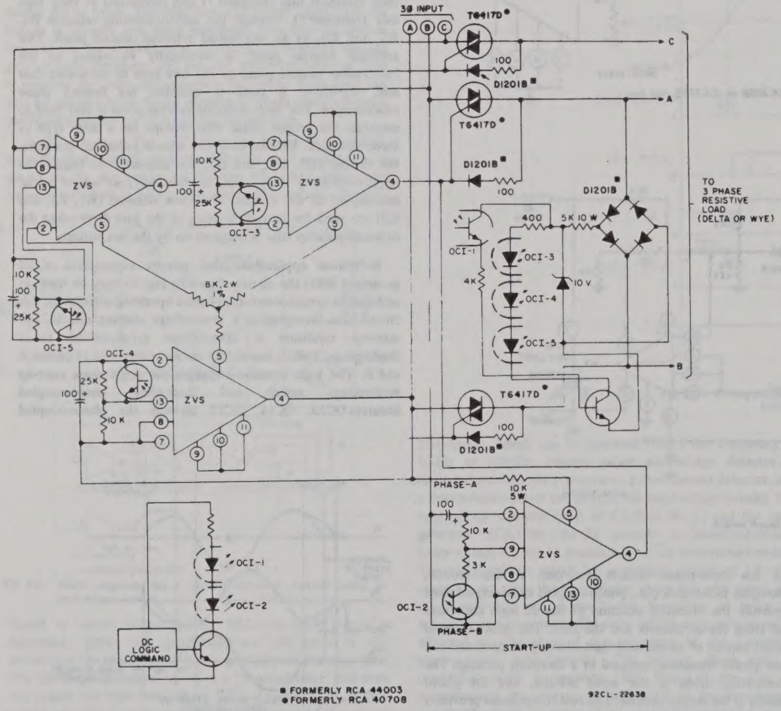

Fig. 61 – Three-phase power control that employs zero-voltage synchronous switching both for steady-state operation and for starting.

isolators OC11 and OC12. The single-phase zero-voltage switch, which is synchronized to phases A and B, starts the system at zero voltage. As soon as start-up is accomplished, the three photo-coupled isolators OC13, OC14, and OC15 take control, and three-phase synchronization begins. When the "logic command" is turned off, all control is ended, and the triacs automatically turn off when the sine-wave current decreases to zero. Once the first phase turns off, the other two will turn off simultaneously, 90° later, as a single-phase line-to-line circuit, as is apparent from Fig. 59.

Inductive Loads

For inductive loads, zero-voltage turn-on is not generally required because the inductive current cannot increase instantaneously; therefore, the amount of RFI generated is usually negligible. Also, because of the lagging nature of the inductive current, the triacs cannot be pulse-fired at zero voltage. There are several ways in which the zero-voltage switch may be interfaced to a triac for inductive-load applications. The most direct approach is to use the zero-voltage switch in the dc mode, i.e., to provide a continuous dc output instead of pulses at points of zero-voltage crossing. This mode of operation is accomplished by connection of terminal 12 to terminal 7, as shown in Fig. 62. The output of the zero-voltage switch should also be limited to approximately 5 milliamperes in the dc mode by the 750-ohm series resistor. Use of a triac such as the T2301D* is recommended for this application. Terminal 3 is connected to terminal 2 to limit the steady-state power dissipation within the zero-voltage switch. For most three-phase inductive load applications, the current-handling capability of the 40692 triac (2.5 amperes) is not sufficient. Therefore, the 40692 is used as a trigger triac to turn on any other currently available power triac that may be used. The trigger triac is used only to provide trigger pulses to the gate of the power triac (one pulse per half cycle); the power dissipation in this device, therefore, will be minimal.

Simplified circuits using pulse transformers and reed relays will also work quite satisfactorily in this type of application. The RC networks across the three power triacs are used for suppression of the commutating dv/dt when the circuit operates into inductive loads.

The specific integrated-circuits, triacs, SCR's, and rectifiers included in circuit diagrams shown in this Application Note are listed below. Additional information on these devices can be obtained by requesting the applicable RCA data-bulletin file number.

Type No.	File No.
CA3058, CA3059, and CA3079	490
CA3099E	620
CA3086	483
CA3080	475
CD4007A, CD4013A	479
2N5444	456
T2800B (40668)	364
T2300B (40526)	470
T2301B (40691), T2301D (40692)	431
T64170 (40708)	406
S2600D (40655)	496
D1201B (44003)	495
D3202U (45412)	577

Note: Numbers in parenthesis (e.g. 40668) are former RCA type numbers.

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* Formerly RCA 40692

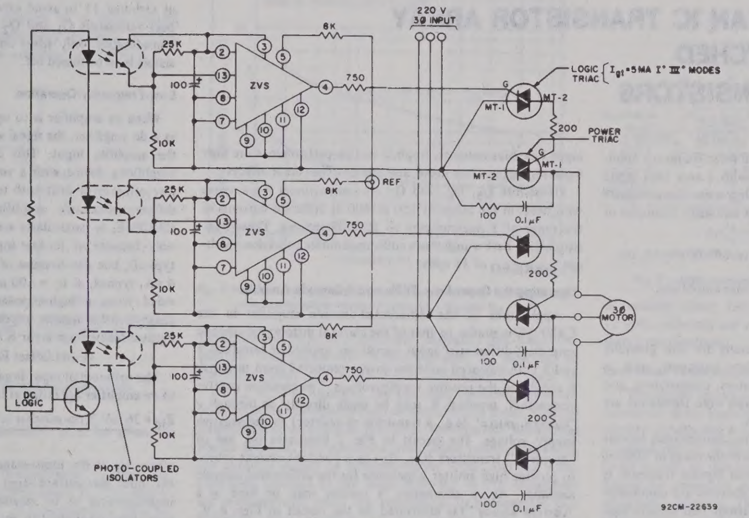

Fig. 62 – Triac three-phase control circuit for an inductive load, i.e., three-phase motor.

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DESIGNING WITH AN IC TRANSISTOR ARRAY CONTAINING MATCHED SUPER-BETA TRANSISTORS

by T. J. Robe

Many small-signal, low-frequency, and video-frequency applications require an amplifying device with a very high input impedance, low input-bias current, and low-noise characteristics that can maintain low dc offset voltage and drift. Examples of such applications include:

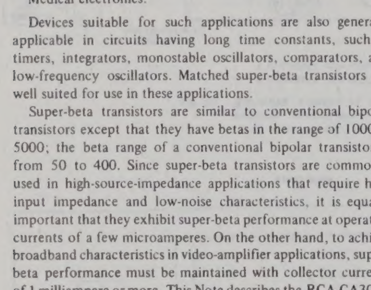
Small-signal instrumentation - chart recorders, meters, etc.
Pre-amps for op-amps.
Magnetic tape-head and phono-cartridge amplifiers.
Opto-electric amplifiers.
Medical electronics.

Devices suitable for such applications are also generally applicable in circuits having long time constants, such as timers, integrators, monostable oscillators, comparators, and low-frequency oscillators. Matched super-beta transistors are well suited for use in these applications.

Super-beta transistors are similar to conventional bipolar transistors except that they have betas in the range of 1000 to 5000; the beta range of a conventional bipolar transistor is from 50 to 400. Since super-beta transistors are commonly used in high-source-impedance applications that require high input impedance and low-noise characteristics, it is equally important that they exhibit super-beta performance at operating currents of a few microamperes. On the other hand, to achieve broadband characteristics in video-amplifier applications, super-beta performance must be maintained with collector currents of 1 milliampere or more. This Note describes the RCA-CA3095 super-beta transistor array and discusses its operation in some typical applications.

A TRANSISTOR-ARRAY IC CONTAINING SUPER-BETA TRANSISTORS

Fig.1 shows the schematic diagram of the RCA-CA3095E, a monolithic IC[1] containing an array of n-p-n transistors of which Q_1 and Q_2 have super-beta characteristics. Q_1 and Q_2 are connected, in conjunction with transistors Q_3 and Q_4, in a differential-cascode-amplifier configuration. Since the super-beta transistors in this IC have a collector-emitter breakdown voltage $V_{(BR)CEO}$ of about 2 volts, it is necessary to limit the collector-emitter voltage accordingly. Limiting is accomplished by means of the voltage-limiting network composed of D_1, D_2 and Q5; these components are included on the CA3095E chip. With this arrangement, the voltage applied to the bases of Q_1 and Q_2 can be varied over a wide common-mode voltage range while the collector-emitter voltages are restrained within a maximum range of about 1.5 volts. The collectors of transistors Q_3 and Q_4 have a minimum collector-to-emitter breakdown voltage of 35 volts. The salient characteristics of the differential-cascode amplifier (Q_1 through Q_4) is the "super-high" ratio between the collector currents (at terminals 10 and 6) and the base currents (into terminals 9 and 7, respectively). The beta of the circuit is typically in the range of 1000 to 5000 at collector currents ranging from less than 1 microampere to more than 1 milliampere. As a consequence, amplifier circuits can be designed to operate with extremely small input base-bias currents. Implicit in this performance are high input impedance, low noise, and low dc offset-error effects.



NOTE: SHADED TRANSISTORS ARE SUPER-BETA TYPES

Fig. 1 – Schematic diagram of the CA3095E.

Transistors Q_5, Q_6, and Q_7 are conventional n-p-n types with betas in the range of 150 to 400 at collector currents in the range of 1 microampere to 10 milliamperes. These transistors also have a minimum collector-emitter breakdown voltage $V_{(BR)CEO}$ of 35 volts.

Operating the Super-Beta, Differential-Cascode Amplifier

Application of the differential-cascode amplifier in the CA3095E is similar to that of the classical differential-cascode amplifier; differential input signals are applied at terminals 7 and 9 with balanced collector loads connected from terminals 6 and 10 to the positive supply voltage. The common emitter connection, terminal 8, may be made directly or through a "current source" (e.g., a transistor or resistor) to the negative supply voltage. The circuit in Fig. 2 illustrates the use of "mirrored" transistors (Q_7, Q_8) as a constant-current source to provide high emitter impedance for the differential-cascode amplifier. As an alternative, a resistor may be used as a "current source" (as illustrated by the circuit in Figs. 8, 9, and 11). The IC substrate (terminal 5) is usually connected directly to the negative supply terminal, as shown in Fig. 2, because it must be maintained at the most negative potential of all elements on the CA3095E chip.

The only additional requirement for CA3095E operation is for bias current into terminal 11 to forward-bias the network composed of D_1, D_2 and Q5, and to supply base-bias current for transistors Q_3 and Q_4. This base-bias current can be provided by connecting a dropping resistor between terminal 11 and the positive supply voltage; this arrangement is illustrated by the use of resistor R_{BIAS} in Fig. 2. As an alternative, this current can be supplied from the positive supply to terminal 11 through a p-n-p constant-current-source transistor to maximize common-mode and power-supply rejection characteristics. In most applications, however, such a constant-current-source arrangement is not necessary because transistor Q_5 conducts most of the D_1, D_2 signal current to the IC substrate connected to terminal 5. As a general rule, the current supplied to terminal 11 should be approximately 4 to 10 per cent of the current drawn from terminal 8. The input signals to the super-beta transistors (terminals 7 and 9) should not be permitted to swing more than 6 volts below the voltage at terminal 11 to avoid exceeding the V_{CBO} rating of super-beta transistors Q_1 and Q_2. This factor is normally a design consideration only when one or both of the input-stage transistors is to be biased off.

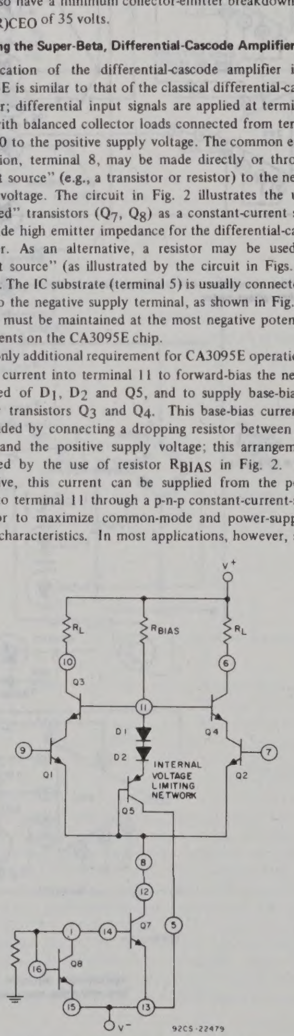


Fig. 2 – Bias arrangement for operation of the super-beta differential-cascode amplifier.

Low-Frequency Operation

When an amplifier is to operate at very low frequencies, or as a dc amplifier, the signal source must be directly coupled to the amplifier input. This coupling requires the use of an amplifying device with a very low input dc offset error and low offset-error drift with temperature variations. A matched differential-cascode amplifier, like the one used in the CA3095E, is particularly well suited to this requirement, not only because of its low input offset voltage (V_{IO} = 1 mV, typical), but also because of its low input offset current (I_O = 4 nA, typical, at I_C = 100 μA). When the input signal is provided from a high-impedance source (R_s), both of these characteristics assume importance because the total effective input-offset-voltage error is the sum of their effects:

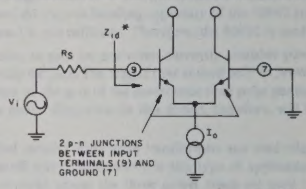
$$\text{Total Offset Error} = V_{IO} + I_{IO}R_s$$

The differential input impedance in megohms (Z_{id} in Fig. 3) of an amplifier operating at low frequencies is given by:

$$Z_{id} = \frac{26\text{ mV X the number of p-n junctions in the input stage}}{I_{IB}\text{ (in nA)}}\ \text{M}\Omega$$

where I_{IB} is the input-stage base-bias current. Consequently, the input bias current (I_{IB}) must be quite low if a high input impedance is to be established. The characteristics of the super-beta transistors in the CA3095E are well suited for use in dc amplifiers requiring high input impedance. For example, with the super-beta transistors operating at input-stage emitter currents of 1 microampere and an H_{FE} of 2000, the base-bias current is only 0.5 nanoampere. Under these conditions,

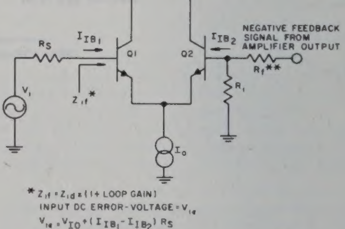
$$Z_{id} = \frac{26\text{ mV X }2}{0.5\text{ nA}} = 104\text{ megohms}$$



*Zid = IMPEDANCE LOOKING INTO TERMINALS (9) AND (7)

Fig. 3 – Input circuit for the differential amplifier.

Impedance levels of this order can also be realized by using negative feedback in connection with devices having higher input bias currents, as illustrated by the circuit shown in Fig. 4. In this arrangement, the use of the feedback network effectively multiplies the differential input impedance. Unfortunately, this arrangement does not avoid the input-offset-voltage effect resulting from the flow of unequal currents through the signal-source resistance (R_s) and the equivalent resistance of the feedback network; i.e., $R_i//R_f$. Consequently, the advantage to be gained by using super-beta transistors is apparent.



$^*Z_{if} = Z_{id} \times (1 + \text{LOOP GAIN})$
INPUT DC ERROR-VOLTAGE = V_{ie}
$V_{ie} = V_{IO} + (I_{IB_1} - I_{IB_2})R_S$

$^{**}R_f // R_i = R_S$
(DESIRED FOR MINIMUM ERROR VOLTAGE)

Fig. 4 – Differential input with provisions for feedback.

Considerations in Low-Noise Performance

Fig.5 shows the schematic diagram of a noise model useful in a review of the considerations pertinent to optimizing low-noise performance in amplifier operation.

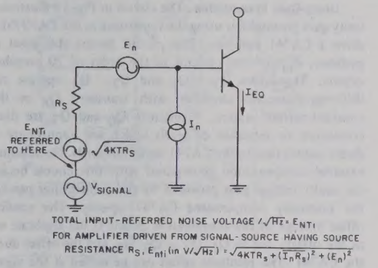

E
n
R
S
E
NTi
REFERRED TO HERE
$\sqrt{4KTR_S}$
V
SIGNAL
I
n
I
EQ
TOTAL INPUT-REFERRED NOISE VOLTAGE $/\sqrt{Hz} = E_{NTi}$
FOR AMPLIFIER DRIVEN FROM SIGNAL-SOURCE HAVING SOURCE RESISTANCE R_S, E_{nti} (in $V/\sqrt{Hz}$) $= \sqrt{4KTR_s + (\overline{I_nR_s})^2 + (E_n)^2}$
92CS-22482

Fig. 5 – Sources of noise in the transistor-amplifier stage.

This model illustrates that consideration must be given to three major sources of noise:

1. Noise contributed by the "thermal-noise" voltage developed across the signal-source resistance, R_s. The magnitude of this voltage in $V/\sqrt{Hz}$ is approximately equal to $\sqrt{4KTR_s}$ for a 1-cycle bandwidth, where k is Boltzmann's constant (1.38 x 10^{-23} joule/°K), T is the temperature in degrees Kelvin, and R_s is the source resistance in ohms.
2. The noise voltage, E_n, resulting from the combined effects of shot noise due to emitter current flow and thermal noise due to transistor base resistance. These effects add in rms fashion to give a total E_n equal to $(E_{shot}^2 + 4KTr_{b'b})^{1/2}$. The shot-noise component, E_{shot}, is inversely proportional to the square root of I_{EQ}, and has a value

$$E_{shot} = \frac{14.2 \times 10^{-12}}{\sqrt{I_{EQ}}} (V/Hz.)$$

   In super-beta transistors, the base resistance component of E_n tends to dominate, particularly at currents greater than 10 microamperes. In addition, this component of E_n has been experimentally found to be inversely related to operating current. Therefore, the total value of E_n is inversely related to operating current I_{EQ}. For example, the CA3095E has a total 1-kHz E_n of approximately 15 $nV/\sqrt{Hz}$ at a collector current of 5 microamperes and approximately 8 $nV/\sqrt{Hz}$ at 50 microamperes.
3. The noise current, I_n, resulting from the combined "shot noise" generated by the flow of base current and the 1/f noise generated in the transistor. The magnitude of I_n is approximately proportional to $\sqrt{I_{IB}}$, where I_{IB} is the base current. The value of I_n is typically 0.12 $pA/\sqrt{Hz}$ at f = 10 Hz when the super-beta differential-cascode amplifier in the CA3095E is operating at $I_{EQ} = 5$ µA. I_n decreases to approximately 0.03 $pA\sqrt{Hz}$ at f = 1 kHz.

When each input terminal in a differential amplifier is driven from a source resistance (R_s), the total noise voltage (referred to the input, see Fig. 5) per unit bandwidth is given by:

$$E_{nti} \text{ (in } V/\sqrt{Hz}) = \sqrt{2KTR_s + 2(\overline{I_nR_s})^2 + (E_n)^2}$$

When amplifiers are driven from low source impedances, E_n is the predominant factor in noise contributions, whereas the effect of I_n predominates when input signals are supplied from high source impedances. Consequently, since the CA3095E operates with very high beta at very low operating currents, it has exceptionally low values of I_n, and is an excellent choice to amplify signals from high source resistances when low amplifier noise contribution is desired. Additionally, the incidence of "popcorn" (burst) noise^2 is low in the CA3095E, a characteristic which further enhances its suitability for use in amplifying signals supplied from high-impedance sources. Figs. 6 and 7 show typical data on I_n and E_n characteristics, respectively, as a function of frequency, for the super-beta transistors in the CA3095E.

Because the operating current of the super-beta transistors in the CA3095E is adjustable over a wide range, the circuit designer can optimize the operating current for maximum signal-to-noise ratio at a particular frequency and source resistance. This adjustment is accomplished by selecting an operating point for which E_n is approximately equal to $\sqrt{2}\, I_n\, R_s$. For example, the optimum operating collector currents in the differential-cascode amplifier are about 5 microamperes when the amplifier is to be driven from two 300-kilohm source resistors. For operation from higher source resistances, the currents should be proportionally lower, and vice versa. Operating currents in the range from 0.1 to 1.0 milliampere are recommended when the amplifier is to be operated as a low-noise video amplifier. At these current levels, the gain-bandwidth product (f_T) is increased significantly with respect to low collector current operation.

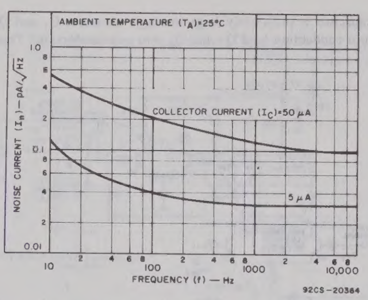


Fig. 6 – Noise current I_n as a function of frequency f for each super-beta cascode-amplifier transistor pair (Q_1 - Q_3 and Q_2 - Q_4).

ILLUSTRATIVE CIRCUIT APPLICATIONS

Like other RCA transistor-array IC's, the CA3095E offers the circuit designer a class of solid-state devices featuring matched electrical and thermal characteristics, compactness, ease of physical handling, economy, and versatility of use. The CA3095E is an electronic "building block" which permits the designer to optimize performance of a particular circuit for gain, noise, power consumption, bandwidth, and/or other specific considerations. Some typical circuit applications of the CA3095E are described below.

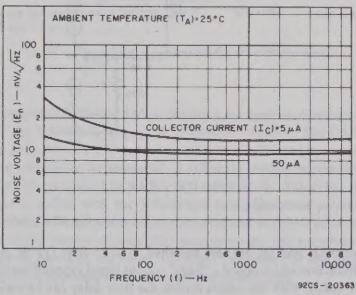


Fig.7 – Noise voltage E_n as a function of frequency f for each super-beta cascode-amplifier transistor pair (Q_1–Q_3 and Q_2–Q_4).

High-Input-Resistance Low-Noise Amplifier

The CA3095E contains all the transistors necessary for the construction of a low-noise, feedback amplifier having a high input resistance ($R_{IN} \cong 20$ MΩ) and a 3-dB bandwidth of about 50 kHz. In the circuit shown in Fig. 8, voltage gain is provided by a cascade of two stages, the differential-cascode stage (Q_1, Q_3 - Q_2, Q_4) and the differential stage (Q_7, Q_8). Transistor Q_6 is an interstage emitter-follower. The voltage gain of the amplifier (approximately 30 dB with the circuit values shown) is essentially established by the ratio of R_8 to the parallel combination of R_5 and R_6. The R_8, C_2 network couples feedback around the entire amplifier. Capacitor C_4 provides stabilizing compensation. The output-voltage swing (E_o) is typically 3 volts, peak-to-peak. Typical noise-figure data are shown in Fig. 8. Power consumption of the amplifier is typically about 750 microamperes at a supply voltage of 12 volts, although the current in transistors Q_1 and Q_2 is less than 5 microamperes.

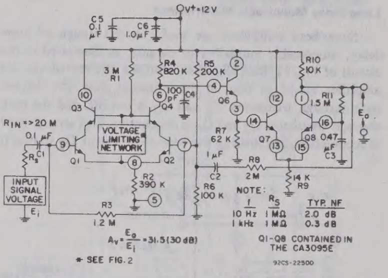


Fig. 8 – High-input-resistance, low-noise amplifier circuit.

Low-Noise Video Amplifier

The circuit shown in Fig. 9 illustrates the use of super-beta transistors in the input stage of a video amplifier. The circuit is capable of delivering 4 volts, peak-to-peak, of output signal with a typical gain of 33 dB across a bandwidth from dc to 10 MHz (3-dB point). In this application, each super-beta transistor is biased for operation at about 400 microamperes to achieve wideband operation. The super-beta transistor characteristics minimize the contributions to noise generated by noise current (I_n) in the input stage. The equivalent input-noise-voltage-vs-frequency characteristics for the entire amplifier circuit are shown in Fig.10. Transistors Q_1 through Q_4 are connected as an emitter-coupled pair of cascode amplifiers with a single-ended load resistor, R_3, to drive a discrete transistor Q-PNP. This combination provides sufficient current gain to drive Q_6, the voltage-gain-stage transistor, with load resistor R_8. Resistor R_7 provides a path for dc and ac feedback around this stage. Transistor Q_8 is an emitter-follower output stage. The typical current drain of the amplifier is approximately 8 milliamperes at a total supply voltage of 10 volts.

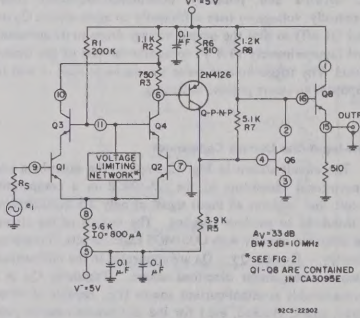


Fig. 9 – Video amplifier.

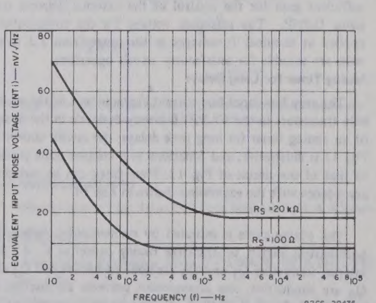


Fig. 10 – Equivalent input noise voltage vs frequency for the circuit of Fig. 9.

Long-Delay Monostable Multivibrator

Super-beta transistors are useful in the design of long-delay, monostable multivibrator circuits, as illustrated in the circuit of Fig. 11. Basically, the circuit is a differential-cascode amplifier biased so that, in the quiescent state, the current path through transistors Q_1 and Q_3 is cut off, and the path through transistors Q_2 and Q_4 is conductive. This arrangement is accomplished by biasing the base of transistor Q_2 so that it is one step of V_{be} (potential $e_7 \cong 0.6$ V) above the base of transistor Q_1, a condition established by the diode-connected transistor Q_6 in shunt with the base of Q_2. The timing cycle is initiated by the application of a negative-going trigger pulse at terminal 13, which is coupled to the base of Q_2 through diode-connected transistor Q_7. Q_2 is cut off and the output voltage rises to essentially V+. Since Q_1 and Q_2 are emitter-coupled, Q_1 is turned on by the trigger pulse, and the potential at terminal 10 drops rapidly; this drop pulls the left-side electrode of capacitor C toward ground. The right-side electrode of capacitor C is connected to the positive 5-volt supply terminal through resistor R; this connection permits the capacitor to be charged in the exponential characteristic of an RC network and, primarily, determines the delay time. Eventually, voltage e_7 rises sufficiently to again switch Q_2 on (and Q1 off) so that the output voltage drops to its quiescent level (approximately +1.8 V) to signify the end of the timing period. The trigger-voltage pulse should be at least -1 volt in amplitude to assure positive switching.

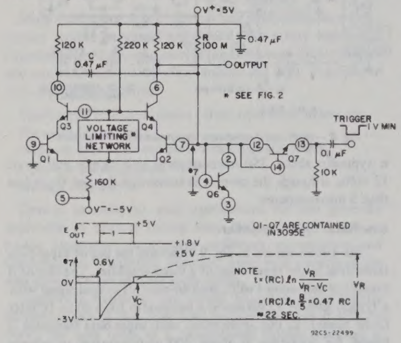


Fig. 11 – Long-delay monostable-multivibrator circuit.

Low-Input-Bias Current Comparator

The circuit shown in Fig. 12 employs the super-beta and conventional transistors in the CA3095E in a comparator circuit that requires an input signal of only 1.5 nanoamperes at threshold to produce toggling. The output of the circuit can interface directly with COS/MOS logic circuits. Transistor pairs $Q_1 - Q_3$ and $Q_2 - Q_4$ are connected in the differential-cascode arrangement described above. Transistor Q_6 is a programmable constant-current source (i.e., capable of being keyed, gated, clocked, etc.) for the differential-cascode pair. Transistors Q_7 and Q_8 are a differential pair used to provide sufficient gain for the control of the external discrete transistor Q-PNP. The reference voltage for the comparator is applied at terminal 7; voltages in the range from 1.5 to 6.0 volts are suitable for satisfactory circuit operation.

Analog Timer for Long Delays

The very low input-bias-current characteristic of the super-beta transistors in the CA3095E is very desirable in the design of an analog timer for long time delays; the circuit shown in Fig. 13 is illustrative, and functions in a manner quite similar to that of the circuit of Fig. 12. Time delay can be varied in accordance with the expression shown in Fig. 13.

The timing cycle is initiated by momentarily closing the push-button switch to discharge timing capacitor C. At this instant, transistors Q_1 and Q_3 are non-conductive and Q_2 and Q_4 are conductive; this arrangement prevents conduction in transistors Q_8 and Q-PNP. Consequently, the output is essentially zero volts. Timing capacitor C is charged exponentially through resistor R until the voltage across the capacitor is sufficiently large to toggle transistor Q_1 and Q_3 into conduction (and Q_2 and Q_4 into non-conduction). Transistors Q_7 and Q_8 are also switched so as to drive Q-PNP into conduction and produce a "high" output signal (approximately 9.7 volts). With the values shown, the time delay can be varied over the range from about 90 to 725 seconds, depending on the setting of the 100-kilohm potentiometer. The leakage-current loading on timing capacitor C due to transistor Q_1 is quite small, and is only of second-order importance in determining timing accuracy.

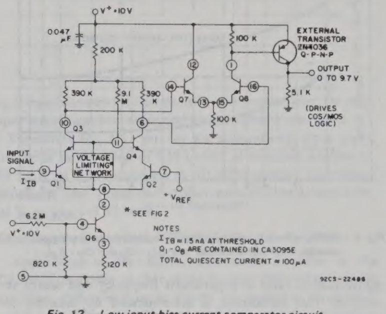


Fig. 12 – Low-input-bias-current comparator circuit.

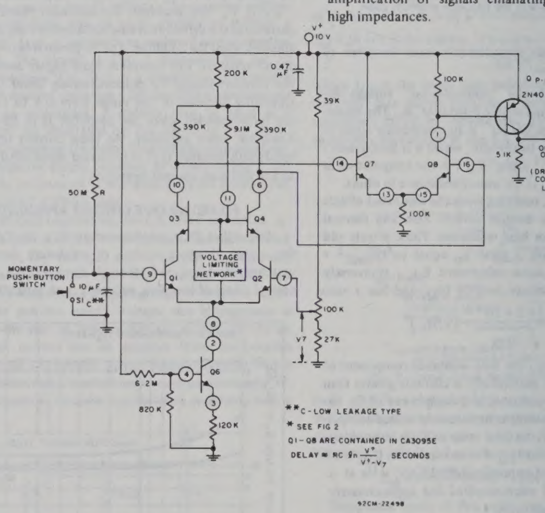


Fig. 13 – Analog timer for long delays.

Super-Beta Transistors in Preamplifier Applications

The wide operating-current range and circuit-connection flexibility available in the super-beta transistors contained in the CA3095E offer numerous advantages for applications in preamplifiers. For example, these transistors can be simply connected as a preamplifier for many of the common, economy-type op-amps (e.g., CA741, CA748)^3 The combination of the CA3095E and one of these op-amps provides an op-amp with the superior input characteristics offered by some of the high-priced op-amps that use super-beta transistors in their input stages. The CA3095E in conjunction with "commodity-class" op-amps can provide an over-all circuit exhibiting orders-of-magnitude improvement over the op-amp itself in terms of input impedance, noise, and the effects of error currents. Several circuit combinations of this type are described below.

Mention has already been made of the low-noise performance which can be achieved with the super-beta transistors in the CA3095E. This attribute is a requisite for preamplifiers operating with low-level signal outputs from sources such as tape heads and magnetic phonograph cartridges. The circuits described below illustrate the simplicity with which super-beta transistor circuits using the CA3095E can be equalized to meet the requirements for NAB playback and RIAA phonograph-record reproduction.

Unity-Gain Preamplifier. The circuit in Fig. 14 illustrates a unity-gain preamplifier using the transistors in the CA3095E to drive a CA741 op-amp. This circuit boosts the input impedance, Z_{id}, of the op-amp to the order of 20 megohms, typical. Transistors Q_1 - Q_3 and Q_2 - Q_4 operate as a differential-cascode amplifier with transistor Q_8 as their constant-current source. Transistors Q_6 and Q_7 are diode-connected to establish dc levels which are appropriate for direct connection to the CA741 input terminals. No additional external compensation is required with this circuit because the unity voltage gain provided by the preamplifier precedes the internally compensated CA741 op-amp. The resultant offset voltage of the combination circuit is the algebraic sum of the offsets due to Q_1, Q_7 vs Q_2, Q_6, and the offset due to the CA741. The resultant offset can be nulled at the normal nulling terminals on the CA741. This circuit is ideal for amplification of signals emanating from sources with very high impedances.

High-Gain Preamplifier The circuit in Fig. 15 shows a high-gain preamplifier using the transistors in the CA3095E to drive a CA748 op-amp. Transistors Q_1 - Q_3, and Q_2 - Q_4 operate as a differential-cascode amplifier with transistor Q_8 as their constant-current source. Transistor Q_7 is diode-connected to drop the dc common-mode voltage at the input of the CA741 to within its linear operating range.

This circuit boosts the input impedance, Z_{id}, of the op-amp to the order of 20 megohms, typical. It also can capitalize on the low-noise operational capability of the CA3095E, and reduces the noise (and offset-voltage) contributions of the CA748 by an increment equal to the gain of the preamplifier, typically about 28 dB with the circuit constants shown. In this case, external compensation of the CA748 may be necessary when the over-all op-amp is connected with feedback.

The approximate value of the compensation capacitor required can be computed by use of the following relationship:

$$C_c \text{ (in pF)} = \frac{30 \text{ X the voltage gain of the preamp}}{\text{closed-loop voltage gain of the composite op-amp}}$$

The circuits in Fig. 16 illustrate applications utilizing the superior input characteristics of super-beta op-amps. A circuit such as the one shown in Fig. 16(a) is useful in applications where input impedances in the order of 150 megohms are required at frequencies up to 5 kHz. Since input bias currents are required to flow through 10-megohm resistors in this circuit, it is mandatory that the input stage exhibit both low bias current and very low input offset current. (The capacitive

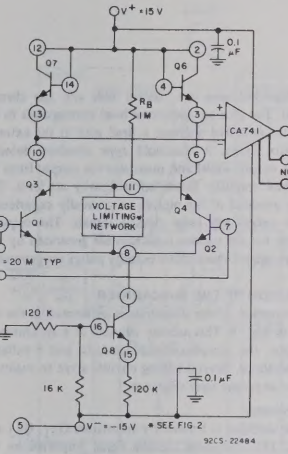


Fig.14 – Op-amp with unity gain preamplifier.

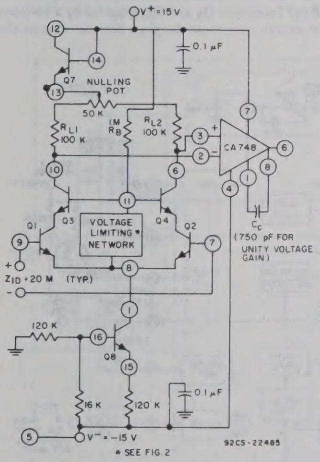


Fig. 15 – Op-amp with high-gain preamplifier.

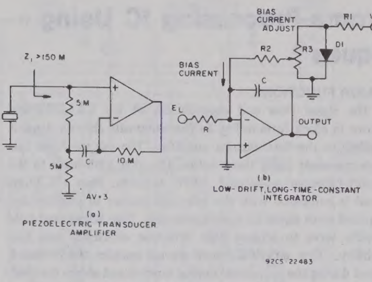


Fig. 16 – Typical super-beta op-amp applications:
(a) piezoelectric transducer amplifier
(b) low-drift, long-time-constant integrator.

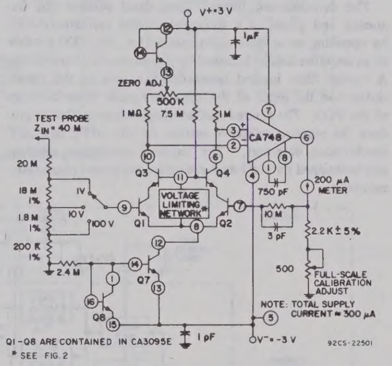


Fig. 17 – Typical high-input-impedance dc-voltmeter circuit.

reactance of the coupling capacitor C must be much lower than 5 megohms to achieve the high-input-impedance characteristic described above.) The low-drift, long-time-constant integrator circuit shown in Fig. 16(b) is another excellent application for the CA3095E super-beta transistor array. Because exceedingly low input bias currents permit the use of a high-value integrating resistor, R, without introducing substantial error, long-time-constant integration can be accomplished. The low input-offset-voltage drift characteristic of the super-beta transistors also contributes to low-error performance. Further reductions in error effects, particularly with temperature variation, can be achieved by using a temperature compensated bias-current source (e.g., R_1–R_3, D_1). In the circuit of Fig.15, such an arrangement could be implemented by using Q_6 in a diode connected fashion to serve as D_1. With such an arrangement, temperature-compensated bias current is applied to the inverting input terminal.

High-Input-Impedance DC-Voltmeter Circuit

The combination of a preamplifier circuit using the CA3095E in conjunction with a CA748 op-amp as described above is adaptable to dc-voltmeter circuits requiring high input impedance, as illustrated by the circuit of Fig. 17. An appropriate resistor-divider network is provided to develop a dc input signal at terminal 9 of the CA3095E with transistors Q_1 - Q_3 and Q_2 - Q_4 connected in the differential-cascode arrangement. Biasing and dc feedback are applied at terminal 7 of the CA3095E through a 10-megohm resistor. The CA748 op-amp drives a 200-microampere meter calibrated in terms of the voltages to be measured. A full-scale reading occurs when the voltage applied to pin 9 is 500 millivolts dc. The entire circuit is nulled with the 500-kilohm zero-adjustment potentiometer. The total power-supply requirement is only 6 volts with a supply current of only 300 microamperes; this requirement can be met with batteries. The input impedance of this simple circuit is approximately 40 megohms on all scales.

Preamplifier for Tape-Head Signals

The exceptional low-noise characteristics of the CA3095E make it suitable for preamplifier service in professional-grade tape-playback systems. A typical circuit with equalization for NAB standards (7.5 in/s) is shown in Fig. 18. Transistors Q_1 and Q_3 are cascode-connected as the input stage, and transistor Q_6 is connected as a common-emitter post-amplifier. Transistors Q_2 and Q_4 are non-conductive because the emitter-base junction in Q_2 and the base-collector junction in Q_4 are shunted by external wiring. Equalization for the NAB tape-playback, frequency-response characteristics is provided by the R_1, C_1, C_2 network connected in the ac feedback path; DC feedback stabilization is provided by the path through resistor R_2. The amplifier has an over-all gain of about 37 db at 1 kHz, and can deliver output voltages in the order of 25 volts, peak-to-peak. The circuit configuration of Fig.18 is preferred to the differential-amplifier configuration because it limits the input-noise contribution to that of a single transistor (e.g., Q_1).

Preamplifier for Signals from Magnetic-Phonograph Cartridges

The exceptional low-noise characteristics of the CA3095E are also of great use in preamplifier service in equipment used to reproduce signals from magnetic phonograph cartridges. A typical circuit for this application with equalization for RIAA playback standards is shown in Fig. 19. Transistors Q_1 and Q_3 are cascode-connected as the input stage, and transistor Q_6 is connected as a common-emitter post-amplifier. Transistor Q_2 and Q_4 are non-conductive because the emitter-base junction in Q_2 and the base-collector junction in Q_4 are shunted by external wiring. Equalization for the RIAA phonograph-frequency-response characteristics is provided by the R_1, C_1 network connected in the ac feedback path. DC feedback stabilization is provided by the path through resistor R_2. The amplifier has an over-all gain of about 40 dB at 1 Hz, and can deliver output voltages in the order of 25 volts, peak-to-peak. The dynamic range of these circuits is typically about 95 dB with the gains indicated.

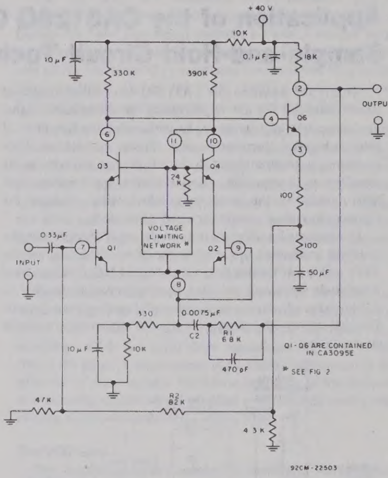


Fig. 18 – Tape play-back preamplifier equalized for NAB standards (7.5 in/s).

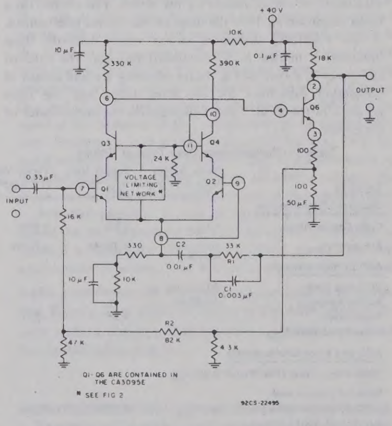


Fig. 19 – Preamplifier equalized for RIAA standards applicable to magnetic phonograph catridges.

ACKNOWLEDGMENT

The circuits of Figs. 18 and 19 were designed by L.A. Kaplan.

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1. "Super-Beta Transistor Array," CA3095E, RCA Data File No. 591.
2. "Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits," T. J. Robe, RCA Application Note ICAN-6732.
3. "Operational Amplifiers," RCA Data File No. 531.

ICAN-6247

Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Circuit Techniques

This Note[*] describes the CA3126Q monolithic integrated circuit intended for use in processing the chrominance signal in a color television receiver. In performing the functions of color subcarrier regeneration and chroma control, emphasis has been placed on utilizing all the information available in the signal so as to approach ultimate system performance capability, while at the same time substantially reducing the number of external components and adjustments.

As contrasted with prior state-of-the-art IC designs, sample-and-hold techniques are used in the phase detectors for the AFPC and the ACC-killer loops of the CA3126Q. The improved signal-to-dc unbalance attained thereby makes it possible to eliminate the adjustments conventionally used in those circuits. The only set-up adjustment is a trimmer capacitor to tune the crystal filter.

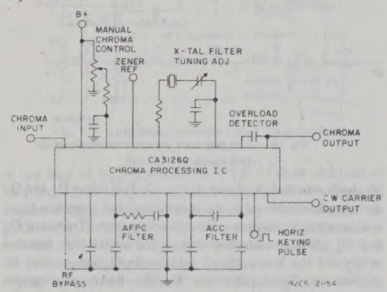


Fig. 1– Components external to the CA3126Q.

Two controls serve to adjust the chroma level: One control is automatic and functions as a supplementary ACC loop to prevent oversaturation under condition of improper transmitted burst-to-chrominance ratio, and under noisy-signal conditions. The second chroma level control is for manual adjustment of the saturation by the viewer. This control has a linear characteristic over the range of the chroma gain control.

The CA3126Q integrated circuit which performs these functions is housed in a 16-terminal package. The external components, shown in Fig. 1, are relatively few and consist of integration capacitors for the servo loops and the filter network in the VCO. Table I summarizes the performance of the circuit.

Table I – Performance Data Typical Values

Function	Nom. Supply $V_{CC} = 11.2$ V	Supply Var. V_{CC} ±2 V	Temp. Var. $\Delta T = 50^{\circ}$C
Oscillator Characteristic			
C. W. Carrier Ampl.	1 V_{pp}	±5%	+ 10%
Frequency	Nom. Sub Carrier	∓70 Hz	–70 Hz
AFPC Characteristic			
DC Loop Gain	40 Hz/deg.		
Pull-in Range	±500 Hz		
Phase Error		∓2°	-2°
Noise Bandwidth f_{NN}	100 Hz		
ACC and Killer Characteristic			
100% Input Level (Red Field)	0.25 V_{pp}		
Nominal Output with Overload Detector	0.5 V_{pp}	±2.5%	–5%
Nominal Output without Overload Detector	2.7 V_{pp}	±10%	–5%
ACC–3 dB Point	20% E_{IN}		
Killer Threshold	5% E_{IN}		
Diff. Phase Error Over Entire ACC Range	1°		
Manual Control Characteristic			
Chroma Output Linearly Proportional to Control Bias			
Diff. Phase Shift with Bias Var.	2°		

MAJOR FUNCTIONS

The signal flow and organization of the CA3126Q are shown in block form in Fig. 2. The composite chroma signal is applied to the first chroma amplifier. The output from this stage proceeds along three paths. The first path leads to the doubly-balanced wide-band AFPC detector. Here the burst signal is compared with the reference carrier to produce the required error signal for synchronization. Two sample-and-hold circuits serve to achieve high detection efficiency and bias stability. One sample-and-hold circuit samples the detected signal during the horizontal keying interval and stores the peak error signal in a filter capacitor. A second similar circuit provides an accurate reference potential as described later. The bias stability of this system is sufficient to eliminate the need for the adjustments required in conventional circuit design.

The detected and filtered burst signal controls the frequency and phase of a voltage-controlled oscillator (VCO) by operating on an electronic phase-shifter. The VCO consists of an amplifier-limiter followed by the electronic phase-shifter. A crystal filter located between the output of the phase-shifter and the input of the amplifier-limiter closes the loop of the VCO. The filtered oscillator signal is amplified to produce the required reference carriers for the AFPC and ACC synchronous detectors. The required quadrature relationship is obtained by $+\pi/4$ and $-\pi/4$ radian integrated phase-shift networks.

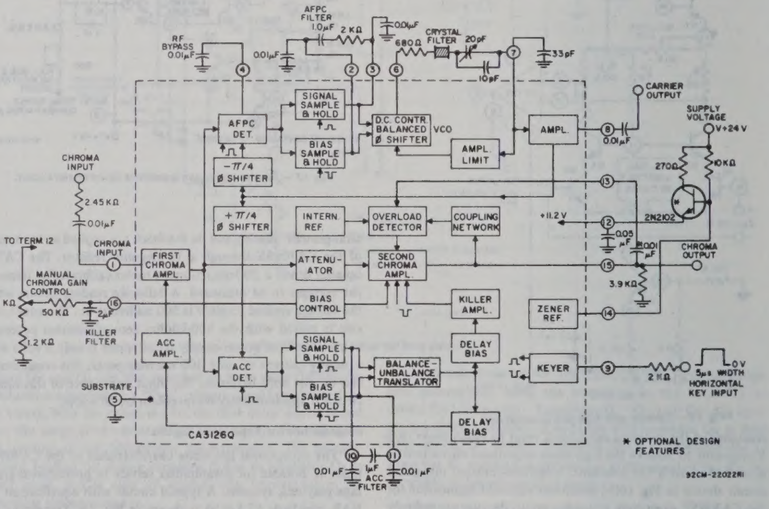


Fig. 2– Signal flow and organization of the CA3126Q.

The ACC-killer detector is similar in structure to the AFPC detector, and is also driven from the first chroma amplifier stage. It detects synchronously the in-phase component of the burst signal and produces a pulse signal proportional in amplitude to the level of the burst signal. The resulting control signal passes through a sampling circuit, as described above, and is applied to the killer and ACC amplifiers. The action of both amplifiers is delayed so that the unkill action takes place prior to ACC and the latter is fully activated upon reaching the predetermined burst level. The ACC amplifier controls the gain of the first chroma amplifier so as to maintain the burst signal constant while the killer amplifier enables the output stage in the presence of the burst signal.

The signal level to the second chroma amplifier is reduced to one fourth of the available signal level to allow for the extremes of the chroma signal excursions. A horizontal rate keyer operating on this stage removes the burst signal so that the output stage is activated only during the horizontal scanning interval. A saturation control, available for front panel control, allows a continuous gain adjustment of this amplifier. A desirable feature of this control is the linear correspondence between the control bias and the chroma output signal. The chroma maximum level corresponds to the maximum bias potential without a dead spot at the extreme of the control range. A threshold type overload detector monitors the output signal and maintains the output from the second chroma amplifier below an arbitrarily set level. This prevents the overload of the picture tube usually experienced on noisy or excessively large chroma signals. The required keying signals for the various functions are generated by two cascaded keyer stages where either polarity pulses are generated.

REGENERATION OF THE SUBCARRIER

The regeneration of the subcarrier is performed in the circuit shown in Fig. 3. This section consists of a synchronous phase detector, the sample-and-hold circuits, and a voltage-controlled oscillator. Several keying circuits serve to maintain the operation in proper time sequence.

The Phase Detector

The phase detector is formed by transistors Q_{51}, Q_{52} and Q_5 to Q_{10}. The composite chroma signal amplified by the first chroma amplifier is applied to transistors Q_7 and Q_8 and the reference carrier is applied to transistors Q_9 and Q_{52}. The product of the two signals is developed across the load resistor R_{13}. Transistors Q_5 and Q_6, triggered by a horizontal rate keyer circuit, operate on the phase detector so as to allow detection of the burst signal only. The current compensation of transistors Q_7 and Q_8 by the gating transistors Q_5 and Q_6 and the absence of filtering at the output of the detector results in transient-free switching of the phase detector. In the absence of chrominance, the potential across the load resistor R_{13} remains constant regardless of the keying. In the presence of the chrominance signal, the phase detector produces two time-spaced outputs: one during the horizontal scanning interval corresponding to the quiescent potential, the second during the horizontal keying interval representing the detected burst. Thus, the detected burst can be measured relative to the quiescent potential rather than to an arbitrary reference. This results in excellent stability for temperature and supply variations.

Sample-and-Hold Circuits

As previously stated, the sample-and-hold circuits shown in Fig. 3 allow efficient utilization of the detected error signal and provide a reliable reference potential. During the sampling interval, the detected pulse signal available at the detector load resistor R_{13} is translated to the AFPC filter capacitor of terminal 2 via transistors Q_{53} and Q_{54}. Q_{53} serves to isolate the

[*] This Note, revised by Wayne Austin (RCA Solid State Division) was originally prepared by L. A. Harwood (Consumer Electronics Division) for publication in the IEEE TRANSACTIONS ON BROADCAST AND TV RECEIVERS, May 1973, Vol. BTR-19, No. 2.

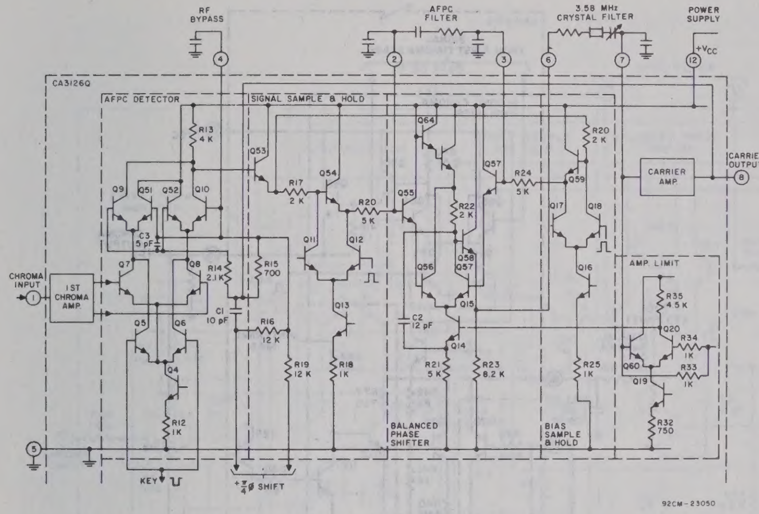


Fig. 3– Subcarrier regeneration circuit.

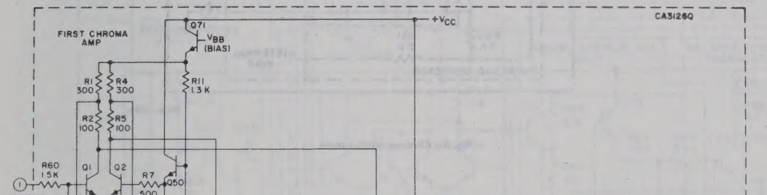


Fig. 4– The first chroma amplifier and the ACC servo loop.

detector from the switching pulses generated in the sampling circuits. The sample-and-hold action is accomplished by controlling the conduction current in transistor Q_{54} thus alternating the charge path during those intervals. During the sampling interval, transistor Q_{54} conducts and its emitter exhibits a relatively low impedance in comparison with the value of the integrated charging resistor R_{20}. The detected or sampled signal is stored in the AFPC filter capacitor which, with R_{20}, determines the time constant during this time interval. During the hold period, transistor Q_{54} is off and the filter time constant is several orders of magnitude larger than previously. The discharge of the filter capacitor is reduced to very small base bias currents only and little of the stored information is lost.

The "on" and "off" condition of the transistor Q_{54} is determined by the state of the transistor-pair Q_{11} and Q_{12}. During the "on" (sampling) interval, a signal from the horizontal rate keyer disables transistor Q_{11} and the collector current of the transistor Q_{12} maintains the transistor Q_{54} in the "on" condition. During the "off" (hold) period, transistors Q_{11} and Q_{12} change their states and the transistor Q_{54} is "off".

The bias sample-and-hold circuit, similar in structure to the above-described circuit, consists of the sampling switch Q_{59} and the transistor-pair Q_{17} and Q_{18}. This circuit, also activated by a signal from a horizontal rate keyer, samples the quiescent potential of the phase detector. The two signals, the error and the bias, processed by the sampling circuits, are stored in filter capacitors, and are applied to opposite terminals of a differential phase control. The phase control circuit synchronizes the reference carrier produced by the VCO.

Depending on the free-running frequency of the VCO, the detected signal is in the form of positive or negative going pulse trains which are then stored in a filter capacitor. The sampling switch has equal drive capabilities for both polarities of the signal; a requirement of particular importance in the presence of noise signals. Non-linear operation of the detector and sampling circuit would produce a rectified dc component causing an erroneous detuning of the VCO.

The VCO Loop

The amplification and amplitude limiting of the oscillator signal takes place in the amplifier-limiter formed by the transistor-pair Q_{60} and Q_{20}. The output from Q_{20} is fed to the dc controlled phase-shifter and returns to the amplifier through a crystal filter. The amplifier operates in a non-inverting mode, hence, the total phase shift through the phase-shifter plus crystal filter must be a multiple of 2 π radians. The crystal filter is tuned to the subcarrier frequency and the filter band-width is determined by a resistor in series with the crystal. The DC controlled phase-shifter has a phase range of approximately $\pm\frac{\pi}{4}$ radians, and a phase change activated by a control signal results in a corresponding oscillator frequency change.

In the phase-shifter, the oscillator signal available at the collector of Q_{20} is applied to the base of Q_{14} from which it proceeds along two paths. An integrated capacitor C_2 couples this signal from the emitter of Q_{14} to the collector load of Q_{15} and, at this point, the signal is phase-shifted by approximately $\pi/4$ radians. In the second path, the signal arriving at the collector of Q_{15} passes through a current splitter formed by the transistor-pair Q_{56}, Q_{15}. This signal is reduced to a level determined by the control voltage at the bases of transistors Q_{56} and Q_{15}. At one extreme, transistor Q_{15} is OFF and the signal at the collector of Q_{15} arrives through the capacitor C_2 only. Conversely, with transistor Q_{15} ON, and Q_{56} OFF, the signal arriving through the transistor Q_{15} is phase-oriented so that the resultant signal has a phase of $+3/4\ \pi$ radians. The phase-control is linear throughout most of the control range.

A buffer amplifier is used to supply the CW carrier required for the demodulators, and the carrier is available at terminal 8. Internally, the buffer amplifier supplies the two synchronous detectors. Two R-C phase-shifters fed from the buffer amplifier provide the required phase orientation. A low-pass R_{14}-C_3 filter shifts the carrier to the AFPC detector by $-\pi/4$ while a high-pass filter provides a $+\pi/4$ oriented carrier for the ACC-killer detector.

AMPLITUDE CONTROL OF THE CHROMINANCE SIGNAL

Two cascaded amplifier stages serve to process the chroma signal and several signals are developed to control the gain of each stage.

First Chroma Amplifier and ACC Servo Loop

The first chroma amplifier, shown in Fig. 4, is controlled by the burst responsive ACC-killer detector only. The amplifier formed by the transistor-pair Q_1, Q_2 is driven single-ended by the applied composite chroma signal. The amplified output from this stage drives differentially the synchronous ACC-killer detector. The gain of the first amplifier is a function of the dc emitter current supplied by the constant current source Q_3. This current source is biased to provide a nominal current and, hence, a nominal gain in the first amplifier stage. The bias of the current source is reduced in response to a detected burst signal and the gain of the first stage diminishes correspondingly.

The ACC-killer detector is similar in structure to the AFPC detector. However, the CW carrier applied to the detector is in phase with the burst signal. The detected burst signal is processed by a sampling circuit in the same manner as previously described in connection with the AFPC circuit. The signal sampling consists of the transistor follower Q_{73} and the keyed transistor-pair Q_{40}, Q_{41}. Resistor R_{63} serves to produce an intentional dc offset across the inputs of the differential pair Q_{43}, Q_{76}. The detected ACC signal is unipolar with respect to the reference potential; thus, the dc offset extends the linear operating range of the amplifier Q_{43}, Q_{76}. The bias sampling circuit consisting of transistors Q_{79}, Q_{44}, Q_{45} applies the quiescent bias to the base of transistor Q_{76}. In the absence of a burst signal, the dc offset maintains transistor Q_{43} in the OFF condition and the following p-n-p transistor, Q_{29}, is also disabled. Thus, the ACC amplifier Q_{28} is non-conducting and the current source Q_3 provides the maximum current to the input stage.

The OFF state of transistor Q_{29} renders the killer amplifier (transistor Q_{27}) inoperative, a condition required to disable the second chroma stage.

Upon amplification of the burst signal in the first chroma amplifier, the detected burst signal increases proportionately to the amplitude of the input signal and combines differentially with the previously described bias signal in the collector load of transistor Q_{43}. Prior to it, the detected and bias signals are smoothed by the ACC filter capacitors. The linear operation of the chroma amplifier, the detector, and the amplifier which follows the sampling circuits is maintained to a signal level sufficient to enable the transistor Q_{28}. This potential, approximately 0.7 V, establishes the delay of the ACC characteristic as shown in Fig. 5. The chroma (burst) signal at the output of the first stage remains essentially constant with further increase of the input signal. The increasing dc potential at the collector of Q_{29} also activates the killer-amplifier Q_{27}. In order to maintain a predictable killer threshold, this action is referenced to the delay point of the ACC. As previously stated, the ACC begins to function at a signal level at which the dc potential across resistor R_{47} reaches 0.7 V. The killer threshold is lower than that of the ACC action and is determined by the voltage drop across resistors R_{48} and R_{47}. Thus, the two threshold signals are predictably established by the ratio $R_{47}/(R_{47} + R_{48})$.

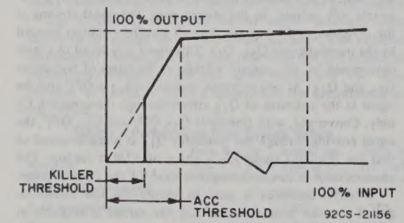


Fig. 5– Normalized ACC characteristic.

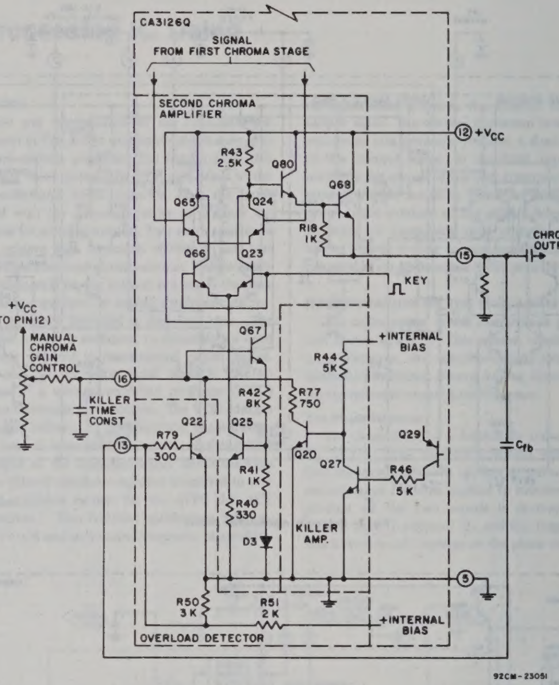


Fig. 6– Chroma output stage.

The Second Chroma Amplifier

The operation of the second chroma amplifier is controlled simultaneously by several signals. As described previously, they are: a customer-operated chroma gain (saturation) control, the killer detector signal, the overload detector, and the keyer.

The amplifier circuit shown in Fig. 6 is formed by the transistor-pair Q_{65}, Q_{24} and is driven differentially by the first chroma amplifier. The signal level to this stage is reduced by means of a resistive voltage divider. The amplifier Q_{65}, Q_{24} is interrupted during the horizontal keying interval by the transistor-pair Q_{66}, Q_{23} to remove the burst information from the composite signal. The gating transistors Q_{66} and Q_{23} are connected so that their emitters and collectors are in parallel with the respective emitters and collectors of transistors Q_{65} and Q_{24}. The resulting collector current compensation maintains the quiescent output potential regardless of the keying operation.

The gain of the second chroma amplifier is adjusted by varying the current in the transistor Q_{25}. A resistive divider R_{41}, R_{42} fed from a follower stage Q_{67} provides the bias potential to the base of the transistor Q_{25} and the voltage drop across resistor R_{40} determines the current flowing from the collector of Q_{25} to the emitters of Q_{65} and Q_{24}. The diode D_3 compensates the base to emitter potential of the transistor Q_{25}.

Since the bias resistors R_{40}, R_{41}, and R_{47}, and also the amplifier load resistor R_{43}, are located on the same IC chip, the resistance ratio of these components is accurately controlled. Thus, the gain of the second chroma amplifier determined by these components is very predictable, and is a function of the bias potential applied to the base of transistor Q_{67} only.

The interfacing of IC's with external control circuits usually presents problems due to the large tolerances associated with both components. The circuit used here overcomes these difficulties. The transistor follower Q_{67} exhibits negligible loading on the bias set by the manual chroma control. Thus, the gain of the second chroma amplifier is uniquely determined by the rotation of the gain control potentiometer and is relatively independent of its resistance value.

The killer operation is also performed on the second chroma amplifier. The amplified output from the ACC-killer detector is applied to the killer switch Q_{20}. In the presence of a burst signal, transistor Q_{20} is off and the chroma amplifier remains undisturbed. In the absence of a burst signal, the collector current in Q_{20} reduces the potential on the base of the transistor Q_{67} so as to cut off the second chroma amplifier.

The Overload Detector

The ACC and the manually operated saturation control provide the essential means to maintain the proper chrominance level to the picture tube. Under certain conditions, however, the presence of the ACC is detrimental. As previously stated, the ACC servo loop maintains a constant output level of the burst signal regardless of the chroma information. Transmitter variations in burst-to-chroma ratios are improperly corrected by the ACC action and, on signals with low burst-to-chroma ratios, the excessively amplified chroma can exceed the dynamic range of the picture tube.

Similar overload problems are experienced when receiving weak signals. The Synchronous ACC detector produces a control signal proportional to the average value of the burst interval signal, and noise does not contribute to the output. Although this type of noise-immune detection is necessary for reliable operation of the killer circuits, it is less desirable for the ACC action because the noise-peaks plus signal tend to produce undesirable over-saturation effects.

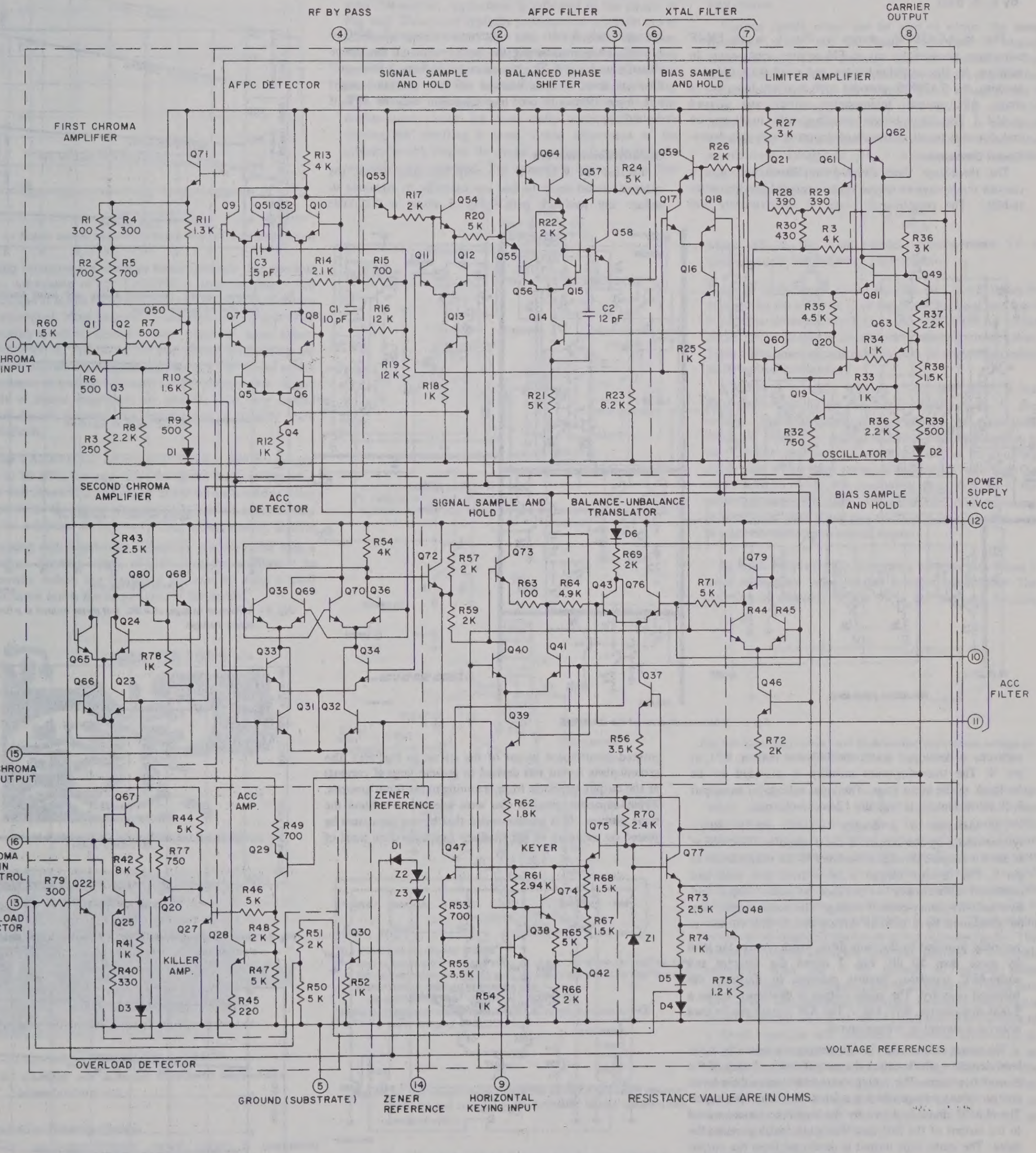
The overload detector operating on the second chroma stage eliminates both these overload problems. The chroma signal from the output terminal of the second chroma amplifier is coupled, by means of the coupling capacitor C_{fb} to overload detector Q_{22}. Transistor Q_{22} is biased by means of an internal bias supply to 0.5 V, and remains off until its base potential is raised to approximately 0.7 V. Thus, detection takes place whenever the chroma signal plus dc bias is equal to or exceeds 0.7 V. The detected and filtered signal lowers the bias potential on the base of transistor Q_{67} and reduces the gain of the output stage.

KEYING CIRCUITS

Details of the keying circuit and of the internal bias circuits are shown in the complete diagram of the CA3126Q in Fig. 7. A positive horizontal rate keying pulse applied to terminal 9 activates the keying circuit. This circuit maintains the AFPC and ACC detectors, with the corresponding sample-and-hold circuit, in the ON position during the keying interval, and disables the chroma output stage at the same time.

CONCLUSION

The new chroma processing circuit improves the performance of a color television receiver. The use of synchronous detection and sampling results in excellent signal stability and fewer external components and adjustments. An overload detector prevents over-saturation of the picture tube, and the improved manual control simplifies the adjustment of the chroma level.



RESISTANCE VALUE ARE IN OHMS.

Fig. 7— Complete circuit diagram showing details of the keying circuit and internal bias circuits.

ICAN-6257

Application of the CA3089E FM-IF Subsystem

by L. S. Baar

The RCA-CA3089E, shown in Fig. 1, is an FM-IF subsystem intended for use in FM receiver applications. In addition to the amplifier-limiter and quadrature detector sections, the CA3089E provides such auxiliary functions as mute, AFC output, tuning-meter output, and delayed rf-AGC.[1] This Note briefly describes each circuit section and discusses practical aspects of designing with this device.

Circuit Description

The three-stage direct-coupled amplifier-limiter uses a cascode input stage to reduce input noise and provide better stability. The peak-to-peak swing of approximately 300 millivolts is developed across the 390-ohm resistor, R31, at pin 8. The operating-point stability is provided by dc feedback to the input stage. The input voltage for an output 3 dB below limiting is typically 12 microvolts rms.

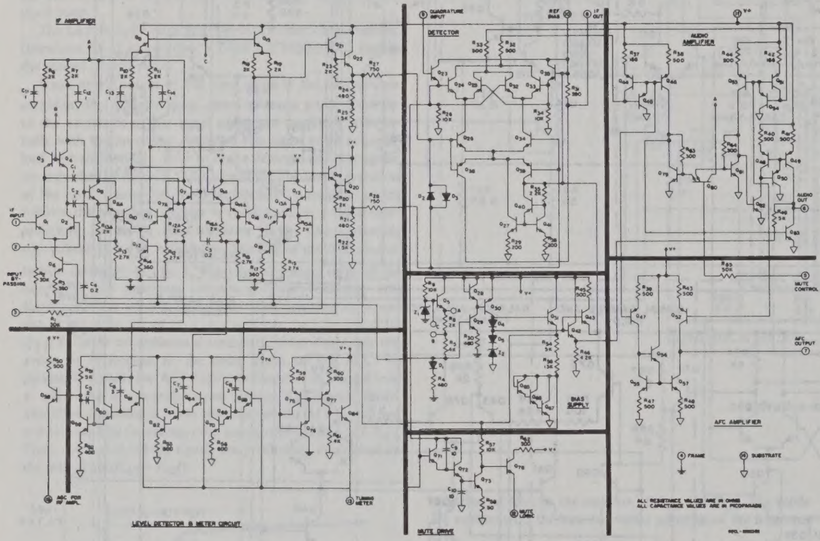


Fig. 1– Schematic diagram of the CA3089E.

The detector is a doubly balanced circuit driven symmetrically by the output of the if amplifier. The voltage at pin 8 is coupled through a reactance to the tuned circuit at pin 9. The detector output is taken from both sides and combined differentially to produce an audio output and automatic-frequency-control voltage. The audio output may be attenuated by a current driving pin 5. The current is normally provided by the mute drive, which reduces the level by more than 50 dB. Fig. 2 shows the detector and audio-AFC translator circuits redrawn to illustrate the balanced circuitry. The audio output is developed across a 5,000-ohm resistor, R49, Fig. 1. The AFC output can be used either as a current or voltage source.

The meter output and rf-AGC circuits are driven by three level detectors which detect the output levels of each of the if amplifier stages. The tuning-meter circuit sums these levels and provides a voltage which is a function of the input signal. The rf-AGC circuit is driven by the level detector connected to the output of the first amplifier stage, which provides the delay. The mute logic output is developed from the output of the third limiter. With a large signal, the if envelope is detected, and drives the mute logic voltage low. As the signal-to-noise ratio deteriorates, "holes" are created in the envelope; these "holes" are detected, and provide the voltage to drive pin 5.

The bias supply maintains the device current drain virtually constant from a supply voltage of 16 volts to approximately 8 volts over a temperature range of –40°C to +100°C while maintaining the performance of the device virtually unchanged. The typical curves in Figs. 3 through 7 illustrate these characteristics. A reference voltage brought out to pin 10 may be used in conjunction with the AFC, if desired.

Stability Considerations

Because the CA3089E is a very high gain device, the external circuit must be laid out carefully to eliminate or reduce any feedback path.[2] Fig. 8 shows a 10.7-MHz printed-circuit-board layout of the circuit in Fig. 9(a). The ground-plane layout was devised to prevent large rf currents at the output terminals from returning to the input grounds. Bypass-capacitor grounds also were selected to achieve the same purpose. It is recommended that bypass capacitors be placed on terminals of the auxiliary functions since most of them are connected to rectifier circuits which are not completely filtered within the device. Capacitors of the disc ceramic type with a 0.01- to 0.02-microfarad value are usually good bypass capacitors at 10.7 MHz. Larger values may exhibit a self-resonance below 10.7 MHz, and actually

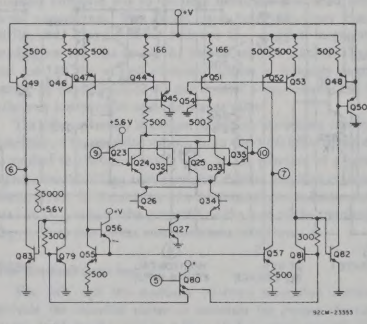


Fig. 2– Detector, audio, and AFC circuits.

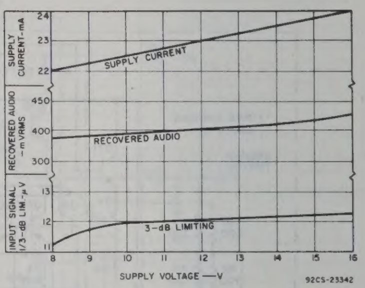


Fig. 3– Supply current, recovered audio, and input limiting as a function of supply voltage.

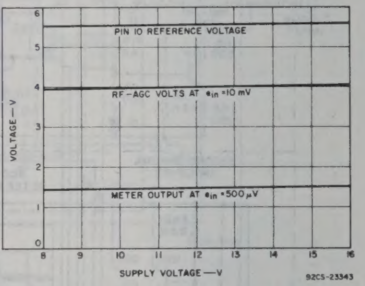


Fig. 4– Reference voltage, rf-AGC, and meter output as a function of supply voltage.

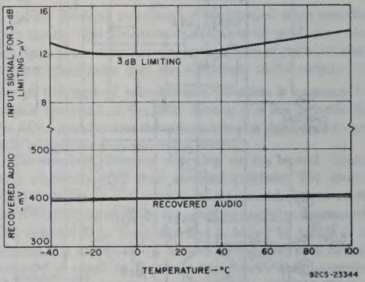


Fig. 5– Input limiting and recovered audio as a function of temperature.

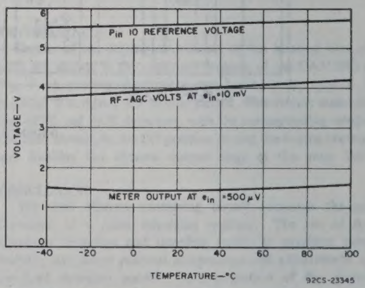


Fig. 6– Reference voltage, rf-AGC, and meter output as a function of temperature.

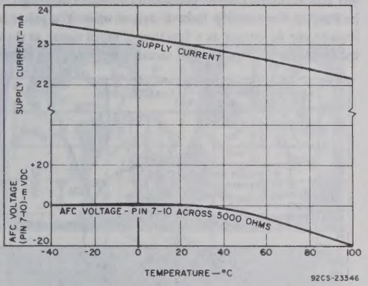


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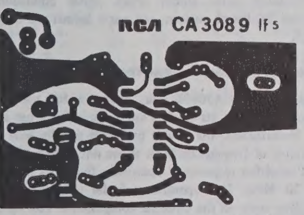
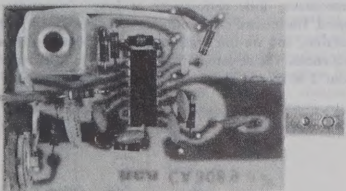
Fig. 7– Supply current and AFC voltage as a function of temperature.

exhibit inductive reactance at their terminals. The nominal input impedance of the CA3089E is approximately 9,000 ohms, and it is not recommended that an impedance match be attempted. Most commercial receivers use ceramic-filter frequency-selective elements that normally have source impedances of 500 ohms or less. When these filters are properly terminated with loading resistors, the typical source impedance is further decreased to 250 ohms or less. Higher levels of source impedance are possible with very careful circuit layout; however, the maintenance of stability could be difficult.

The CA3089E has a frequency response that is typically flat to 20 MHz; consequently, the device can provide useful gain well above that frequency. If the device is used at lower frequencies, the larger-value bypass capacitors required may not be adequate to bypass the higher frequencies. Double bypassing with lower-value capacitors can overcome such a problem. Another means of alleviating the problem is to externally reduce the frequency response by using a small capacitance across the output load of the device.



a) Bottom view of printed-circuit board.

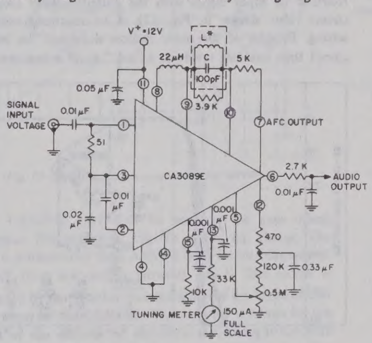


b) Component side – top view.

Fig. 8.– CA3089E and outboard components mounted on a printed circuit board.

Quadrature-Detector Circuits

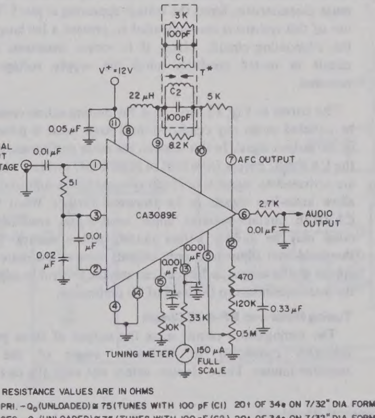
The quadrature-detector tuned circuit is connected between pins 9 and 10. The signal voltage at pin 8 is normally coupled to pin 9 through a choke. The circuit values for the detector network are determined by several factors, the primary one being distortion at a particular level of recovered audio. Distortion is determined by the phase linearity of the quadrature network and is not influenced by the device unless excessive, recovered audio overdrives the audio circuit. With a single tuned network, the phase linearity improves as the bandwidth increases; however, recovered audio decreases. A satisfactory compromise for most FM-receiver applications is reflected in the circuit of Fig. 9(a). This circuit typically provides 400 millivolts rms of recovered audio with less than 0.5-percent distortion. Because a double-tuned circuit has better phase linearity over a wider bandwidth, distortion figures of less than 0.1-percent are attainable with the network used in the circuit of Fig. 9(b). Proper alignment and coupling adjustment of the double-tuned circuit are most easily accomplished while viewing the resulting S curve. Initial adjustment of the primary tuning slug to the proper crossover is made with the secondary slug removed. The secondary tuning slug is then adjusted until a slight "ripple" is observed moving along the S curve. If the ripple is excessive (enough to distort the S curve) the coupling is too tight. If no ripple is observed, the coupling is too loose. As the ripple moves through the crossover point, it will be observed that the S curve becomes more linear near the center frequency. Slight readjustment of both slugs may be necessary for final alignment. The best performance can then be achieved by slight adjustment while measuring distortion. The coupling may be varied by either moving the coils or by changing the value of the secondary load resistor.



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O(UNLOADED) ≅ 75 (G.I. AUTOMATIC MFG. DIV. EX22741 OR EQUIVALENT)

92CM-19040R1

(a)



ALL RESISTANCE VALUES ARE IN OHMS
*T: PRI. – Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20t OF 34e ON 7/32" DIA FORM
SEC. – Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20t OF 34e ON 7/32" DIA FORM
kQ (PER CENT OF CRITICAL COUPLING) ≅ 70%
(ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4mm

92CM-19041R1

(b)

Fig. 9– (a) Test circuit for the CA3089E using a single-tuned detector coil, (b) test circuit for the CA3089E using a double-tuned detector coil.

Various circuit values can be used to obtain the same recovered audio, but the basic conditions of circuit bandwidth and phase linearity must be maintained. The detector circuit also sets up conditions which are required for proper operation of the mute circuit. The rf voltage on pin 9 must be held at approximately 175 millivolts rms, ±25 millivolts. The reason for this requirement is discussed subsequently in connection with the mute logic circuit. The approximate voltage at pin 9 is determined from the equivalent circuit shown in Fig. 10.

The peak-to-peak voltage on pin 9 is:

$$|V_9| \cong |V_8| \frac{R1}{\omega L_{ch}}$$

where R1 is the total parallel resistance and V8 is approximately 300 millivolts, peak-to-peak.

The Q of the tuned circuit between pins 9 and 10 may be affected by the effective Q of the choke between pins 8 and 9 and the series resistor R31 in the CA3089E. All of the above factors should be considered in selecting circuit values. Table I lists some typical combinations of component values under various conditions.

A choke is normally selected to equalize delays in the signal path and in the limiter–quadrature path. It also reduces the if harmonic content across the quadrature circuit. In some cases, such as in narrow-band applications, it may become necessary to use a capacitor as the coupling component where large values of inductance with high Q's are difficult to obtain. If a capacitor is used, the phase of the recovered audio and AFC voltage will be reversed, some asymmetry of the S curve may result, and the distortion may be adversely affected to a small degree.

As indicated above, the inductance between pins 8 and 9 tends to equalize delays in the detector signal paths. The matching of elements of the IC in the balanced detector circuit results in an AFC output with a very small offset when referred to the voltage at pin 10. For most applications, the inherent offset variation is well within tolerances, and does not affect circuit performance. In some narrow-band applications, however, the offset becomes more critical because of the very narrow bandwidth. In such situations, the combination of normal production variations of the device and the external circuit components results in receiver detuning when the AFC loop is closed. This detuning results in an increased distortion of the recovered audio. This distortion can be corrected with the addition of a variable capacitor from pin 8 to ground to provide phase compensation. The capacitor can be adjusted to provide zero AFC offset with minimum distortion. Generally, the offset is in one direction for a given set of conditions. The addition of a fixed capacitor will minimize variations sufficiently to satisfy many applications. A value of 5 picofarads is an effective value for the circuit of Fig. 9(a) with the recommended PC-board layout. Conversely, the offset created by using a capacitor between pins 8 and 9, as mentioned earlier, may be compensated by placing an inductance between pins 8 and 10.

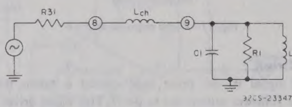


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Fig. 10– Equivalent circuit used to determine approximate voltage on pin 9 of the CA3089E in Fig. 9.

Audio and AFC Circuits

The audio and AFC circuits are very similar, and both develop the same audio signal at their respective output terminals. The audio output voltage on pin 6 is developed across an internal, nominal, 5,000-ohm resistor (R49) connected to the 5.6-volt reference. In addition, the audio signal level can be attenuated by providing a direct current into pin 5 without any shift in its dc level. The audio output,

TABLE I – FIG. 10 COMPONENT VALUES AND CHARACTERISTICS AS A FUNCTION OF FREQUENCY

Freq. (Hz)	L_1 (H)	QL_1	C_1 (pF)	R1 (ohms)	X (pin 8 to pin 9)	Deviation (kHz)	Recovered Audio (mV)
10.7M	2.2µ	75	100	3900	22µH	±75	400
10.7M	2.2µ	120	100		120µH	±5	280
10.7M	2.2µ	120	100		1.3pF	±5	290
455k	0.1m	65	1000	68k	1 mH	±5	400

as shown in Fig. 11, is uniform to a frequency of more than 1 MHz when measured in the circuit shown.

The AFC output at pin 7 is a current source and, if terminated with 5,000 ohms, will provide an audio output identical to that at pin 6. The AFC output may be referenced to a wide range of voltages, from near ground potential to near supply voltage. However, because of the balanced circuit configuration, the best AFC sensitivity and offset will occur at, or near, the 5.6-volt internal reference. An AFC voltage developed across a load tied back to pin 10 is recommended. As a consequence of this connection, variations in the AFC voltage as a function of operating voltage and temperature are minimized because the voltage on pin 7 tends to follow changes in the reference voltage.

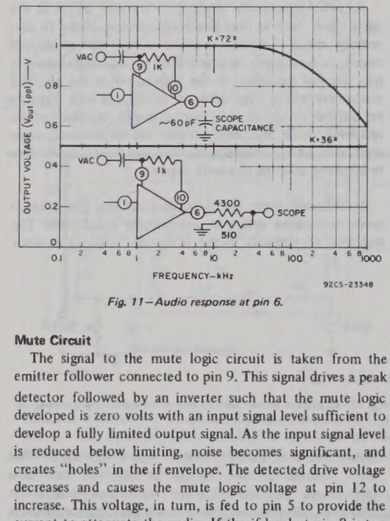

Fig. 11—Audio response at pin 6.

Mute Circuit

The signal to the mute logic circuit is taken from the emitter follower connected to pin 9. This signal drives a peak detector followed by an inverter such that the mute logic developed is zero volts with an input signal level sufficient to develop a fully limited output signal. As the input signal level is reduced below limiting, noise becomes significant, and creates "holes" in the if envelope. The detected drive voltage decreases and causes the mute logic voltage at pin 12 to increase. This voltage, in turn, is fed to pin 5 to provide the current to attenuate the audio. If the if level at pin 9 is too high, the "holes" created by the noise are insufficient to drive the mute logic voltage high enough to attenuate the audio. If the pin 9 voltage is too low, the mute drive voltage never reaches zero, and the external mute-threshold control behaves like a volume control. It is for this reason that the mute logic circuit requirements influence the selection of detector circuit values.

Another condition affecting proper mute performance is excessive gain in the tuner or preceding if stages. High gain ahead of the CA3089E under a condition of low signal-to-noise ratio results in the noise being clipped by the limiting amplifiers. The clipping has the effect of reducing the number of "holes" in the if envelope, and limits the mute drive voltage at pin 12 to values insufficient to attenuate the audio. If high gain is a system requirement, an externally derived mute logic voltage is necessary to drive pin 5.

The external circuit on pin 12 in Fig. 9(a) serves to filter the output, and provides a variable potential for mute-threshold adjustment. The 470-ohm resistor in series with pin 12 reduces the effective Q of the filter capacitor and prevents the circuit from setting up on noise current transients as the mute circuit begins to function. The voltage divider, composed of the 500 kilohm potentiometer and 120 kilohm resistor, controls the threshold point. These values are suggested ones, and may be altered to suit the user. Curve A in Fig. 12 shows the change in audio output level as a function of input signal with the mute-threshold control circuit (also shown in Fig. 12) at its maximum-voltage setting. Because of the more shallow slope and the larger circuit time constant involved, a "soft" mute action results.

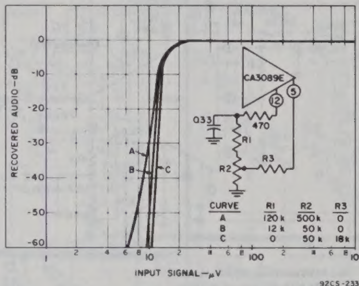

Fig. 12—Mute curves.

Curves B and C illustrate the change in the curves resulting from adjustment of the values of the threshold control circuit. These latter circuits provide a faster acting mute. The fixed resistor, R1, in addition to controlling the slope of the mute characteristic, limits the voltage appearing at pin 5. The use of this resistor is recommended to prevent a latch-up at the attenuating circuit, which, if it occurs, maintains the circuit in muted condition until the supply voltage is removed.

The curves in Fig. 12 show that the muting action cannot be initiated under any condition until some noise is present in the output signal. In this respect, the mute performance of the CA3089E differs from that of some other systems which are activated by signal level. Such systems can be adjusted to allow noise-free signals to be processed further. When the CA3089E circuit operates under small-signal conditions, noise may be audible before muting action occurs. The threshold-level adjustment only permits more or less noise to appear at the output; a listener can use the control to adjust the interstation hiss to the level of his preference.

Tuning Meter and RF-AGC Circuit

The tuning-meter circuit sums the output of three peak detectors connected to successive stages of the if amplifier-limiter. These circuits detect not only the carrier, but also harmonics developed when successive stages go into limiting and eventually form a square wave. The result is a logarithmic dc output as a function of input signal, as shown by the curve in Fig. 13. The circuit developing the delayed rf-AGC voltage is driven by the level detector connected to the first if stage. As a result, no output is detected until the input signal is large enough to drive the peak detector; the result is a delayed AGC action. The curve of rf-AGC voltage as a function of input signal is also shown in Fig. 13.

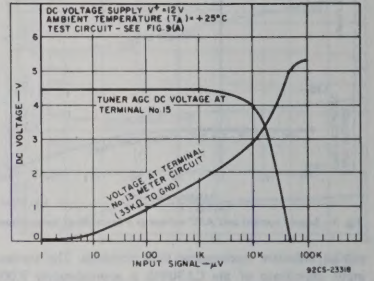

Fig. 13—Tuner AGC and tuning-meter output as a function of input signal voltage.

IF Amplifier/Detector System and Stereo Decoder

Fig. 14 shows the circuit diagram of a complete FM-if detector system driving a stereo decoder. Using the selectivity of two ceramic filters, the CA3089E in conjunction with the CA3090AQ stereo decoder provides the basic signal processing between the tuner output and the audio amplifiers. The gain of the silicon n-p-n bipolar-transistor stage is adjusted to make up the losses of the two filters. In addition to driving a tuning meter, the voltage at pin 13 of the CA3089E may be used to drive a "stereo defeat" circuit in the CA3090AQ, thereby holding the decoder in a monaural condition to improve the signal-to-noise ratio under weak signal conditions. A suggested PC-board pattern and parts layout are shown in Fig. 15.

Operation at Frequencies Other Than 10.7 MHz

Because the CA3089E was designed for use in FM broadcast receivers, its circuits are optimized for use at 10.7 MHz. Nevertheless, the device performs equally well over a wide range of frequencies both above and below 10.7 MHz. The if amplifier response is essentially flat from dc to more than 20 MHz. The operation of the detector circuit is dependent only on the external components. The operation of the auxiliary sections–rf-AGC, meter output, and mute logic – depend on internal peak detectors, and, as a consequence, their performance at lower frequencies is limited. The internal capacitors were optimized for 10.7 MHz operation, and are too small to operate effectively at lower frequencies. The detector efficiencies begin to deteriorate at about 2 MHz, and the detectors are essentially unusable at

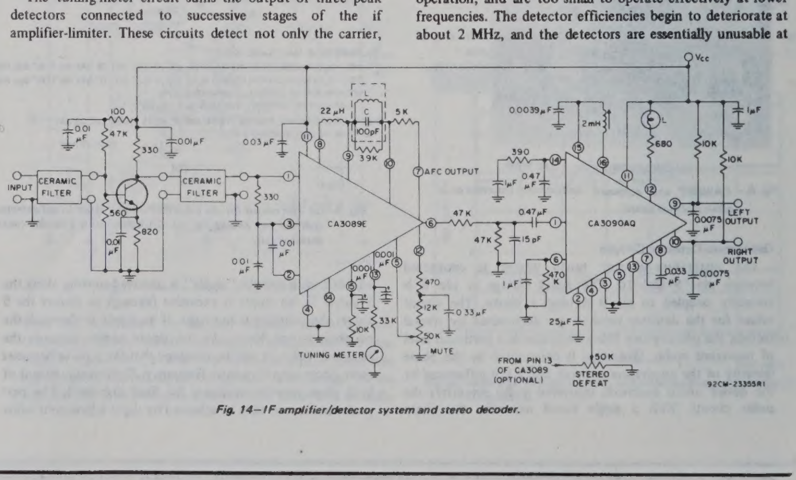

Fig. 14—IF amplifier/detector system and stereo decoder.

455 kHz without the use of external circuitry. The rf-AGC and mute logic circuits do not develop sufficient dc voltage to perform their functions, and the meter output signal loses its logarithmic characteristic and exhibits peaks and valleys as input signal is increased. Operation of the rf-AGC and mute logic circuits may be enhanced by the addition of a dc amplifier and inverter to each circuit. A simple example using a CA3096E IC transistor array is shown in Fig. 16.[3]

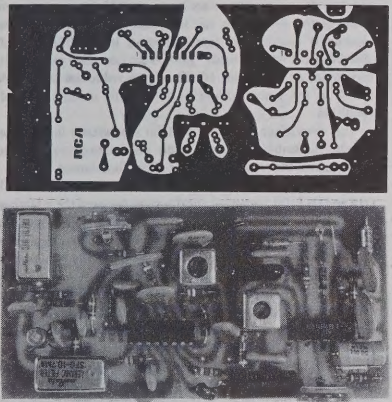

Fig. 15—Suggested PC-board pattern and parts layout for the circuit of Fig. 14.

The CA3089E may be used effectively in narrow-band communication receivers. In double-conversion receivers, some of the functions of the CA3089E are negated at a 455-kHz intermediate frequency. However, if a 10.7-MHz intermediate frequency is used, all of the auxiliary features may be used, but another set of problems is encountered. The small deviation signals encountered in narrow-band systems require the use of high-Q circuits in the quadrature detector, as indicated in Table I. However, variations in external-component parameters with temperature changes may cause the tuned frequency of the detector to drift out of the if pass band. Normally temperature-compensated components are necessary. The CA3089E, operating in conjunction with an inexpensive operational transconductance amplifier,[4,5] provides means of locking the tuned circuit to the incoming frequency. Fig. 17 shows the block diagram of such a system. The AFC output voltage developed across the resistor between pins 7 and 10 is amplified by the op-amp and drives a varactor to maintain the tuned frequency on the incoming-signal frequency.

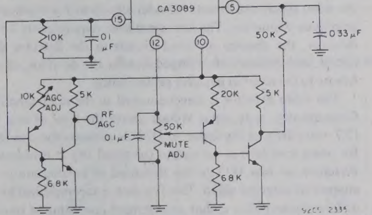

Fig. 16—External mute and rf-AGC drive circuits for the CA3089E operating at 455 kHz. External transistors are parts of the CA3096E n-p-n/p-n-p transistor array.

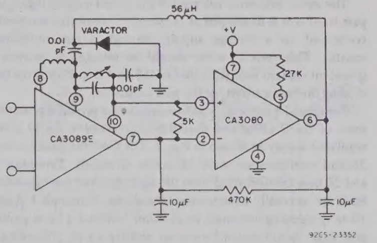

Fig. 17—Detector frequency-stabilization circuit.

The CA3089E may also be used as the core of an ultra-linear FM generator; Fig. 18 shows the circuit. The carrier is generated by the CA3089E with the introduction of feedback from the output terminal, pin 8. The carrier is modulated by the varactor connected across the tuned circuit at the input of the CA3089E. The varactor is driven by the output of the differential amplifier, A1, using a CA3028 IC.[6,7] This differential-amplifier stage is driven at one of its input terminals by the audio modulating signal. Negative feedback of the audio signal is provided by driving the other differential-amplifier input from the recovered audio output of the CA3089E at pin 6. The detector circuit uses a double-tuned transformer to produce audio with very little distortion at pin 6. This feedback technique results in a very low distortion modulation. The rf output of the CA3089E at pin 8 is essentially a square wave, and is fed to a tuned-amplifier stage to buffer the signal and restore the sine-wave-shaped rf output signal.

Acknowledgments

The author thanks Jack Craft for his aid and suggestions in many discussions and Frank Curley for his aid in circuit construction and collection of data.

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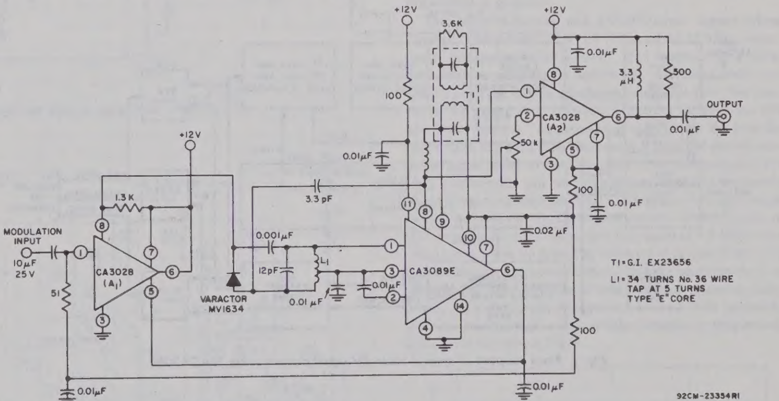


Fig. 18—FM generator circuit.

ICAN-6303

A Single IC for the Complete PIX-IF-System in TV Receivers

The RCA-CA3068 linear integrated circuit is a PIX-IF-subsystem in a shielded, quad-formed, dual-in-line, 20-lead, plastic package. This package contains all the active devices and most of the passive elements necessary for a high performance, PIX-if-system for a TV receiver. **This Note* describes** the receiver functions performed by the CA3068, and its application to color and monochrome T.V receivers.

Specifically, the receiver functions performed by the CA3068 are:

Video if amplification
Linear video detection
Noise-limited amplification of detected video
Keyed agc, with noise-immunity circuits
AGC delay for tuner rf stage
Buffered output signal to drive Automatic-Fine-Tuning (AFT) circuits
Amplification of intercarrier frequencies
Sound-carrier detection
Sound-carrier amplification
Zener reference diode for voltage regulation.

The only external components required for the operation of this if subsystem are bandwidth shaping networks, biasing networks, and a power supply. A functional block diagram of the signal portion of a typical color-TV receiver is shown in Fig. 1. A detailed block diagram of the CA3068, together with its peripheral tuned-circuits, is provided in Fig. 2.

This Note contains a detailed description of circuit functions within the integrated circuit, together with examples of the use of the CA3068 in PIX-IF amplifier PC-boards for color and monochrome TV.

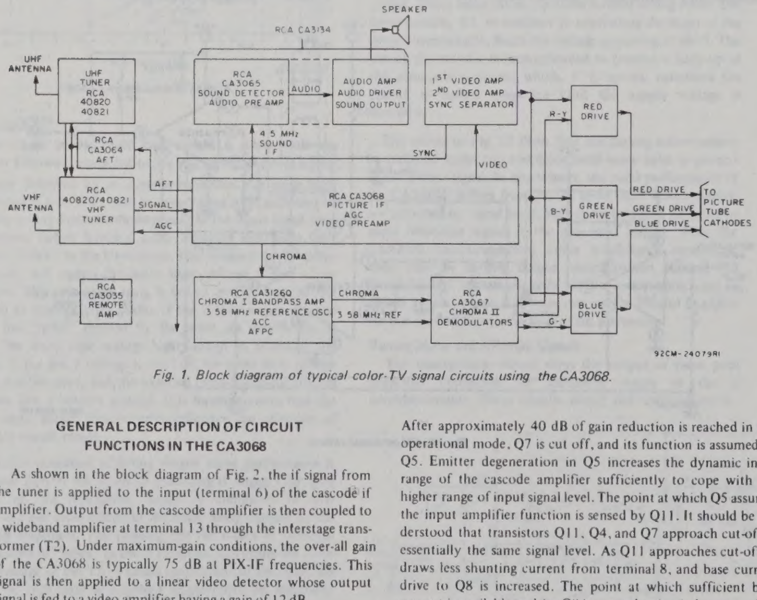

SPEAKER
RCA CA3134
UHF ANTENNA
UHF TUNER RCA 40820 40821
RCA CA3065 SOUND DETECTOR AUDIO PRE AMP
AUDIO
AUDIO AMP AUDIO DRIVER SOUND OUTPUT
1ST VIDEO AMP 2ND VIDEO AMP SYNC SEPARATOR
RED DRIVE
R-Y
RCA CA3064 AFT
4 5 MHz SOUND I F
SYNC
VIDEO
VHF ANTENNA
RCA 40820/40821 VHF TUNER
AFT
SIGNAL
AGC
RCA CA3068 PICTURE IF AGC VIDEO PREAMP
B-Y
GREEN DRIVE
RED DRIVE
GREEN DRIVE
BLUE DRIVE
TO PICTURE TUBE CATHODES
CHROMA
RCA CA3035 REMOTE AMP
RCA CA3126Q CHROMA I BANDPASS AMP 3 58 MHz REFERENCE OSC ACC AFPC
CHROMA
3 58 MHz REF
RCA CA3067 CHROMA II DEMODULATORS
G-Y
BLUE DRIVE
92CM-24079R1

Fig. 1. Block diagram of typical color-TV signal circuits using the CA3068.

GENERAL DESCRIPTION OF CIRCUIT FUNCTIONS IN THE CA3068

As shown in the block diagram of Fig. 2, the if signal from the tuner is applied to the input (terminal 6) of the cascode if amplifier. Output from the cascode amplifier is then coupled to a wideband amplifier at terminal 13 through the interstage transformer (T2). Under maximum-gain conditions, the over-all gain of the CA3068 is typically 75 dB at PIX-IF frequencies. This signal is then applied to a linear video detector whose output signal is fed to a video amplifier having a gain of 12 dB.

Bandpass shaping is accomplished by means of tuned-circuits preceding the input stage (terminal 6) and at the interstage circuit comprising input and output terminations via terminals 9, 12 and 13, as shown in Fig. 2. Terminal 16 is tied in at this point to provide loop bias for the input stages of the amplifiers connected to terminals 12 and 13. The agc voltage developed within the CA3068 is applied to its input stage by an external path from terminal 4 to terminal 6 through the input circuitry, as shown in Fig. 2. The developed agc is gated by a keying pulse applied to terminal 3 from the horizontal sweep circuit of the TV receiver. Delayed agc for the rf amplifier in the tuner is obtained from terminal 7; the delay is variable by adjustment of a resistance (25 kilohms) in series with the supply to terminal 8.

The zener reference voltage for the power-supply regulating pass-transistor is developed at terminal 18 when this terminal is connected to a voltage supply through a current-limiting resistor. This resistor value should be selected to provide a quiescent current into the zener of 0.5 to 1.5 milliamperes (excluding the base current for the pass transistor).

Terminal 15 is the dc input terminal that provides power for most of the CA3068 and should be connected to the 11.2-volt regulated supply as shown in Fig. 2. The CA3068 package has a 20-lead configuration with 18 active terminals. Terminals 11 and 20 have been omitted from the package; their corresponding leads are internally connected to the shield. Terminals 1, 5, and 10 are grounding terminals. In addition, terminal 17 is at ground potential. Additional information relative to dc grounding is given in the section concerning if design.

DETAILED CIRCUIT FUNCTIONS

Fig. 3 is a schematic diagram of the CA3068. The diagram is partitioned to facilitate the explanation of the circuit configuration and its functions.

The cascode input amplifier (first if) is a unique circuit designed for dual-mode operation. At low-level input signals, the buffer stages formed by Q3 and Q4 drive the base of the cascode-if amplifier composed of Q7 and Q6. Negative-going agc applied to Q3 (through an external connection to terminal 6) increases in proportion to the increase of the input signal level. After approximately 40 dB of gain reduction is reached in this operational mode, Q7 is cut off, and its function is assumed by Q5. Emitter degeneration in Q5 increases the dynamic input range of the cascode amplifier sufficiently to cope with the higher range of input signal level. The point at which Q5 assumes the input amplifier function is sensed by Q11. It should be understood that transistors Q11, Q4, and Q7 approach cut-off at essentially the same signal level. As Q11 approaches cut-off, it draws less shunting current from terminal 8, and base current drive to Q8 is increased. The point at which sufficient base current is available to drive Q8 into conduction is determined by an external-delay agc potentiometer connected in series with the V+ supply-lead and terminal 8. As Q11 cuts-off, the voltage increases at terminal 8, and current flowing into terminal 8 is diverted to the base of Q8. When Q8 starts to conduct, it turns on Q9 and Q10, thereby causing the open-circuit voltage at terminal 7 to drop and produce a negative-going agc voltage for the rf stage of the tuner. Q8 is also part of the if-agc feedback loop, and provides an increase in agc loop-gain. This increase compensates for the decrease in agc loop-gain that occurs when the cascode if amplifier is transitioned to its modified cut-off characteristic. After tuner gain reduction has reached its maximum, an additional 10 dB of gain reduction can be obtained in the cascode-amplifier under this modified cut-off condition.

This reverse-agc system is used for the cascode input stages because the stability achieved under maximum-gain conditions is maintained throughout the range of agc functioning.

The wideband if amplifier consists of transistors Q12, Q13, Q14 and Q15. Q12 serves as a buffer stage between the interstage tuned-circuits and the automatic-fine-tuning (AFT) output-signal terminal. The actual if signal amplification takes place in Q13, Q14 and Q15, which effectively serve the function of second and third PIX-IF stages. Transistor Q15 is the driving source to Q17, the video detector. This driving source impedance is approximately 500 ohms as a result of the degenerative feedback loop through Q16. The feedback network also extends the 3-dB-down frequency response to beyond 70 MHz. It is this low detector-driving-point impedance and the absence of a tuned-circuit at this interstage point that contribute to the superior performance of the detector system. In most conventional detection systems, the detector is driven from a high-impedance source involving a double-tuned interstage transformer with unequal primary and secondary Q's. In such a system, variations in detector impedance (caused by normal video excursions) can produce significant phase shifts that adversely affect color fidelity. In the CA3068, the untuned, low-impedance detector drive circuit produces a nearly optimum condition for the detector circuit.

The detector circuit consists of transistor Q17 and its biasing network Q18, Q19 and R20. Q18 is biased to the same potentials as Q17 because the bases are tied together through the resistance element of the low-pass filter that consists of R19 and C3. R20 and C4 form a conventional peak detector in which the time constants are selected for optimum detector efficiency and desired video bandwidth. This system detects chroma subcarrier without introducing differential phase errors as a function of the video signal, and detects the video signals with a minimum of amplitude distortion. The low signal-level requirements for the detector, the absence of tuned-circuits in the detector drive circuit, and the low source impedance for the detector, all contribute to the superior detector performance.

The video detector is direct-coupled to the video amplifier. Consequently, a dc input voltage above the level of one V_{be} (0.7 volt) drop at the input to Q23 determines the condition for white level (dc) at the output (terminal 19). It is necessary, therefore, to bias Q23 to the threshold of conduction in the absence of detected video. This function is accomplished by the differential-amplifier circuit arrangement consisting of transistors Q20 and Q21. In the absence of signal, the dc potentials at the emitters of Q20 and Q21 are identical. The current through Q20 must equal the current through Q21 because R25 is similar in value to (R27 + R28). This current also flows through D3 (which has the same geometry as Q22). Consequently, Q22 carries all the current supplied by Q20, and no current is available for the base of Q23, so that Q23 is held on the edge of conduction. When an rf carrier is present, the current in Q20 increases in direct proportion to the carrier level; however, the current in Q21 remains fixed. When the current increases in Q20, this increase can only flow to the base of Q23. Since the current in Q23 is directly proportional to its base current flow, a corresponding increase in current through Q20 as a result of rf carrier detection produces a video output at terminal 19.

As the video carrier signal increases, the dc level at the base of Q23 increases, and there is an accompanying decrease in the dc level at the base of Q25 and, consequently, at terminal 19. With a sufficiently strong rf signal, the current through Q23 and R29 increases such that the base voltage of Q25 is driven toward dc ground. The "bottoming" level at terminal 19 under nominal signal conditions is locked to about 0.8-volt as a result of the high loop gain of the agc system. Any further increase in the signal, after "bottoming" is reached, will be clipped. This operational feature serves as a highly effective mechanism to limit impulse noise.

When a signal is present at the input, the composite video signal at the base of Q25 appears at terminal 19 through the Darlington connection to the emitter of Q26. The sync tips in

*This Note, revised by Maurice Caputo (Solid State Division), was orginally prepared by S. Reich and R. T. Peterson.

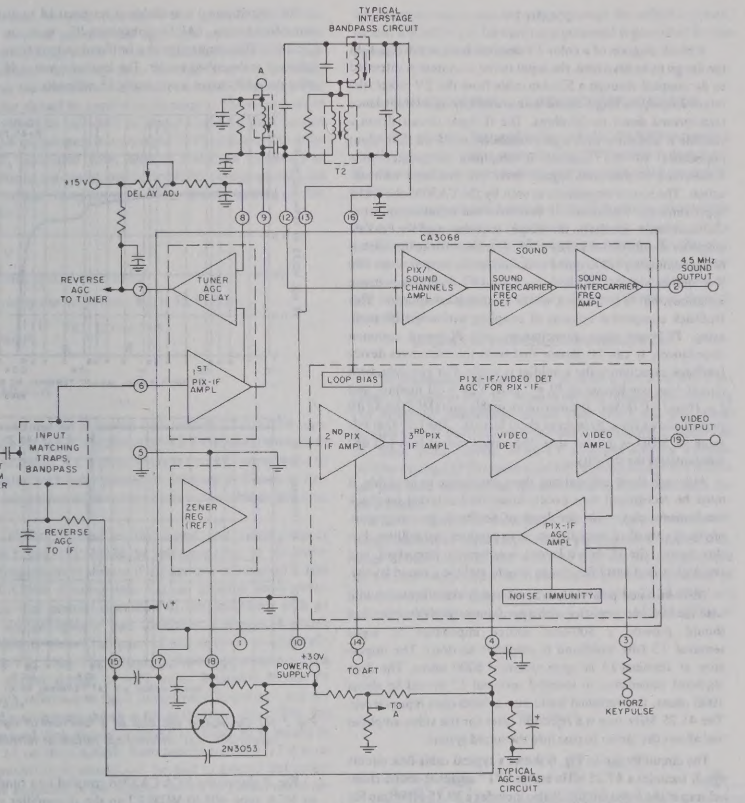


Fig. 2. Detailed block diagram of the CA3068 together with its peripheral tuned circuits.

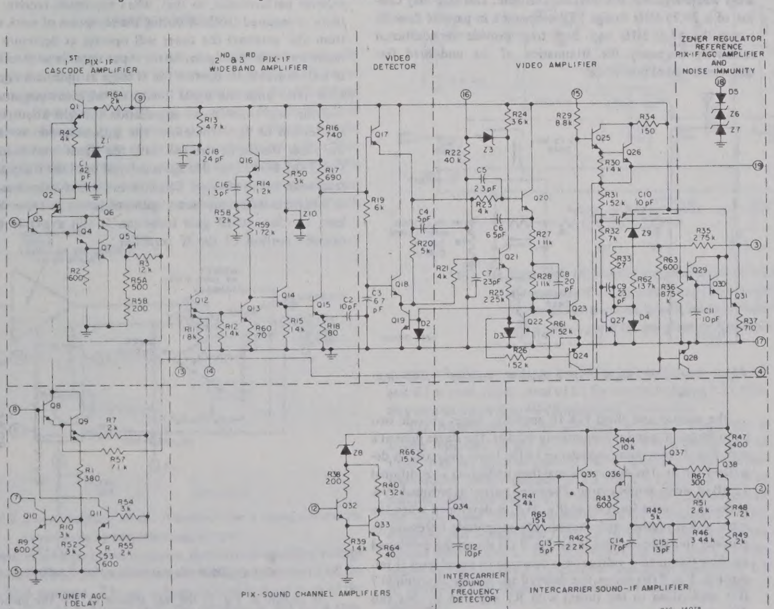

1ST PIX-IF CASCODE AMPLIFIER
2ND & 3RD PIX-IF WIDEBAND AMPLIFIER
VIDEO DETECTOR
VIDEO AMPLIFIER
ZENER REGULATOR REFERENCE PIX-IF AGC AMPLIFIER AND NOISE IMMUNITY
TUNER AGC (DELAY)
PIX-SOUND CHANNEL AMPLIFIERS
INTERCARRIER SOUND FREQUENCY DETECTOR
INTERCARRIER SOUND-IF AMPLIFIER
92CL-24078

Fig. 3. Schematic diagram of the CA3068.

this composite waveform drive the keyed agc amplifier Q27, which in turn drives Q28. Without a video rf signal there is no video signal output, and Q27 conducts during the keying intervals (the horizontal pulse is connected to terminal 3). As the detected signal level increases in amplitude and the output voltage at terminal 19 approaches its typical operational level of 7 volts peak-to-peak, the peak potential at the base of Q27 begins to fall below 0.8 volt. Under these conditions, the keying current formerly channeled through Q27 is diverted through diode D4. As the signal level rises even higher, a greater portion of the Q27 collector current is diverted through D4, and the base current to Q28 is proportionately increased. A 10-microfarad capacitor is normally connected between terminal and ground and is, by this connection, put in shunt with Q28. The charge on this external capacitor is maintained through a bleeder resistor to V+. As the base current to Q28 increases, Q28 discharges the capacitor at a rate that is proportional to the base current of Q28. Integration of the total charge on the capacitor over the keying interval yields a dc level (agc voltage) that is inversely proportional to the incoming signal level; i.e., agc voltage approaches zero as the signal increases.

Any high-performance agc system must have noise-immunity characteristics in order to avoid the establishment of false agc levels. AGC voltage developed from random noise can produce "wash-out", "blank raster" and/or a momentary "loss of sync". The CA3068 is designed with an improved noise-immunity circuit that essentially removes the keying current during periods of high noise input. The active devices responsible for providing protection against this deleterious effect of the impulse noise are the "noise detector", Q29, and the "noise clamp" Q31, which is driven by Q30. Impulse noise is channeled through the high-pass filter network consisting of C10 and R36 to the detector input Q29. Q29 and C11 comprise a conventional peak detector. The dc level across C11, which is proportional to the level of impulse noise, turn on Q30 and Q31, thereby clamping the keying supply voltage (terminal 3) to ground. In actual operation, the terminal-3 supply has a series resistance that is large enough to limit the peak current into the zener diode (Z5) to approximately 0.8 milliampere. When Q31 conducts, it shunts this current to ground.

The sound-if-channel and PIX-IF-channel signals whose "carrier" frequencies are 41.25 MHz and 45.75 MHz, respectively, are applied to terminal 12. Q32 functions as a buffer between the interstage-tuned-circuits associated with terminal 12 and the PIX/sound-channels amplifier, Q33. The intercarrier frequency (the difference frequency between the PIX and sound "carrier" frequencies) is detected by the peak detector Q34 and C12. The resultant 4.5 MHz FM sound-intercarrier signal is fed to transistor Q35. This transistor and Q36 form a differential pair that provides an amplified intercarrier sound-if signal to the base of Q37. A feedback system through the RC networks in the Darlington emitter-follower output of Q37 provides bandpass shaping in the region of 4.5 MHz while maintaining a low dc gain. The low level of dc gain is desirable because the circuit receives its bias in an open-loop manner from terminal 16. The bandpass of this amplifier system is fairly broad, and even though it is optimized for 4.5 MHz operation, there is relatively high output at other intercarrier frequencies, as shown in the curve in Fig. 4.

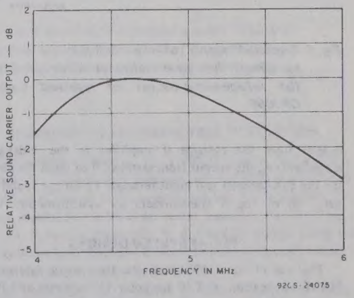


Fig. 4. Relative sound-carrier output as a function of frequency.

The internal zener reference-diode consists of the series diode arrangement shown connected between terminal 18 and the substrate in Fig. 3. A regulator-circuit configuration showing the pass transistor interconnected with the reference diode is given as part of the color and monochrome if amplifier circuits that are discussed in the following paragraphs. Similarly, the regulation curves shown in Figs. 5 (a) and 5 (b) are discussed below in more detail. It should be noted that (with a heat sink for the 2N3053 and a lower value for the resistor in series with the collector) the regulated voltage from this supply may be used to provide power to other circuits in addition to the CA3068.

The distribution of tuned circuits around the CA3068 amplifier circuit is a matter of preference of the circuit designer. In general, a total of five tuned circuits will be required subsequent to the mixer for proper selectivity and bandpass shaping. In addition, at least one 47.25 MHz adjacent sound-channel and one 41.25 MHz sound-channel trap will be required. The systems to be discussed in this Note are designed to be driven from a single tuned circuit connected to the mixer output. In addition, both the color and monochrome if systems described subsequently utilize tuned circuits at the input and output to the cascode amplifier. The second transformer is used to couple output from the cascode if amplifier to the wideband if amplifier (i.e., the output from terminal 9 to input terminal 13 for the PIX-channel and input terminal 12 for the sound-channel). All of the if transformers are synchronously tuned.

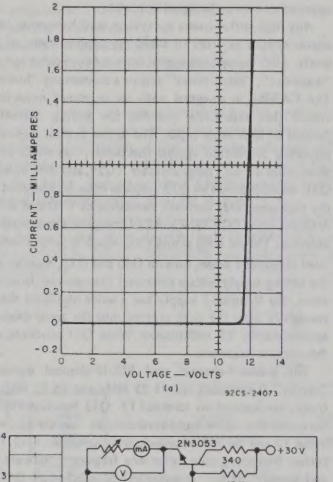


Fig. 5. Regulated supply of the CA3068: (a) voltage-versus-current for zener reference diode of CA3068; (b) voltage-versus-current for regulated supply of CA3068.

PIX–IF SYSTEM DESIGNS

The use of the CA3068 in the two major categories of PIX-IF application, PIX-IF for color-TV receivers and PIX-IF for monochrome receivers, is described below. To illustrate the use of the CA3068 in a tuner requiring "reverse" agc action, the rf-stage of the tuner employed in the PIX-IF for color-TV receiver contains a MOSFET. In contrast, the rf-stage of the tuner employed in the PIX-IF for the monochrome receiver makes use of a bipolar transistor in a "forward" agc arrangement.

COLOR TV

A block diagram of a color-TV receiver is shown in Fig. 1. In the design to be described, the input to the if system is intended to be coupled through a 50-ohm cable from the TV mixer; the mixer employs a single tuned-output coil having an impedance transformed down to 50 ohms. The if input circuit drives a cascode if amplifier with a gain capability of 35 dB. The input impedance to the cascode if amplifier is greater than 4000-ohms at minimum signal levels and increases with agc action. The source impedance as seen by the CA3068 should be approximately 500 ohms to dominate the input-circuit conductance node. Similarly, the output impedance of the cascode amplifier should be loaded by a tuned circuit with an impedance of approximately 3000 ohms to dominate the output node. The if amplifier stability is then unaffected by the IC impedance variations, but is a function of the feedback component. This feedback component consists of coupling within the IC packaging, PC-board stray capacitances, and PC-board common impedances. It can be shown that with the maximum device feedback capacitance the amplifier is stable. For example, with circuit bias conditions of I9 = 2 mA, Y21 = 50 mmhos, and C_{fb} (max) = 0.005pF, the maximum usable gain (MUG) is 42 dB (which allows for a 20 percent skew factor). The fact that this value of MUG is greater than the actual circuit gain (35 dB) substantiates the stability.

Although these calculations show the device to be stable, it must be recognized that poorly controlled external feedback mechanisms may raise the level of feedback in a high-gain, physically small rf amplifier so as to produce instabilities. For this reason, the PC-board layout is extremely important, and any high-gain if amplifier design should include a board layout.

As mentioned previously, the interstage transformer should load the cascode amplifier with approximately 3000 ohms, and should provide a 500-ohm source impedance to input terminal 13 (the wideband if amplifier section). The impedance at terminal 13 is approximately 5000 ohms. The driving-point impedance to sound-if terminal 12 should be about 1000 ohms, this terminal looks into a 5000-ohm input circuit. The 41.25 MHz trap is a rejection filter for the video amplifier and allows the carrier to pass into the sound system.

The circuit design in Fig. 6 shows a typical cable-link circuit which includes a 47.25 MHz bridged "T" adjacent-sound-channel trap at the input circuit. It also includes a 39.75-MHz trap for an adjacent video carrier for operation in CATV systems or in areas where adjacent channels are available. This trap may consist of a 39.75-MHz bridge "T" connected in parallel directly across the 47.25-MHz trap. Both traps provide the additional selectivity necessary for attenuation of the undesired frequencies by more that 40 dB.

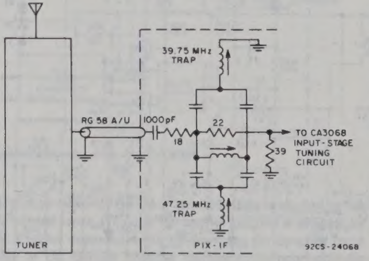


Fig. 6. Schematic diagram of a typical tuner-to- PIX-IF link circuit.

The second and third PIX-IF amplifier stages provide two extra stages of gain (approximately 40 dB). The stages present a very low driving-point impedance to the linear detector, as described earlier. The detected signal then undergoes an additional 12 dB of video amplification. The video output at terminal 19 is nominally 7 volts (peak-to-peak). AGC is developed when the input signal reaches and exceeds the magnitude necessary to produce this video output level. Fig. 7 (a) shows the developed agc bias (terminal-4 voltage) as a function of signal level at terminal 6. Fig. 7 (b) shows the delayed agc voltage at terminal 7 (for application to the tuner) with R1 adjusted so that this delay-bias is generated whenever the input signal at terminal 6 exceeds 8 millivolts.

An output signal is available at terminal 14 to drive an automatic-fine-tuning (AFT) subsystem-IC, such as the RCA CA3064. This connection is a buffered output from an emitter follower as described earlier. The level of signal at 45.75 MHz to drive the AFT circuit is nominally 15 millivolts.

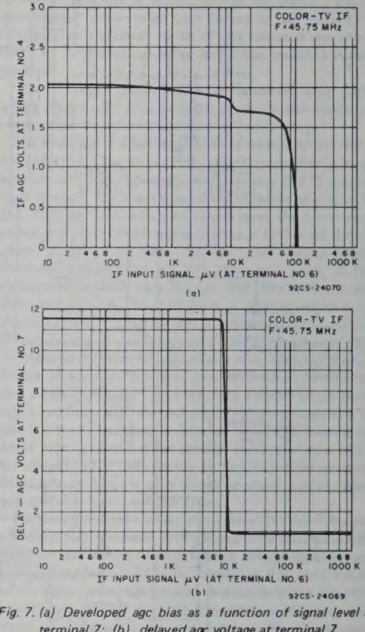


Fig. 7. (a) Developed agc bias as a function of signal level at terminal 7; (b) delayed agc voltage at terminal 7.

Fig. 8 shows the RCA CA3068 coupled to a tuner that uses an RCA type 40820 MOSFET in the rf-amplifier stage. AGC voltages are applied (shown in Fig. 8) to optimize over-all TV-receiver performance, so that, when maximum receiver sensitivity is required (such as during the reception of weak signals from the antenna) the tuner will operate at optimum noise factor and maximum gain. As the input signal level increases, it is still desirable to operate the rf stage at optimum signal-to-noise ratio until the signal level is of sufficient magnitude to override any tuner noise degradation brought about by the application of agc. Therefore, the gain-reduction voltage to the tuner should be delayed until the signal level builds up. Fig. 7 (b) shows that this agc is delayed until the if **signal level** reaches an 8-millivolt level. Then the tuner-gain-reduction mode is initiated. After the tuner gain reduction is expended, at least another 10-dB gain reduction is still available in the cascode portion of the if amplifier.

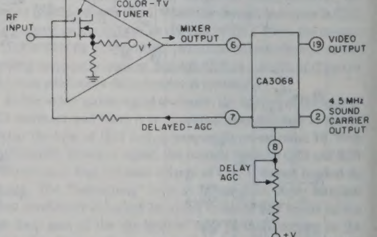


Fig. 8. Block diagram of a color if system.

As shown in Fig. 2, the agc system is, for the most part, self-contained. An optimized agc response characteristic can be achieved by use of a high-quality tantalum 10-microfarad capacitor connected between terminal 4 and ground. An RC decoupling network smooths the agc ripple associated with the charge and discharge of the 10-microfarad capacitor at the horizontal-oscillator frequency rate. The agc system is normally keyed from the horizontal-output circuit in the TV system. This keying pulse should be applied to terminal 3. The magnitude of the pulse should be sufficient to supply a nominal peak current value of 0.8 milliampere into terminal 3. The value of the series resistor R_s associated with terminal 3 may be computed as follows: During the conduction period (with keying applied), the constant-voltage components within the integrated circuit account for:

$V_k = 8.2$ V

(It is assumed that $I3 = 0.8$ mA)

If the keying-pulse magnitude, V_p, is 15 V, then:

$$I3 = 0.8 \text{ mA} = \frac{15 - V_k}{R_s} = \frac{(15 - 8.2)\text{ V}}{R_s}$$

$R_s = 8.5$ kilohms

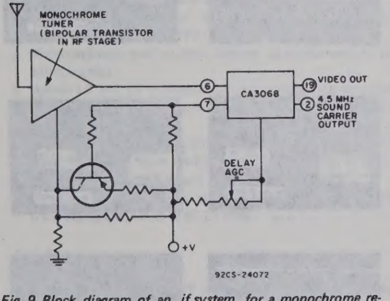
The sound output is derived from terminal 2 at a level compatible with the input requirements of a TV-sound-if-subsystem IC, such as the RCA CA3065. There is also a dc component of approximately 6.7 volts present at terminal 2. Coupling networks to subsequent circuits must contain a suitable dc-blocking capacitor.

Small chokes located in the sound and video outputs (terminals 2 and 19) should be self-resonating at the intermediate frequencies to prevent if leakage into subsequent stages.

The CA3068 if subsystem has an internal zener reference-diode that permits operation of the subsystem with an external voltage-regulator pass transistor. A suggested circuit arrangement is shown as part of the over-all if schematic diagram in Fig. 5 (b). The voltage-regulator pass-transistor has a nominal output voltage of 11.2 volts. Bypassing of the V+ supply with reference to the if subsystem is important, and the suggested arrangement shown in the application circuit (Fig. 10) should be used. Specifically, terminal 15 should be bypassed to terminal 17 on the CA3068. Even though terminal 17 is at dc ground potential, it should not be tied to ground but rather should be bypassed in the manner shown to avoid mutual impedance coupling within the CA3068.

MONOCHROME TV

The delayed-agc circuits used in the CA3068 were originally intended to control a MOSFET in the rf-stage of the TV tuner. This arrangement permits direct application of the delayed-agc voltage from the CA3068 to the tuner. In monochrome receivers, however, it is common practice to employ a bipolar transistor in the rf-stage of the tuner, and a circuit with a "forward"-agc characteristic is required to control the rf-stage. This characteristic is easily established by means of an inverter network utilizing a p-n-p transistor, as shown in the circuit of Fig. 9.



MONOCHROME TUNER (BIPOLAR TRANSISTOR IN RF STAGE)
CA3068
6
7
19
VIDEO OUT
2
4.5 MHz SOUND CARRIER OUTPUT
DELAY AGC
+V
92CS-24072

Fig. 9. Block diagram of an if system for a monochrome receiver showing peripheral agc circuit.

As the input signal level increases, the forward-agc delay voltage is developed at the tuner when the voltage at terminal 7 of the CA3068 decreases. The agc voltage applied to the rf-stage of the tuner (Fig. 9) is derived from the collector of the p-n-p transistor. As the delay-agc voltage is generated at terminal 7 of the CA3068, the base of the p-n-p inverter is driven into conduction, which causes more current to flow through the collector circuit, so that a positive (or forward) agc potential is generated for the bipolar transistor in the tuner.

TV RECEIVER PIX–IF CIRCUIT APPLICATIONS

In this section, the application of the CA3068 integrated circuit in a color and a monochrome TV receiver is described. The circuits shown were constructed on single-sided copper PC boards.

As previously noted, because of the high gain encountered in PIX-IF design, positive feedback must be avoided if the amplifier is to remain free of spurious oscillation. To this end, the optimization of printed board layout and component placement is essential. The proper choice of bypassing components and signal-path layout is necessary to avoid feedback through ground loops.

IF CIRCUIT FOR COLOR TV RECEIVER

The schematic diagram of an if system for a color-TV receiver is shown in Fig. 10. A parts list and illustrations showing the PC-board component layout (top view) and the actual printed circuit (bottom view of board) are shown in Appendix A. Since most current color-TV receivers employ automatic-fine-tuning (AFT) systems, an AFT system using the CA3064 has also been included on the same board; Fig. 10 includes the AFT circuit.

The if-response is determined by the triple-tuned circuit, which consists of three traps: two preceding the IC and an interstage double-tuner circuit with one trap. In the tripled-tuned circuit, the two bridge-T traps are used to provide attenuation of the adjacent-channel picture carrier (frequency 39.75 MHz) and adjacent-channel sound carrier frequency (47.25 MHz). A common bridge impedance consisting of parallel-connected L1 and R2 is used. Adjustment of L1 for best null of the 47.25 MHz trap assures the desired 60-dB minimum attenuation.

The triple-tuned circuit provides, at center frequency, a source resistance to the IC of 800 ohms and a voltage gain of three from the input to pin 6 of the IC. The first section of the triple-tuned circuit consists of L2 and C6. Capacitor C6 is in parallel resonance with coil L2 at 44 MHz. The third section of the triple-tuned circuit consists of coil L4 and capacitor C14. Coupling and voltage-gain from L2 to L4 are provided by the second section, coil L3 and capacitors C10, C11, and C12. The inductive reactance of L3 is made 75 times larger than that of L2 to provide a high degree of tuned-circuit isolation for ease of alignment.

The circuit provides protection against interference resulting from a strong rf signal which might inadvertently be introduced between the tuner and the if stage. Parasitic resonance and couplings have been minimized to maintain a high degree of attenuation at frequencies remote from the if-resonance frequency.

The interstage double-tuned bandpass circuit, with a bifilar T-trap at 41.25 MHz, is similar to that commonly used in the third stage of color-TV receivers. The sound and picture carriers are present at the input (terminal 12) to the 4.5 MHz sound-if detector circuit. Trapping action removes the 41.25 MHz sound carrier at terminal 13 to prevent a difference-frequency beat of 0.92 MHz with the chroma subcarrier at 42.17 MHz. The picture carrier and chroma subcarrier entering terminal 13 are amplified, detected, and additionally amplified as detected video signal. If the sound carrier is not attenuated by the 41.25 MHz trap, the carrier will be detected as a large 4.5 MHz difference-signal in the video output. A 4.5 MHz trap (T5) is included to prevent interference of a residual 4.5 MHz intercarrier signal in the chroma and luminance circuits.

The chroma peaking circuit compensates for the slope of the video response, as shown in Figs. 11 (a), 11 (b) and 11 (c). The actual slope and shape of the video response between 3.08 MHz and 4.08 MHz will vary because of normal component tolerance. The chroma-peaking coil, L7, has two cores, one to adjust inductance to center the response at 3.58 MHz, and the other to adjust chroma output level and bandwidth. The latter core controls circuit Q with little effect on over-all inductance.

Photographs of the detected sweep-response characteristics are shown in Fig. 12. The sweep-response of Fig. 12 (f) shows the interstage alignment from TP3 (of Fig. 10) to terminal 9 of the CA3068. The sweep-response curves in Figs. 12 (a) through 12 (e) show 60 dB of agc range from a level of 100 microvolts (Fig. 12 (e)) to 100 millivolts (Fig. 12 (a)).

The alignment procedure for the color-TV PIX-IF system using the CA3068, Fig. 10, is given in Appendix A.

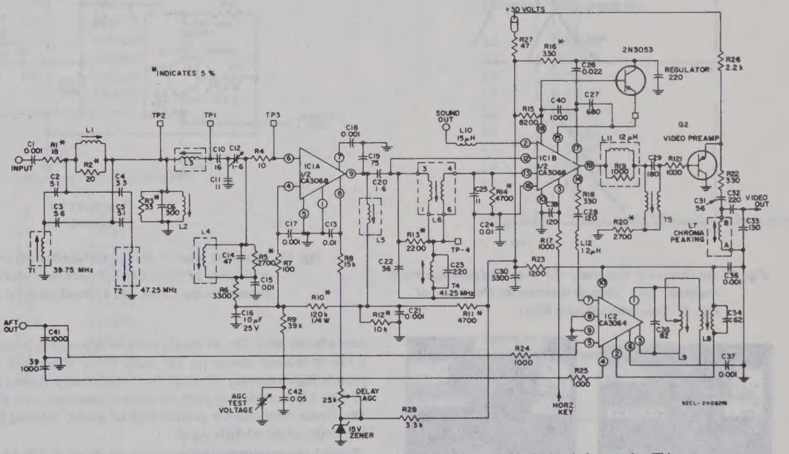


Fig. 10. Schematic diagram of a typical application of the CA3068 to a PIX-IF circuit for a color-TV system. A template of the printed circuit board used to construct this circuit, a diagram of the position of all components on the board, a block diagram of the location of major components on the board, and a circuit parts list are given in Appendix A.

IF CIRCUIT FOR MONOCHROME TV RECEIVER

The schematic diagram for a PIX-IF system for a monochrome TV system that employs the CA3068 is shown in Fig. 13. A PC-board component-layout diagram (top view), the actual printed circuit (bottom view of board), and a circuit parts list are shown in Appendix B. A sound-if system using the CA3065 has been included to show the simplicity with which it can be used in conjunction with the CA3068.

The selectivity is provided in two sections, an input single-tuned circuit with trap, and a double-tuned interstage circuit. The resistive pad, R1, R2, and R3 of Fig. 13, is used to terminate the link-cable and isolate cable effects from the high-Q input circuit. The bridge-T trap-circuit is used to give maximum attenuation to the adjacent-channel sound carrier. Precision components (R2, C1, C2) achieve a good null at 47.25 MHz without the need for additional components. The circuit Q is controlled by R11 and the resistive input network to yield a 3-dB bandwidth of 3 MHz centered at 44.5 MHz. The "T"-equivalent circuit is used for interstage coupling to realize a miniature, precision, double-tuned transformer. The mutual coupling element, L5, is an air-core, spring-winding coil which is actually calibrated by physical dimensions. If necessary, this coil may be "knifed" to provide a simple and effective coupling adjustment. The circuit Q's are each set at 21, and are controlled by R17 and R18, which also feed bias for the broadband amplifier and sound channels, respectively. The picture-carrier at 45.75 MHz is set at 50 percent to yield proper reception of the vestigial sideband. The color subcarrier at 42.17 MHz is placed comparatively low on the response curve, since the resulting beat with the 41.25 MHz is placed at greater than 5 percent but less than 10 percent to produce an adequate sound-if intercarrier signal at 4.5 MHz, and yet maintain low intermodulation. Typical over-all sensitivity of the if circuit is approximately 150 microvolts for full video output.

Interference from the 45-MHz high-level signals and harmonics is prevented by care in passing and filtering. A 12-microhenry choke (L4 of Fig. 13), self-resonant at the fourth harmonic, is used in the video output lead; the sound output contains a ferrite bead. The B+ supply must be bypassed to provide a low-impedance source for the video driver stages and to provide high-frequency filtering. The 1-microhenry choke (L3 of Fig. 13) is made very lossy to prevent resonance with C8. The ferrite bead and C9 provide high-frequency filtering for harmonics of the 45-MHz signal.

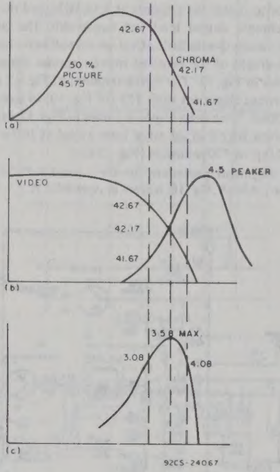


Fig. 11. (a) Over-all if response, (b) video and peaking circuit response, (c) chroma response for the circuit of Fig. 10 (frequency values in MHz).

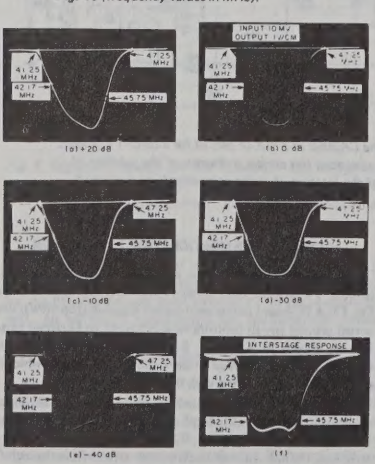


Fig. 12. Detected sweep-response characteristics for the circuit of Fig. 10.

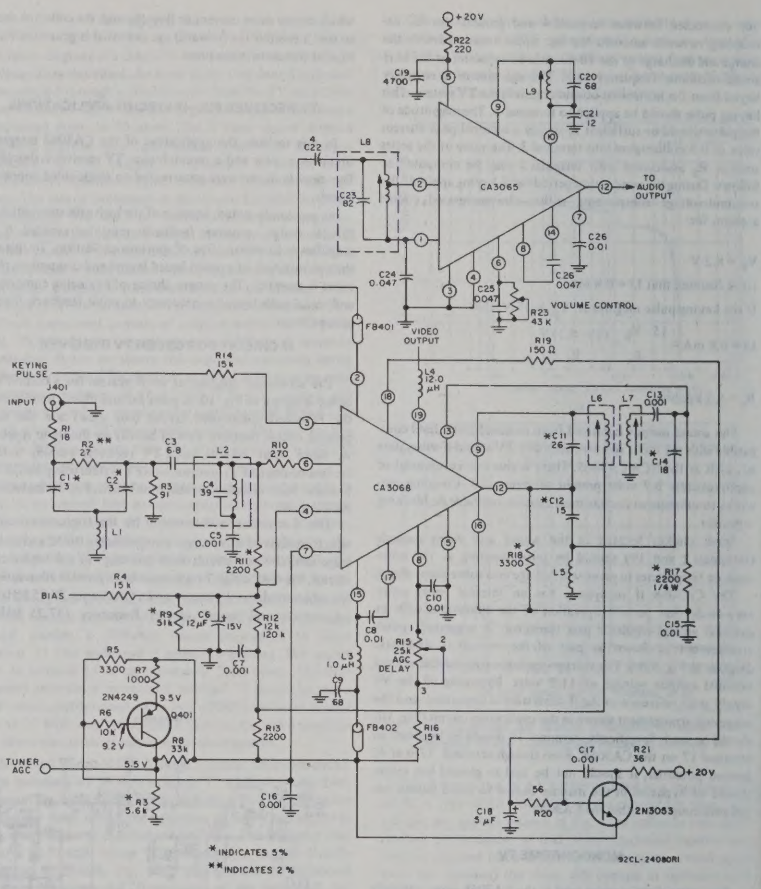


Fig. 13. Schematic diagram of a typical application of the CA3068 to a PIX-IF circuit for a monochrome-TV system. A template of the printed-circuit board used to construct this circuit, a diagram of the position of all components on the board, and a circuit parts list are given in Appendix B.

Typical sweep-response characteristics are shown in Fig. 14. The alignment instructions for the monochrome, PIX-IF circuit are given in Appendix B.

SUMMARY

A complete if subsystem has been described for use in both color and monochrome TV receivers. The only signal inputs required by the CA3068 are if signals from the tuner and a keying pulse from the horizontal circuitry. The CA3068 provides all outputs needed to drive the video output stage, delay line, sync-separator circuitry, RCA CA3065 sound if subsystem, RCA CA3064 AFT subsystem, and delayed-agc voltage for the rf stage in the tuner. Additionally, circuits for noise immunity and signal overload protection are an integral part of the CA3068 design. These subsystems have typical input sensitivities of 100 microvolts for a 4-volt, peak-to-peak video output. A unique video detector arrangement provides extremely linear output throughout the 7-volt, peak-to-peak, video-output range of the system.

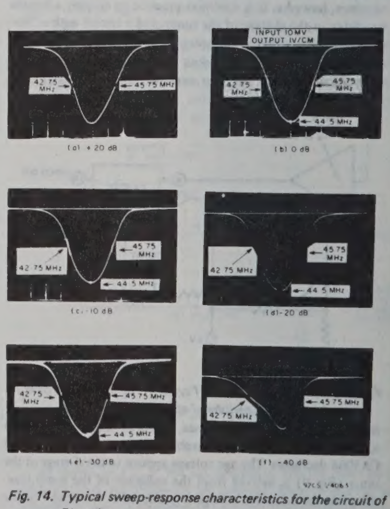


Fig. 14. Typical sweep-response characteristics for the circuit of Fig. 13.

Although this Application Note describes subsystem designs in TV receivers, the CA3068 is also applicable in AM communications systems requiring performance at frequencies within the range of 10 to 70 MHz.

REFERENCES

1. RCA Data Bulletin File No. 396 concerning the CA3064 and CA3064E, "TV Automatic Fine Tuning Circuit", or the RCA DATABOOK, 1975 Series SSD-201C.
2. RCA Data Bulletin File No. 412 concerning the CA3065, "TV IF Sound System", or the RCA DATABOOK, 1975 Series SSD-201C.
3. RCA Data Bulletin File No. 467 concerning the CA3068, "Television Video IF System", or the RCA DATABOOK, 1975 Series SSD201C.

APPENDIX A – THE COLOR CIRCUIT

ALIGNMENT PROCEDURE FOR THE COLOR CIRCUIT

Preliminary Adjustments and Calibration

1. Adjust delay-agc (noise pot) fully cw.
2. Connect supplies as indicated on schematic diagram (Fig. 10), set bias to zero.
3. Set sweep generator to 10 millivolts as indicated on Boonton 91DA meter with 56-ohm termination.

Step 1 - IF Interstage Alignment

a. Ground TP1 with short clip lead.
b. Connect sweep generator with 56-ohm termination and 1000-picofarad decoupling capacitor to TP3.
c. Connect oscilloscope to video output.
d. Adjust bias for 5-volt peak-to-peak response on oscilloscope.
e. Adjust bottom core of T4 for minimum at 41.25 MHz.
f. Adjust L5 and L6 for symmetrical response with PIX and color markers equal (Fig. 12 (a)): L5 controls markers and L6 controls tilt.
g. Adjust top and bottom cores of T4 simultaneously, top core for maximum rejection of 41.25 MHz and bottom core to maintain minimum 41.25 MHz.

Step 2 - IF Overall Alignment

a. Leave ground clip lead on TP1.
b. Remove sweep input from TP3.
c. Connect TP2 through a 1000-picofarad capacitor to TP3.
d. Connect sweep generator to input.
e. Readjust variable bias to maintain 5-volts peak-to-peak response on oscilloscope.
f. Adjust T1 for minimum 39.75 MHz.
g. Adjust T2 for minimum 47.25 MHz.
h. Adjust L2 for equal height of PIX and color markers.
i. Remove ground-clip lead from TP1 and 1000-picofarad capacitor from between TP2 and TP3.
j. Maintain 5-volts peak-to-peak response on oscilloscope by re-adjusting bias.
k. Adjust L3 and L4 simultaneously for symmetrical response with PIX and color markers equal: L4 controls markers and L3 controls tilt.
l. Adjust bandpass trimmer, C12, to place PIX and color markers at 40 percent while readjusting L3 and L4 (Fig. 12 (b)).
m. Re-adjust T1 for minimum at 39.75 MHz if necessary.
n. Re-adjust T2 for minimum at 49.25 MHz. Then adjust L2 to maximize the rejection at 47.25 MHz.

AFT Alignment

a. With oscilloscope on AFT output, adjust bias for 10-volts peak-to-peak response.
b. Adjust L8 for maximum 45.75 MHz.
c. Adjust L9 for crossover at 45.75 MHz.
d. Re-adjust L8 and L9 to obtain symmetry.
e. Adjust L8 to obtain maximum width.

Color-Circuit Parts List

Capacitors		Resistors (All values in ohms)	
C1	0.001μF	R1	18
C2	5.1pF	R2	20
C3	5.6pF	R3	33
C4	3.3pF	R4	10
C5	5.1pF	R5	2.7k
C6	300pF	R6	3.3k
C10	16pF	R7	100
C11	11pF	R8	15k
C12	1-6pF	R9	39k
C13	0.01μF	R10	120k
C14	47pF	R11	4.7k
C15	0.01μF	R12	10k
C16	10μF	R13	2.2k
C17	0.001μF	R14	4.7k
C18	0.001μF	R15	8.2k
C19	7.5pF	R16	330
C20	1.6pF	R17	1k
C21	0.001μF	R18	330
C22	3.6pF	R19	1k
C23	220pF	R20	2.7k
C24	0.01μF	R21	1k
C25	11pF	R22	330
C26	0.022μF	R23	1.2k
C27	680pF	R24	1k
C28	120pF	R25	1k
C29	180pF	R26	2.2k
C30	0.022μF	R27	47
C31	56pF	R28	3.3k
C32	220pF	R29	25k
C33	130pF		
C34	62pF		
C35	82pF		
C36	0.001μF		
C40	1000pF		
C41	1000pF		
C42	1000pF		

Inductors	RCA Stock No.
L1	132159
L2	132161
L3	132839
L4	132658
L5	137126
L6	132146
T1	132839
T2	132157
T4	132150
T5	132135

APPENDIX B – THE MONOCHROME CIRCUIT

ALIGNMENT PROCEDURE FOR THE MONOCHROME-CIRCUIT

Step 1 -

1. Connect +20 volts to appropriate points on board.
2. Connect sweep generator to input
3. Connect dc bias voltage to appropriate point on board.
4. Adjust sweep generator for 10-millivolt input.
5. Adjust bias voltage for 5-volt, peak-to-peak output.

Step 2 -

1. Adjust LT for minimum response at 47.25 MHz.
2. Adjust L2 for maximum at 44.5 MHz.
3. Adjust L6, L7 for bandpass shown in Fig. 14 (b). The curve should have 3-MHz bandwidth centered at 44.5 MHz.

Monochrome-Circuit Parts List

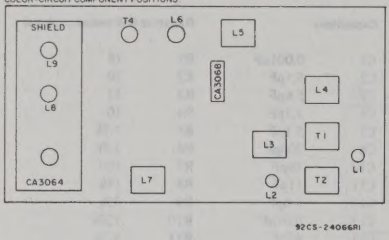
Capacitors	
C1	3.0pF
C2	3.0pF
C3	6.8pF
C4	3.9pF
C5	0.001μF
C6	12μF
C7	0.001μF
C8	0.001μF
C9	6.8pF
C10	0.01μF
C11	20pF
C12	15pF
C13	0.001μF
C14	18pF
C15	0.01μF
C16	0.001μF
C17	0.001μF
C18	5μF
C19	4700pF
C20	68pF
C21	12pF
C22	4pF
C23	82pF
C24	0.047μF
C25	0.047μF
C26	0.01μF
C27	0.047μF

Inductors	RCA Stock No.
L1	131655
L2	133463
L3	1.0μH
L4	12.0μH
L5	134754*
L6	131465
L7	133546
L8	130120
L9	130121

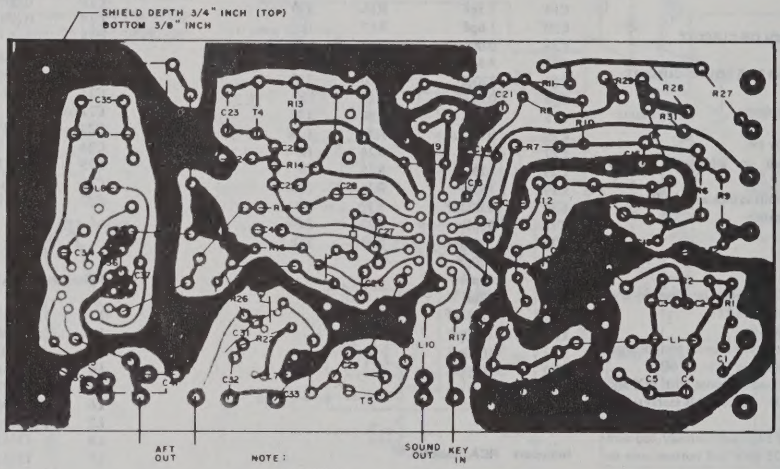
*(9 turns No. 23 wire; use 1/2 W resistor to form coil)

Resistors (All values in ohms)	
R1	18
R2	27
R3	91
R4	15k
R5	3.3k
R6	10k
R7	1.0k
R8	33k
R9	51k
R10	270
R11	2.2k
R12	120k
R13	2.2k
R14	15k
R15	25k
R16	8.2k
R17	2.2k
R18	3.3k
R19	150
R20	56
R21	36
R22	220
R23	5.6k

COLOR-CIRCUIT COMPONENT POSITIONS

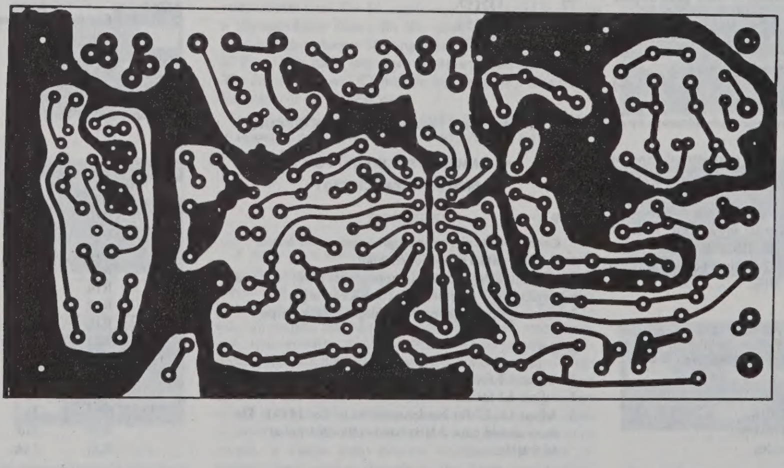


THE COLOR CIRCUIT

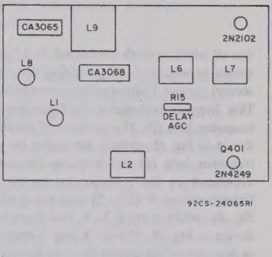


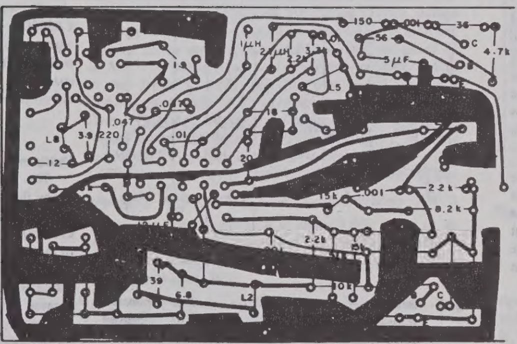
NOTE:
(1) +30 VOLTS
(2) TUNER AGC
(3) CONTROL AGC
(4) GND
(5) INPUT

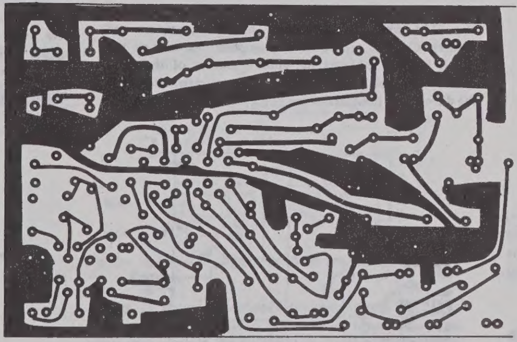
92CS-24077



THE MONOCHROME CIRCUIT







ICAN-6668

Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers

by H. A. Wittlinger

The CA3080 and CA3080A are similar in generic form to conventional operational amplifiers, but differ sufficiently to justify an explanation of their unique characteristics. This new class of operational amplifier not only includes the usual differential input terminals, but also contains an additional control terminal which enhances the device's flexibility for use in a broad spectrum of applications. The amplifier incorporated in these devices is referred to as an Operational Transconductance Amplifier (OTA), because its output signal is best described in terms of the output-current that it can supply. (Transconductance $g_m = \frac{\wedge i_{out}}{\wedge e_{in}}$). The amplifier's output-current is proportional to the voltage difference at its differential input terminals.

This Note describes the operation of the OTA and features various circuits using the OTA. For example, communications and industrial applications including modulators, multiplexers, sample-and-hold-circuits, gain control circuits and micropower comparators are shown and discussed. In addition, circuits have been included to show the operation of the OTA being used in conjunction with RCA COS/MOS devices as post-amplifiers.

Fig. 1 shows the equivalent circuit for the OTA. The output signal is a "current" which is proportional to the transconductance (gm) of the OTA established by the amplifier bias current (I_{ABC}) and the differential input voltage. The OTA can either source or sink current at the output terminals, depending on the polarity of the input signal.

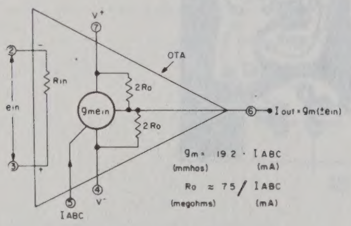


Fig. 1— Basic equivalent circuit of the OTA.

The availability of the amplifier bias current (I_{ABC}) terminal significantly increases the flexibility of the OTA and permits the circuit designer to exercise his creativity in the utilization of this device in many unique applications not possible with the conventional operational amplifier.

Circuit Description

A simplified block diagram of the OTA is shown in Fig. 2. Transistors Q1 and Q2 comprise the differential input amplifier found in most operational amplifiers, while the lettered-circles (with arrows leading either into or out of the circles) denote "current-mirrors". Fig. 3a shows the basic type of current-mirror which is comprised of two transistors,

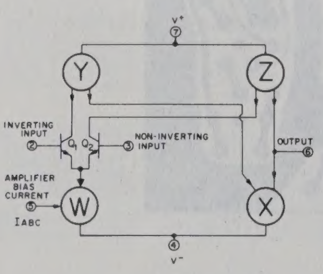


Fig. 2— Simplified diagram of OTA.

one of which is diode-connected. In a "current-mirror", with similar geometries for Q_A and Q_B, the current I' establishes a second current I whose value is essentially equal to that of I'. This basic current-mirror configuration is sensitive to the transistor beta (β). The addition of another active transistor, shown in Fig. 3b, greatly diminishes the circuit sensitivity to transistor beta (β) and increases the current-source output impedance in direct proportion to the transistor beta (β). Current-mirror W (Fig. 2) uses the configuration shown in Fig. 3a, while mirrors X, Y, and Z are basically the version shown in Fig. 3b. Mirrors Y and Z employ p-n-p transistors, as depicted by the arrows pointing outward from the mirrors. Appendix 1 describes "current-mirrors" in more detail.

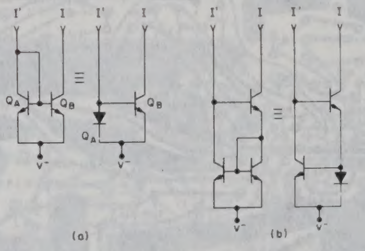


Fig. 3— Basic types of current mirrors; a) diode-connected transistor paired with transistor; b) improved version: employs an extra transistor.

Fig. 4 is the complete schematic diagram of the OTA. The OTA employs only active devices (transistors and diodes). Current applied to the amplifier-bias-current terminal, I_{ABC}, establishes the emitter current of the input differential amplifier Q1 and Q2. Hence, effective control of the differential transconductance (g_m) is achieved.

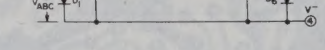


Fig. 4— Schematic diagram of OTA types CA3080 and CA3080A.

The g_m of a differential amplifier is equal to

$$\Big| \frac{q a I_C}{2KT}$$

(see Ref. 2 for derivation) where q is the charge on an electron, a is the ratio of collector current to emitter current of the differential amplifier transistors, (assumed to be 0.99 in this case), I_C is the collector current of the constant-current source (I_{ABC} in this case), K is Boltzman's constant, and T is the ambient temperature in degrees Kelvin. At room temperature, $g_m = 19.2 \times I_{ABC}$, where gm is in mmho and I_{ABC} is in milliamperes. The temperature coefficient of g_m is approximately -0.33%/°C (at room temperature).

Transistor Q3 and diode D1 (shown in Fig. 4) comprise the current mirror "W" of Fig. 2. Similarly, transistors Q7, Q8 and Q9 and diode D5 of Fig. 4 comprise the generic current mirror "Z" of Fig. 2. Darlington-connected transistors are employed in mirrors "Y" and "Z" to reduce the voltage sensitivity of the mirror, by the increase of the mirror output impedance. Transistors Q10, Q11, and diode D6 of Fig. 2 comprise the current-mirror "X" of Fig. 2. Diodes D2 and D4 are connected across the base-emitter junctions of Q5 and Q8, respectively, to improve the circuit speed. The amplifier output signal is derived from the collectors of the "Z" and "X" current-mirror of Fig. 2, providing a push-pull Class A output stage that produces full differential g_m. This circuit description applies to both the CA3080 and CA3080A. The CA3080A offers tighter control of g_m and input offset voltage, less variation of input offset voltage with variation of I_{ABC} and controlled cut-off leakage current. In the CA3080A, both the output and the input cut-off leakage resistances are greater than 1,000 MΩ.

APPLICATIONS

Multiplexing

The availability of the bias current terminal, I_{ABC}, allows the device to be gated for multiplex applications. Fig. 5 shows a simple two-channel multiplex system using two CA3080 OTA devices. The maximum level-shift from input to output is low (approximately 2mV for the CA3080A and 5mV for the CA3080). This shift is determined by the amplifier input offset voltage of the particular device used, because the open-loop gain of the system is typically 100dB when the loading on the output of the CA3080A is lqw. To further increase the gain and reduce the effects of loading, an additional buffer and/or gain-stage may be added. Methods will be shown to successfully perform these functions.

In this example positive and negative 5-V power-supplies were used, with the IC flip-flop powered by the positive supply. The negative supply-voltage may be increased to -15 V, with the positive-supply at 5 V to satisfy the logic supply voltage requirements. Outputs from the clocked flip-flop are applied through p-n-p transistors to gate the CA3080 amplifier-bias-current terminals. The grounded-base con-

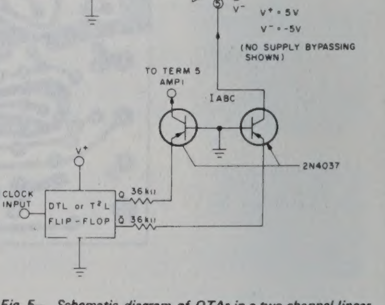


Fig. 5— Schematic diagram of OTAs in a two-channel linear time-shared multiplex circuit.

figuration is used to minimize capacitive feed-through coupling via the base-collector junction of the p-n-p transistor.

Another multiplex system using the OTA's clocked by a COS/MOS flip-flop is shown in Fig. 6. The high output voltage capability of the COS/MOS flip-flop permits the circuit to be driven directly without the need for p-n-p level-shifting transistors.

A simple RC phase-compensation network is used on the output of the OTA in the circuits shown in Figs. 5 & 6. The values of the RC-network are chosen so that $\frac{1}{2\pi RC} \cong 2\text{MHz}$.

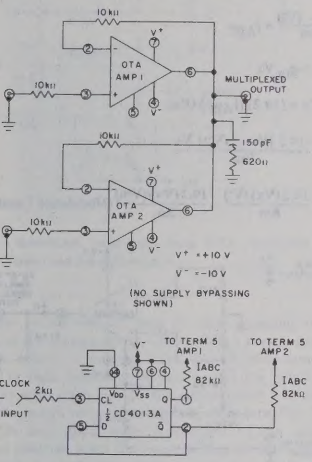
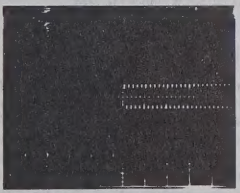


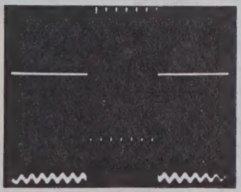
Fig. 6– Schematic diagram of a two-channel linear multiplex system using a COS/MOS flip-flop to gate two OTAs.

This RC-network is connected to the point shown because the lowest-frequency pole for the system is usually found at this point. Fig. 7 shows an oscilloscope photograph of the multiplex circuit functioning with two input signals. Fig. 8 shows an oscilloscope photograph of the output of the multiplexer with a 6-V p-p, sine wave signal (22 kHz) applied to one amplifier and the input to the other amplifier grounded. This photograph demonstrates an isolation of at least 80 dB between channels.



TOP TRACE: MULTIPLEXED OUTPUT 1V/DIV & 100μsec/DIV
BOTTOM TRACE: TIME EXPANSION OF SWITCHING BETWEEN INPUTS 2V/DIV & 5 μsec/DIV

Fig. 7– Voltage waveforms for circuit of Fig. 6; top trace: multiplexed output; lower trace: time expansion of switching between inputs.



TOP TRACE: 1V/DIV & 100μsec/DIV —OUTPUT
BOTTOM TRACE: VOLTAGE EXPANSION OF OUTPUT 1mV/DIV & 100μsec/DIV ISOLATION IS IN EXCESS OF 80 db

Fig. 8– Voltage waveforms for circuit of Fig. 6; top trace: output; lower trace: voltage expansion of output; isolation in excess of 80 dB.

Sample-and-Hold Circuits

An extension of the multiplex system application is a sample-and-hold circuit (Fig. 9), using the strobing characteristics of the OTA amplifier bias-current (ABC) terminal as a means of control. Fig. 9 shows the basic system using the CA3080A as an OTA in a simple voltage-follower configuration with the phase-compensation capacitor serving the additional function of sampled-signal storage. The major consideration for the use of this method to "hold" charge is that neither the charging amplifier nor the signal readout device significantly alter the charge stored on the capacitor. The CA3080A is a particularly suitable capacitor-charging amplifier because its output resistance is more than 1000 MΩ under cut-off conditions, and the loading on the storage capacitor during the hold-mode is minimized. An effective solution to the read-out requirement involves the use of an RCA 3N138 insulated-gate field-effect transistor (MOS/FET) in the feedback loop. This transistor has a maximum gate-leakage current of 10 picoamperes; its loading on the charge "holding" capacitor is negligible. The open-loop voltage-gain of the system (Fig. 9) is approximately 100 dB if the MOS/FET is used in the source-follower mode to the CA3080A as the input amplifier. The open-loop output impedance $(\frac{1}{g_m})$ of the 3N138 is approximately 220 Ω because its transconductance is about 4,600 μmho at an operating current of 5 mA. When the CA3080A drives the 3N138 (Fig. 9), the closed loop operational-amplifier output impedance characteristic

$$Z_{out} \cong \frac{Z_o\text{ (open-loop)}}{A\text{ (open-loop voltage-gain)}}$$

$$\cong \frac{220\ \Omega}{100\text{dB}} \cong \frac{220\ \Omega}{10^5} \cong 0.0022\ \Omega$$

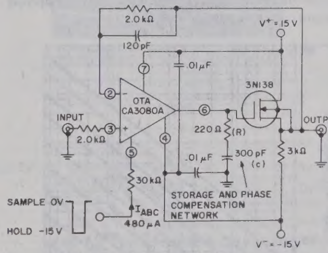
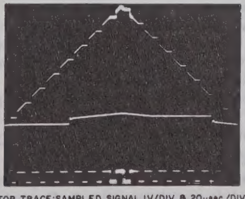


Fig. 9– Schematic diagram of OTA in a sample-and-hold circuit.

Fig. 10 shows a "sampled" triangular signal. The lower trace in the photograph is the sampling signal. When this signal goes negative, the CA3080A is cutoff and the signal is "held" on the storage capacitor, as shown by the plateaus on the triangular wave-form. The center trace is a time expansion of the top-most transition (in the upper trace) with a time scale of 2 μsec/div.



TOP TRACE: SAMPLED SIGNAL 1V/DIV & 20μsec/DIV
CENTER TRACE: TOP PORTION OF UPPER SIGNAL 1V/DIV & 2μsec/DIV
BOTTOM TRACE: SAMPLING SIGNAL 20V/DIV & 20μsec/DIV

Fig. 10– Waveforms for circuit of Fig. 9; top trace: sampled signal; center trace: top portion of upper signal; lower trace: sampling signal.

Once the signal is acquired, variation in the stored-signal level during the hold-period is of concern. This variation is primarily a function of the cutoff leakage current of the CA3080A (a maximum limit of 5 ηA), the leakage of the storage element, and other extraneous paths. These leakage currents may be either "positive" or "negative" and, consequently, the stored-signal may rise or fall during the "hold" interval. The term "tilt" is used to describe this condition. Fig. 11 shows the expected pulse "tilt" in microvolts as a function of time for various values of the compensation/storage capacitor. The horizontal axis shows three scales representing leakage currents of 50 ηA, 5 ηA, 500 pA.

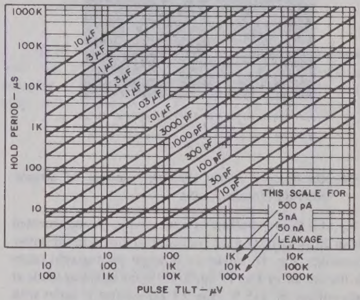
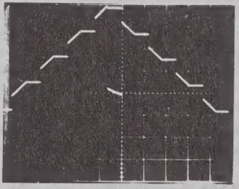


Fig. 11– Chart showing "tilt" in sample-and-hold potentials as a function of hold time with load capacitance as a parameter.

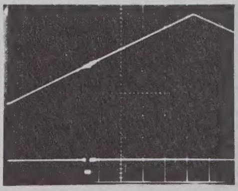
Fig. 12 shows a dual-trace photograph of a triangular signal being "sampled-and-held" for approximately 14 ms with a 300 pF storage capacitor. The center trace (expanded to 20 mV/div) shows the worst-case "tilt" for all the steps shown in the upper trace. The total equivalent leakage current in this case is only 170 pA $(I = C\frac{dv}{dt})$.



TOP TRACE SAMPLED SIGNAL 1V/DIV & 20msec/DIV
CENTER TRACE WORSE CASE TILT 20mV/DIV & 20msec/DIV

Fig. 12– Oscilloscope photo of "triangular-voltage" being sampled by circuit of Fig. 9.

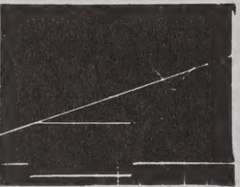
Fig. 13 is an oscilloscope photograph of a ramp voltage being sampled by the "sample-and-hold" circuit of Fig. 9. The input signal and sampled-output signal are superimposed. The lower trace shows the sampling signal. Data shown in Fig. 13 were recorded with supply voltages of ±10 V and the series input resistor at terminal 5 was 22 kΩ.



TOP TRACE INPUT AND OUTPUT SUPERIMPOSED 1V/DIV & 2μsec/DIV
BOTTOM TRACE SAMPLING SIGNAL 20V/DIV & 2μsec/DIV

Fig. 13– Oscilloscope photo of "ramp-voltage" being sampled by circuit of Fig. 9.

In Fig. 14, the trace of Fig. 13 has been expanded (100 mV/div and 100 ηsec/div) to show the response of the sample-and-hold circuit with respect to the sampling signal. After the sampling interval, the amplifier overshoots the signal level and settles (within the amplifier offset voltage) in approximately 1 µs. The resistor in series with the 300 pF phase-compensation capacitor was adjusted to 68 ohms for minimum recovery time.



TOP TRACE INPUT AND SAMPLED OUTPUT SUPER-IMPOSED 100mV/DIV & 100ns/DIV
BOTTOM TRACE SAMPLING SIGNAL 20V/DIV & 100 ns/DIV

Fig. 14– Oscilloscope photo showing response of sample-and-hold circuit (Fig. 9).

Fig. 15 shows the basic circuit of Fig. 9 implemented with an RCA 2N4037 p-n-p transistor to minimize capacitive feedthrough. Fig. 16 shows oscilloscope photographs taken with the circuit of Fig. 15 operating in the sampling mode at supply-voltage of ±15 V. The 9.1 kΩ resistor in series with the p-n-p transistor emitter establishes amplifier-bias-current (I_{ABC}) conditions similar to those used in the circuit of Fig. 9.

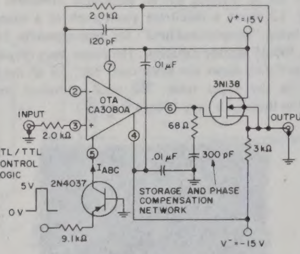
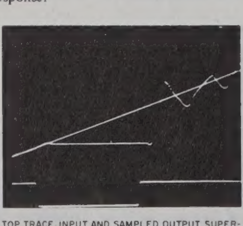


Fig. 15– Schematic diagram of the OTA in a sample-and-hold configuration (DTL/TTL control logic).

Considerations of circuit stability and signal retention require the use of the largest possible phase-compensation capacitor, compatible with the required slew rate. In most systems the capacitor is chosen for the maximum allowable "tilt" in the storage mode and the resistor is chosen so that $\frac{1}{2\pi RC} \cong 2\text{MHz}$, corresponding to the first pole in the amplifier at an output current level of 500 µA. It is frequently desirable to optimize the system response by the placement of a small variable resistor in series with the capacitor, as is shown in Figs. 9 and 15. The 120 pF capacitor shunting the 2 kΩ resistor improves the amplifier transient response.

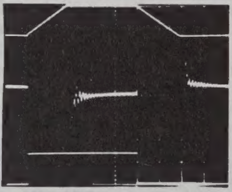


TOP TRACE INPUT AND SAMPLED OUTPUT SUPER-IMPOSED 100 mV/DIV & 100 ns DIV
BOTTOM TRACE SAMPLING SIGNAL 5 V/DIV & 100 ns/DIV

Fig. 16– Oscilloscope photo for circuit of Fig. 15 operating in sampling mode.

Fig. 17 shows a multi-trace oscilloscope photograph of input and output signals for the circuit of Fig. 9, operating in the linear mode. The lower portion of the photograph shows the input signal, and the upper portion shows the output signal. The amplifier slew-rate is determined by the output current and the capacitive loading: in this case the slew rate (dV/dt) = 1.8V/µs.

The center trace in Fig. 17 shows the difference between the input and output signals as displayed on a Tektronix 7A13 differential amplifier at 2 mV/div. The output of the amplifier system settles to within 2 mV (the offset voltage specification for the CA3080A) of the input level in 1 µs after slewing.



TOP TRACE: OUTPUT 5V/DIV & 2µsec/DIV
CENTER TRACE: DIFFERENTIAL COMPARSION OF INPUT AND OUTPUT 2mV/DIV– 0 VOLTS THROUGH CENTER– 2 µsec/DIV
BOTTOM TRACE: INPUT 5V/DIV & 2µsec/DIV

Fig. 17– Oscilloscope photo showing circuit of Fig. 9 operating in the linear sample-mode.

Fig. 18 is a curve of slew-rate as a function of amplifier-bias-current (I_{ABC}) with various storage/compensation capacitors. The magnitude of the current being supplied to the storage/compensation capacitor is equal to the amplifier-bias-current (I_{ABC}) when the OTA is supplying its maximum output current.

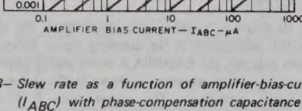


Fig. 18– Slew rate as a function of amplifier-bias-current (I_{ABC}) with phase-compensation capacitance as a parameter.

Gain Control – Amplitude Modulation

Effective gain control of a signal may be obtained by controlled variation of the amplifier-bias-current (I_{ABC}) in the OTA because its g_m is directly proportional to the amplifier-bias-current (I_{ABC}). For a specified value of amplifier-bias-current, the output current (I_O) is equal to the product of g_m and the input signal magnitude. The output voltage swing is the product of output current (I_O) and the load resistance (R_L).

Fig. 19 shows the configuration for this form of basic gain control (a modulation system). The output signal current (I_O) is equal to $-g_m V_x$; the sign of the output signal is negative because the input signal is applied to the inverting input terminal of the OTA. The transconductance of the OTA is controlled by adjustment of the amplifier bias current, I_{ABC}. In this circuit the level of the unmodulated carrier output is established by a particular amplifier-bias-current (I_{ABC}) through resistor Rm. Amplitude modulation of the carrier frequency occurs because variation of the voltage Vm forces a change in the amplifier-bias-current (I_{ABC}) supplied via resistor Rm. When Vm goes positive the bias current increases which causes a corresponding increase in the g_m of the OTA. When the Vm goes in the negative direction (toward the amplifier-bias-current terminal potential), the amplifier-bias-current decreases, and reduces the g_m of the OTA.

As discussed earlier, $g_m = 19.2 \times I_{ABC}$, where g_m is in millimhos when I_{ABC} is in milliamperes. In this case, I_{ABC} is approximately equal to:

$$\frac{Vm - (V^-)}{Rm} = I_{ABC}$$

$$(I_O) = -g_m\, Vx$$

$$g_m\, Vx = (19.2)(I_{ABC})(Vx)$$

$$I_O = \frac{-19.2\,[Vm - (V^-)]\,Vx}{Rm}$$

$$I_O = \frac{19.2\,(Vx)(V^-)}{Rm} - \frac{19.2\,(Vx)(Vm)}{Rm}\ \text{(Modulation Equation).}$$

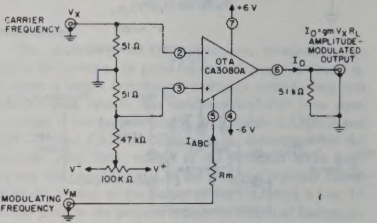


Fig. 19– Amplitude modulator circuit using the OTA.

There are two terms in the modulation equation: the first term represents the fixed carrier input, independent of Vm, and the second term represents the modulation, which either adds to or subtracts from the first term. When Vm is equal to the V- term, the output is reduced to zero.

In the preceding modulation equations the term

$$(19.2)(Vx)\ \frac{V_{ABC}}{Rm}$$

involving the amplifier-bias-current terminal voltage (V_{ABC}) (see Fig. 4 for V_{ABC}) was neglected. This term was assumed to be small because V_{ABC} is small compared with V- in the equation. If the amplifier-bias-current terminal is driven by a current-source (such as from the collector of a p-n-p transistor), the effect of V_{ABC} variation is eliminated and transferred to the involvement of the p-n-p transistor base-emitter junction characteristics. Fig. 20 shows a method of driving the amplifier-bias-current terminal to effectively remove this latter variation. If an n-p-n transistor is added to

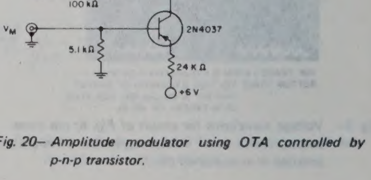


Fig. 20– Amplitude modulator using OTA controlled by p-n-p transistor.

the circuit of Fig. 20 as an emitter-follower to drive the p-n-p transistor, variations due to base-emitter characteristics are considerably reduced due to the complementary nature of the n-p-n base-emitter junctions. Moreover, the temperature coefficients of the two base-emitter junctions tend to cancel one another. Fig. 21 shows a configuration using one transistor in the RCA type CA3018A n-p-n transistor-array as an input emitter-follower, with the three remaining transistors of the transistor-array connected as a current-source for the emitter – followers. The 100-kΩ potentiometer shown in these schematics is used to null the effects of amplifier input offset voltage. This potentiometer is adjusted to set the output voltage symmetrically about zero. Figs. 22a and 22b show oscilloscope photographs of the output voltages obtained when the circuit of Fig. 19 is used as a modulator for both sinusoidal and triangular modulating signals. This method of modulation permits a range exceeding 1000:1 in the gain, and thus provides modulation of the carrier input in excess of 99%. The photo in Fig. 22c shows the excellent isolation achieved in this modulator during the "gated-off" condition.

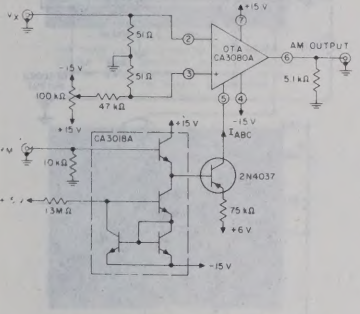


Fig. 21– Amplitude modulator using OTA controlled by p-n-p and n-p-n transistors.

Four-Quadrant Multipliers

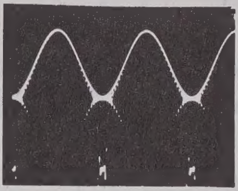
A single CA3080A is especially suited for many low-frequency, low-power four-quadrant multiplier applications. The basic multiplier circuit of Fig. 23 is particularly useful for waveform generation, doubly balanced modulation, and other signal processing applications, in portable equipment, where low-power consumption is essential and accuracy requirements are moderate. The multiplier configuration is basically an extension of the previously discussed gain-controlled configuration (Fig. 19).

To obtain a four-quadrant multiplier, the first term of the modulation equation (which represents the fixed carrier) must be reduced to zero. This term is reduced to zero by the placement of a feedback resistor (R) between the output and the inverting input terminal of the CA3080A, with the value of the feedback resistor (R) equal to $1/g_m$. The output current is $I_O = g_m\,(\text{-}Vx)$ because the input is applied to the inverting terminal of the OTA. The output current due to the resistor (R) is $\frac{Vx}{R}$. Hence, the two signals cancel when $R = 1/g_m$. The current for this configuration is:

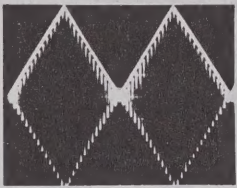
$$I_O = \frac{-19.2\ Vx\ Vm,}{Rm} \quad \text{and } Vm = Vy$$

The output signal for these configurations is a "current" which is best terminated by a short-circuit. This condition can be satisfied by making the load resistance for the multiplier output very small. Alternatively, the output can be applied to a current-to-voltage converter shown in Fig. 24.

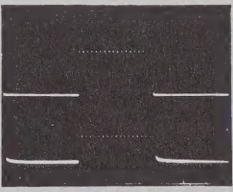
In Fig. 23, the current "cancellation" in the resistor R is a direct function of the OTA differential amplifier linearity. In the following example, the signal excursion is limited to ±10 mV to preserve this linearity. Greater signal-excursions on the input terminal will result in a significant departure from linear operation (which may be entirely satisfactory in many applications).



TOP TRACE: MODULATION FREQUENCY INPUT ≈ 20 VOLTS P-P & 50μsec/DIV
CENTER TRACE AMPLITUDE MODULATE OUTPUT 500mV/DIV & 50μsec/DIV
BOTTOM TRACE EXPANDED OUTPUT TO SHOW DEPTH OF MODULATION 20mV/DIV & 50μsec/DIV



TOP TRACE: MODULATION FREQUENCY INPUT 20 VOLTS & 50μsec/DIV
BOTTOM TRACE AMPLITUDE MODULATED OUTPUT 500mV/DIV & 50μsec/DIV



TOP TRACE GATED OUTPUT 1V/DIV AND 50μsec/DIV
BOTTOM TRACE VOLTAGE EXPANSION OF ABOVE SIGNAL–SHOWING NO RESIDUAL 1mV/DIV AND 50μsec/DIV– AT LEAST 80 db OF ISOLATION fq = 100 kHz

Fig. 22– a) Oscilloscope photo of amplitude modulator circuit of Fig. 15 with $R_m = 40\,k\Omega$, $V^+ = 10$ v and V- = -10 V. Top trace: modulation frequency input ≃ 20-V p-p; center trace: amplitude modulated output 500-mV/div.; lower trace: expanded output to show depth of modulation, 20 mV/div.; b) triangular modulation; top trace: modulation frequency input ≃ 20 V; lower trace: amplitude modulated output 500 mV/div.; c) square wave modulation, top trace: gated output 1 V/div.; lower trace: expanded scale, showing no residual (1 mV/div) and at least 80 dB of isolation at fq = 100 kHz.

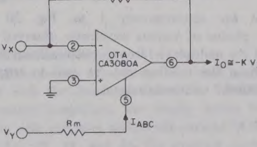


Fig. 23– Basic four quadrant analog multiplier using an OTA.

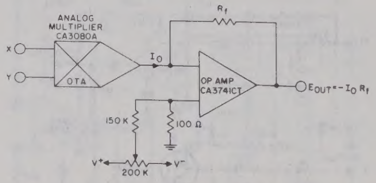


Fig. 24– OTA analog multiplier driving an op-amp that operates as a current-to-voltage converter.

Fig. 25 shows a schematic diagram of the basic multiplier with the adjustments set-up to give the multiplier an accuracy of approximately ±7 percent "full-scale". There are only three adjustments: 1) one is on the output, to compensate for slight variations in the current-transfer ratio of the current-mirrors (which would otherwise result in a symmetrical output about some current level other than zero); 2) the adjustment of the 20-kΩ potentiometer establishes the g_m of the system equal to the value of the fixed resistor shunting the system when the Y-input is zero; 3) compensates for error due to input offset voltage.

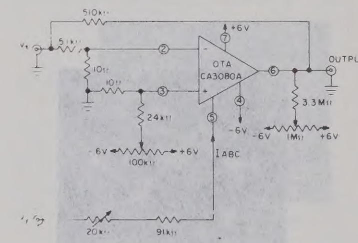


Fig. 25– Schematic diagram of analog multiplier using OTA.

Procedure for adjustment of the circuit:

1. a) Set the 1 MΩ output-current balancing potentiometer to the center of its range
   b) Ground the X- and Y- inputs
   c) Adjust the 100 kΩ potentiometer until a zero-V reading is obtained at the output.
2. a) Ground the Y-input and apply a signal to the X-input through a low source-impedance generator. (It is essential that a low impedance source be used; this minimizes any change in the g_m balance or zero-point due to the 50-μA Y-input bias current).
   b) Adjust the 20-kΩ potentiometer in series with Y-input until a reading of zero-V is obtained at the output. This adjustment establishes the g_m of the CA3080A at the proper level to cancel the output signal. The output current is diverted through the 510-kΩ resistor.
3. a) Ground the X-input and apply a signal to the Y-input through a low source-impedance generator.
   b) Adjust the 1-MΩ resistor for an output voltage of zero-V.

There will be some interaction among the adjustments and the procedure should be repeated to optimize the circuit performance.

Fig. 26 shows the schematic of an analog multiplier circuit with a 2N4037 p-n-p transistor replacing the Y-input "current" resistor. The advantage of this system is the higher input resistance resulting from the current-gain of the p-n-p transistor. The addition of another emitter-follower preceding the p-n-p transistor (shown in Fig. 21) will further increase the current gain while markedly reducing the effect of the V_{be} temperature-dependent characteristic and the offset voltage of the two base-emitter junctions.

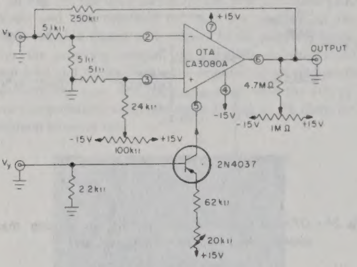
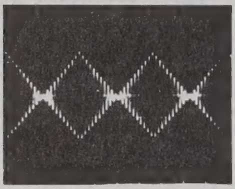
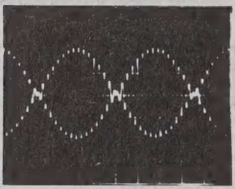


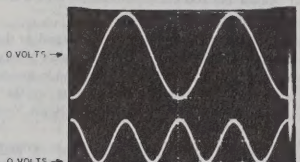
Fig. 26– Schematic diagram of analog multiplier using OTA controlled by a p-n-p transistor.



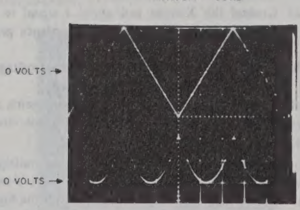
500 mV/DIV AND 200 µsec/DIV
TRIANGLAR INPUT 700 Hz TO V_Y INPUT 5 VPP
CARRIER INPUT 30 kHz TO V_X INPUT 13.5 VPP



500 mV/DIV AND 200 µsec/DIV
MODULATING FREQUENCY 700 Hz TO V_Y INPUT 5 VPP
CARRIER INPUT 21 kHz TO V_X INPUT 13.5 VPP



TOP TRACE INPUT TO X AND Y 2 V/DIV AND
1 msec/DIV – 200 Hz
BOTTOM TRACE: OUTPUT 500 mV/DIV AND
1 msec/DIV – 400 Hz



SAME SCALE AS 27C

Fig. 27– a) Waveforms observed with OTA analog multiplier used as a suppressed carrier generator; b) waveforms observed with OTA analog multiplier used in signal-squaring circuits.

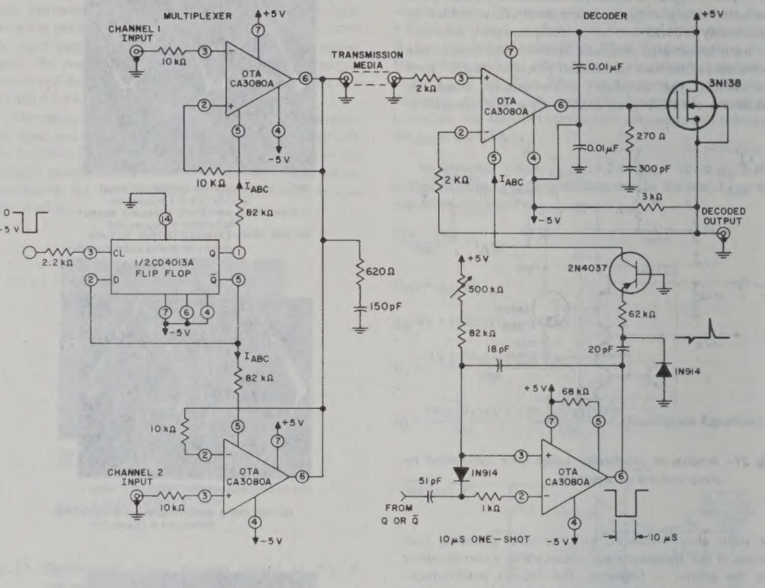


Fig. 28– Two-channel multiplexer and decoder using OTAs.

Figs. 27a and 27b show oscilloscope photographs of the output signals delivered by the circuit of Fig. 26 which is connected as a suppressed-carrier generator. Figs. 27c and 27d contain photos of the outputs obtained in signal "squaring" circuits, i.e. "squaring" sine-wave and triangular-wave inputs.

If ±15-V power supplies are used (shown in Fig. 26), both inputs can accept ±10-V input signals. Adjustment of this multiplier circuit is similar to that already described above.

The accuracy and stability of these multipliers are a direct function of the power supply-voltage stability because the Y-input is referred to the negative supply-voltage. Tracking of the positive and negative supply is also important because the balance adjustments for both the offset voltage and output current are also referenced to these supplies.

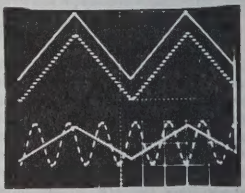
Other forms of four-quadrant multipliers using operational transconductance amplifiers have been published. (See Ref. 2.) the circuit shown in Ref. 2 tends to reduce the effects of the previously discussed g_m temperature dependency.

Linear Multiplexer – Decoder

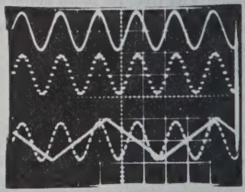
A simple, but effective system for multiplexing and decoding can be assembled with the CA3080 shown in Fig. 28. Only two channels are shown in this schematic, but the number of channels may be extended as desired. Fig. 29 shows oscilloscope photos taken during operation of the multiplexer and decoder. A CA3080 is used as a 10 µsec delay- "one-shot" multivibrator in the decoder to insure that the sample-and-hold circuit can sample only after the input signal has settled. Thus, the trailing edge of the "one-shot" output-signal is used to sample the input at the sample-and-hold circuit for approximately 1 µs. Fig. 30 shows oscilloscope photos of various waveforms observed during operation of the multiplexer/decoder circuit. Either the Q or $\overline{Q}$ output from the flip-flop may be used to trigger the 10 µsec "one-shot" to decode a signal.

High-Gain, High-Current Output Stages

In the previously discussed examples, the OTA has been buffered by a single insulated-gate field-effect-transistor (MOS/FET) shown in Fig. 9. This configuration yields a voltage gain equal to the (g_m) (R_o) product of the CA3080, which is typically 142,000 (103dB). The output voltage and current-swing of the operational amplifier formed by this configuration (Fig. 9) are limited by the 3N138 MOS/FET performance and its source-terminal load. In the positive direction, the MOS/FET may be driven into saturation; the source-load resistance and the MOS/FET characteristics become the factors limiting the output-voltage swing in the negative direction. The available negative-going load current may be kept constant by the return of the source-terminal to

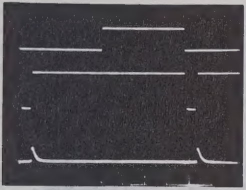


20 msec/DIV
TOP TRACE INPUT SIGNAL (1 VOLT/DIV)
CENTER TRACE RECOVERED OUTPUT (1 VOLT/DIV)
BOTTOM TRACE MULTIPLEXED SIGNALS (2 VOLTS/DIV)

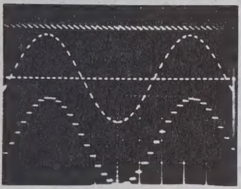


20 msec/DIV
TOP TRACE INPUT SIGNAL (1 VOLT/DIV)
CENTER TRACE RECOVERED OUTPUT (1 VOLT/DIV)
BOTTOM TRACE MULTIPLEXED SIGNALS (1 VOLT/DIV)

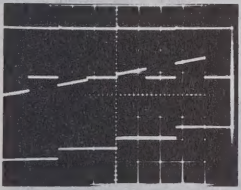
Fig. 29– Waveforms showing operation of linear multiplexer/sample-and-hold decode circuitry (Fig. 28).



20 µsec/DIV
TOP TRACE FLIP-FLOP OUTPUT (5 VOLTS/DIV)
CENTER TRACE "ONE-SHOT" OUTPUT (5 VOLTS/DIV)
BOTTOM TRACE PULSE AT THE COLLECTOR OF THE 2N4037 TRANSISTOR (0.1 VOLTS/DIV)



TOP TRACE COLLECTOR OF PNP TRANSISTOR (0.5 V/DIV)
CENTER TRACE MULTIPLEXED OUTPUT WITH ONE CHANNEL INPUT GROUND (0.5V/DIV)
LOWER TRACE DECODED OUTPUT (0.5V/DIV)
TIME ALL SCALES 5 msec/DIV



TIME EXPANSION TO 500µsec/DIV

Fig. 30– (a) Waveforms showing timing of flip-flop, delay–"one-shot" and the strobing pulse to the sample-and-hold circuit (Fig. 28): top trace: flip-flop output (5 V/div); center trace: "one-shot" output (5 V/div); lower trace: pulse at collector of 2N4037 transistor (0.1 V/div); b) Waveforms showing the decoding operation from the decoder keying pulse (top traces) to the recovered "decoded" sampled output (lower traces). 1) top trace: collector of 2N4037; center trace: multiplexed output with one channel input grounded; lower trace: decoded output; 2) Expanded scale of (1).

a constant-current transistor. Phase compensation is applied at the interface of the CA3080 and the 3N138 MOS/FET shown in Fig. 9.

Another variation of this generic form of amplifier utilizes the RCA CD4007A (COS/MOS) "inverter" as an amplifier driven by the CA3080. Each of the three "inverter"/amplifiers in the CD4007A has a typical voltage gain of 30 dB. The gain of a single COS/MOS "inverter"/amplifier coupled with the 100 dB gain of the CA3080 yields a total forward-gain of about 130 dB. Use of a two-stage COS/MOS amplifier configuration will increase the total open-loop gain of the system to about 160 dB (100,000,000). Figs. 31 through 34 show examples of these configurations. Each COS/MOS "inverter"/amplifier can sink or source a current of 6 mA (typ.). In Figs. 33 and 34, two COS/MOS "inverter"/amplifiers have been connected in parallel to provide additional output current.

The open-loop slew-rate of the circuit in Fig. 31 is approximately 65 V/µsec. When compensated for the unity-gain voltage-follower mode, the slew-rate is about 1 V/µsec (shown in Fig. 32). Even when the three "inverter"/amplifiers in the CD4007A are connected as shown in Fig. 33, the open-loop slew-rate remains at 65 V/µsec. A slew-rate of about 1 V/µsec is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 34. Fig. 35 contains oscilloscope photos of input-output waveforms under small-signal and large-signal conditions for the circuits of Figs. 32 and 34. These photos illustrate the inherent stability of the OTA and COS/MOS circuits operating in concert.

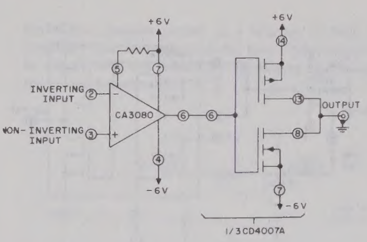


Fig. 31– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (open-loop mode). For greater current output the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown. Open-loop gain ≃ 130 dB.

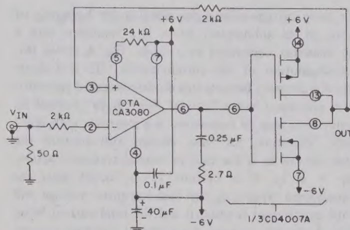


Fig. 32– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (unity-gain closed-loop mode). For greater current output, the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown.

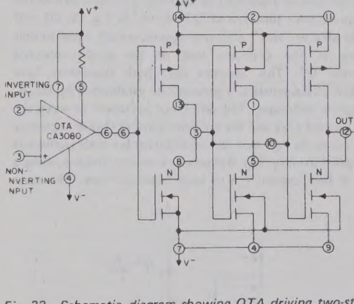


Fig. 33– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (open-loop mode). gain ≃ 160 dB.

Precision Multistable Circuits

The micropower capabilities of the CA3080, when combined with the characteristics of the CD4007A COS/MOS "inverter"/amplifiers, are ideally suited for use in connection with precision multistable circuits. In the circuits of Figs. 31, 32, 33, and 34, for example, power-supply current drawn by the COS/MOS "inverter"/amplifier approaches zero as the output voltage swings either positive or negative, while the CA3080 current-drain remains constant.

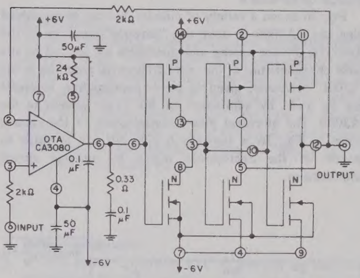
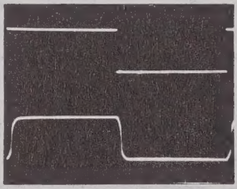


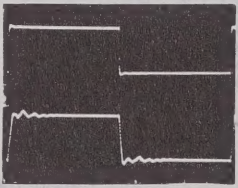
Fig. 34– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (unity gain closed-loop mode).

(a)



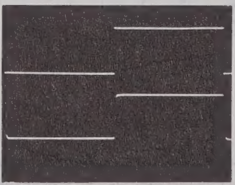
TOP TRACE INPUT 5V/DIV -100µsec/DIV
BOTTOM TRACE OUTPUT SAME SCALE

(b)



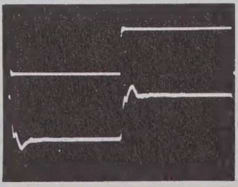
TOP TRACE INPUT-50mV/DIV-1µsec/DIV
BOTTOM TRACE OUTPUT-SAME SCALE

(c)



TOP TRACE INPUT-5V/DIV-100µsec/DIV
BOTTOM TRACE OUTPUT-SAME SCALE

(d)



TOP TRACE INPUT-50mV/DIV-1µsec/DIV
BOTTOM TRACE OUTPUT-SAME SCALE

Fig. 35– a) Waveforms for circuit of Fig. 32 with large signal input; b) Waveforms for circuit of Fig. 32 with small signal input; c) Waveforms for circuit of Fig. 34 with large signal input; d) Waveforms for circuit of Fig. 34 with small signal input.

Fig. 36 shows a variety of circuits that can be assembled using the CA3080 to drive one "inverter"/amplifier in the CD4007A. Precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080. Moreover, speed vs. power consumption tradeoffs may be made by adjustment of the I_{ABC} current to the CA3080. The quiescent power consumption of the circuits shown in Fig. 36 is typically 6 mW, but can be made to operate in the micropower region by suitable circuit modifications.

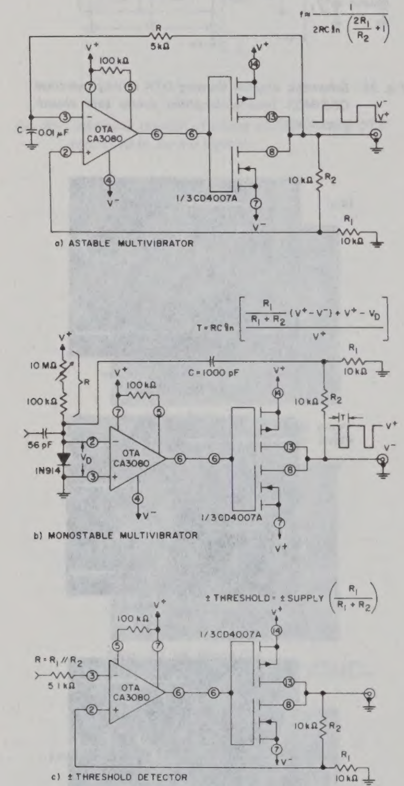

$f \approx \frac{1}{2RC \ln \left(\frac{2R_1}{R_2}+1\right)}$
R
5kΩ
V+
100kΩ
OTA
CA3080
C
0.01µF
1/3CD4007A
10kΩ
R2
R1
a) ASTABLE MULTIVIBRATOR
$T = RC \ln \left[\frac{\frac{R_1}{R_1+R_2}(V^+-V^-)+V^+-V_D}{V^+}\right]$
10MΩ
100kΩ
C=1000pF
56pF
IN914
VD
b) MONOSTABLE MULTIVIBRATOR
$\pm \text{THRESHOLD} = \pm \text{SUPPLY} \left(\frac{R_1}{R_1+R_2}\right)$
R=R1//R2
5.1kΩ
c) ± THRESHOLD DETECTOR

Fig. 36– Multistable circuits using the OTA and COS/MOS Inverter/Amplifiers: a) astable multivibrator; b) monostable multivibrator; c) threshold detector (plus or minus). For greater current output, the remaining amplifiers in the CD4007A may be connected in parallel with the single stage shown.

Micropower Comparator

The schematic diagram of a micropower comparator is shown in Fig. 37. Quiescent power consumption of this circuit is about 10 µW (typ). When the comparator is strobed "ON", the CA3080A becomes active and consumes 420 µW. Under these conditions, the circuit responds to a differential input signal in about 8 µsec. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 nsec., but the power consumption rises to 21 mW.

The differential amplifier input common-mode range for the circuit of Fig. 37 is -1V to +10.5 V. Voltage of the micropower comparator is typically 130 dB. For example, a 5 µV input signal will toggle the output.

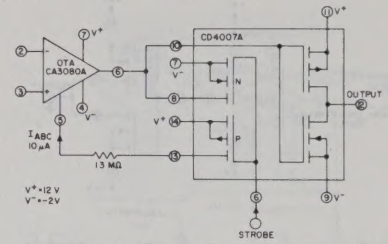


Fig. 37– Schematic diagram of micropower comparator using the CA3080A and COS/MOS CD4007A.

APPENDIX I
CURRENT MIRRORS

The basic current-mirror, described in the beginning of this note, in its rudimentary form, is a transistor with a second transistor connected as a diode. Fig. A shows this basic configuration of the current-mirror. Q2 is a diode connected transistor. Because this diode-connected transistor is not in saturation and is "active", the "diode" formed by this connection may be considered as a transistor with 100% feedback. Therefore, the base current still controls the collector current as is the case in normal transistor action, i.e., $I_C = \beta\ I_b$. If a current I_1 is forced into the diode-connected transistor, the base-to-emitter voltage will rise until equilibrium is reached and the total current being supplied is divided between the collector and base regions. Thus, a base-to-emitter voltage is established in Q2 such that Q2 "sinks" the applied current I_1.

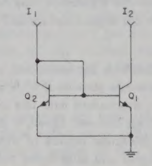


Fig. A– Diode – transistor current source.

If the base of a second transistor (Q1) is connected to the base-to-collector junction of Q2, shown in Fig. A, Q1 will also be able to "sink" a current approximately equal to that flowing in the collector lead of the diode-connected transistor Q2. This assumes that both transistors have identical characteristics, a prerequisite established by the IC fabrication technique. The difference in current between the input current (I_1) and the collector current (I_2) of transistor Q, is due to the fact that the base-current for both transistors is supplied from I_1. Fig. B shows this current division, using a unit of base current (1) to each transistor base. This base current causes a collector current to flow in direct proportion to the β of each transistor. The ratio of the "sinking" current I_2 to the input current I_1 is therefore equal to $\frac{I_2}{I_1} = \beta/(\beta+2)$. Thus, as β increases, the output "sinking" current (I_2) level approaches that of the input current (I_1). The curves in Fig. C show this ratio as a function of the transistor β. When the transistor β is equal to 100, for example, the difference between the two currents is only two percent.

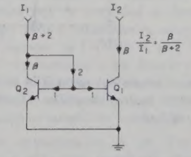


Fig. B– Diode – transistor current source. Analysis of current flow.

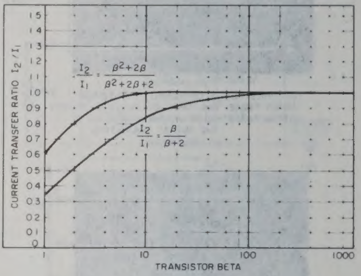


Fig. C– Current transfer ratio I_2/I_1 as a function of transistor beta.

Fig. D shows a curve-tracer photograph of characteristics for the circuit of Figs. A and B. No consideration in this discussion is given to the variation of the transistor (Q1) collector current as a function of its collector-to-emitter voltage. The output resistance characteristic of Q1 retains its similarity to that of a single transistor operating under similar conditions. An improvement in its output resistance characteristic can be made by the insertion of a diode-connected transistor in series with the emitter of Q1.

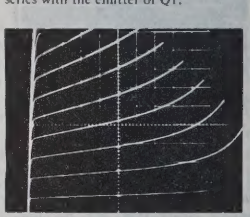


Fig. D– Photo showing results of Figs. A & B.

This diode-connected transistor (Q3 in Fig. E) may be considered as a current-sampling diode that senses the emitter-current of Q1 and adjusts the base current Q1 (via Q2) to maintain a constant-current in I_2. Because all controlling transistors are operated at relatively fixed voltages, the previously discussed effects due to voltage coefficients do not exist. The curve-tracer photograph of Fig. F shows the improved output resistance characteristics of the circuit of Fig. E. (Compare Fig. D and F).

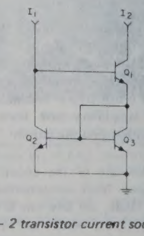


Fig. E– Diode – 2 transistor current source.

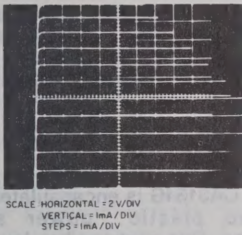
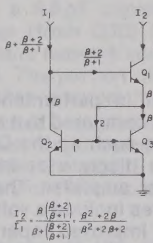


Fig. F– Photo showing results of Fig. E.

Fig. G shows the current-division within the "mirror" assuming a "unit" (1) of current in transistors (Q2 and Q3).

The resulting current-transfer ratio $I_2/I_1 = \dfrac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$: Fig. C shows this equation plotted as a function of beta. It is significant that the current transfer ratio (I_2/I_1) is improved by the β^2 term, and reduces the significance of the $2\beta + 2$ term in the denominator.



$$\frac{I_2}{I_1} = \frac{\beta\left(\frac{\beta+2}{\beta+1}\right)}{\beta + \left(\frac{\beta+2}{\beta+1}\right)} = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$$

Fig. G– Current flow analysis of Fig. E.

Conclusions

The Operational Transconductance Amplifier (OTA) is a unique device with characteristics particularly suited to applications in multiplexing, amplitude modulation, analog multiplications, gain control, switching circuitry, multivibrators, comparators, and a broad spectrum of micropower circuitry. The CA3080 is ideal for use in conjunction with COS/MOS (Complementary-Symmetry MOS) IC's being operated in the linear mode.

Acknowledgements

The author is indebted to C. F. Wheatly for many helpful discussions. Valued contributions in circuit evaluation were made by A. J. Visioli Jr. and J. H. Klinger.

References

1 RCA's Linear Integrated Circuits Manual, Basic Circuits Section.
2 RCA published data for CA3060 File No. 404

ICAN-6728

Application of the CA3134G Sound IF and Output Subsystem in Television Receivers

by George M. Harayda

In the CA3134, the sound if and audio output subsystems for color or black-and-white television receivers are combined in a single monolithic integrated circuit.[1] As shown in the block diagram, Fig. 1, the CA3134 includes a multistage if amplifier-limiter, an fm detector, an electronic attenuator, and an audio power amplifier. The power amplifier is designed to drive, primarily, an 8-, 16-, or 32-ohm speaker, although, if the designer chooses, it may be used to drive 4- or 10-ohm or other sized loads. The amplifier has a typical power output of 5 watts with a 16-ohm load and a V+ of 30 volts. The consolidation of the functions mentioned into an integrated circuit minimizes the number of components and reduces the area of the printed circuit board necessary for this portion of a television receiver. This consolidation also permits a reduction in manufacturers' component inventories and simplifies field servicing.

The incorporation of additional features in the CA3134 results in an improvement in performance when the circuit is compared to a system in which a type such as the CA3065 is used with a discrete or integrated-circuit power amplifier. These additional features include a volume control with an improved taper, a provision for the optional use of an unattenuated audio output (fixed level unaffected by volume control position) (terminal 8), an additional power-supply-ripple bypass point (terminal 6), and a power amplifier with both current limiting and thermal-sensing shutdown protection.

Installation Considerations

The CA3134 employs the hermetic Gold-CHIP (G suffix) system, which is of the sealed-junction type designed to provide protection against humidity and other surface contaminants without a hermetic package enclosure. The semiconductor junctions are sealed by a silicon-nitride passivation layer. A multilayered, highly corrosion-resistant, terminal-connection system of special design is employed as the chip metalization.

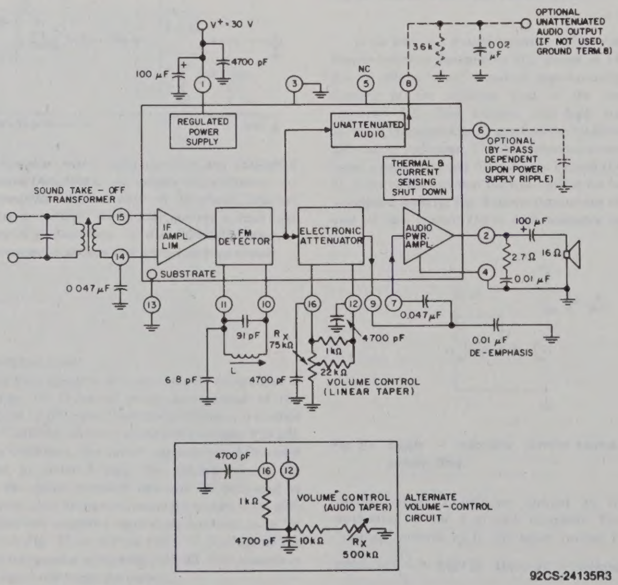


Fig. 1 - Block diagram of CA3134 in typical circuit application.

The CA3134G is encapsulated in a 16-lead plastic "power stud" package. This package has low thermal resistance, and the number of input and output terminals has not been compromised to make allowance for heat-sinking tabs. The "power stud" package lends itself to a wide variety of heat-sink methods depending on the application requirements. The CA3134GM and CA3134GQM are similar to the CA3134G except that they incorporate a tin-plated copper-strap heat sink. The CA3134GQM also has quad-formed leads.

The CA3134G is designed for applications in which it is desired to employ other than the standard heat-sinked configurations. Heat sinks similar to the type provided with the CA3134GM or GQM may also be attached to the CA3134G.[2]

Circuit Description

The CA3134 is designed primarily for use with either a single- or double-tuned sound take-off transformer (balanced input) to couple the sound if frequency (4.5 MHz) output from the video detector stage to the CA3134. This transformer serves both for impedance matching and as a band-width-limiting network to help reject unwanted frequencies such as intermodulation frequency products. Other undesired signals including residual am video information and sync information. Fig. 4 shows the overall circuit diagram for the CA3134.

Sound IF Amplifier-Limiter

The sound if stage amplifies the input signal until clipping eliminates am video and sync signals. In a typical TV system, the signal level available to the sound if amplifier-limiter is 35 mV rms. At this signal level, the input impedance components at terminals 14 and 15 of the CA3134 consist of a resistance, R_p, of approximately 25 kilohms in parallel with a capacitance, C_p, of approximately 3 pF. The sound if amplifier provides enough gain to bring the input signal level to an amplitude suitable for fm detection, but not so high as to cause PC layout or coupling problems, Fig. 2.

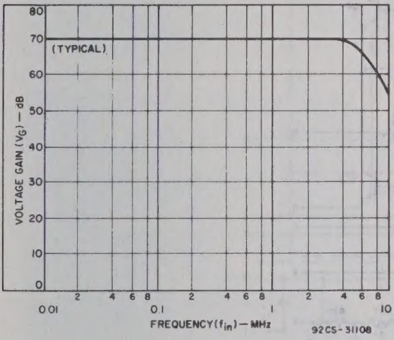


Fig. 2 - Voltage gain of if amplifier as a function of frequency.

As shown in Fig. 4, the if amplifier consists of four stages of differential amplifiers, Q15-Q16, Q19-Q20, Q23-Q24, and Q27-Q28, using resistors R13, R16, R19, and R24 as constant-current sinks; each stage is followed by emitter followers, Q17, Q21, and Q25. Because the differential amplifier functions as a limiter, am signals are eliminated and the signal into Q30 consists of constant-amplitude, frequency-modulated square waves. These square waves are shaped into approximate sine waves by Q30 and its associated RC networks to assure proper operation of the fm detector. The signal output from R31 into the base of Q41 and to terminal 10 is a constant-amplitude fm sine wave.

FM Detector

The fm sine wave at terminal 10 constitutes the input signal to the differential peak detector stage. The extracted signal contains the audio information. The detector section is formed by the differential amplifier configuration comprising transistors Q31, Q32, Q35, Q36, Q40, and Q41. Transistors Q31 and Q41 are emitter followers that operate at approximately 0.3 mA and provide high impedance at each input of the detector (terminals 10 and 11). Transistors Q32 and Q40, which operate at approximately 10 microamperes, along with the 15-picofarad capacitors C3 and C4 and the external frequency-sensitive network on terminals 10 and 11, perform peak or envelope detection. As shown in Fig. 1, this frequency-sensitive network consists of a parallel LC network in series with a 6.8-pF capacitor. The signal voltage (from Q30) is applied across the entire network connected to terminal 10. The portion of the signal from Q30 that is across the external 6.8-pF capacitor is applied to terminal 11, and the resulting difference in these signals provides the basic S curve used in the recovery of the audio signal from the fm signal.

An advantage of the differential peak detector is that it requires the alignment of only one single-tuned coil. This coil (L in Fig. 1) can be aligned by any one of the following methods (with an input terminated in 50 ohms, f_o = 4.5 MHz, f_m = 400 Hz, $\Delta f = \pm 25$ kHz, and a voltage at terminal 15 (V_{15}) $\simeq$ 100 mV rms):

1. Tune L for maximum recovered audio. To minimize thermal effects on alignment, the volume control should be adjusted so that the maximum recovered audio level at the load is limited to a low power level (approximately 0.1 watt or less).
2. Tune L for maximum recovered audio and fine tune for minimum distortion.
3. With no rf input signal, note the dc voltage at terminal 9. Then apply a 4.5-MHz cw signal and adjust the detector coil L until the dc voltage at terminal 9 is the same as the value noted.

After aligning the differential peak detector coil, align the input transformer by reducing the fm input signal level until the recovered audio level drops approximately 3 dB. Then tune the input transformer for a maximum recovered audio level while the input level of the if amplifier-limiter is below its limiting point. Fig. 3 shows the recovered audio, am rejection, and signal-to-noise ratio for the CA3134 as a function of rf input level.

Volume Control and Electronic Attenuator

Control of the audio signal detected by the differential peak detector is accomplished by differential amplifiers Q33-Q34 and Q38-Q39.

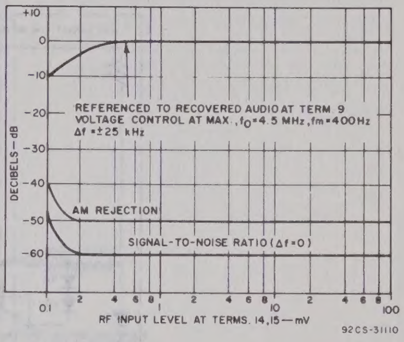


Fig. 3 - Recovered audio and signal-to-noise ratio as functions of rf input level.

The volume is controlled when the bias levels of the differential amplifiers are changed by a current flowing through an external fixed resistor between terminals 12 and 16. The amount of current flowing through this external resistor (which determines the level of recovered audio) is controlled by the position of the variable resistance (volume control) relative to ground. The voltage reference at terminal 16 is established by internal zener diode Z2, approximately 6 volts. The maximum level of recovered audio, therefore, occurs when no currents other than the base currents for Q34 and Q39 are being drawn from the zener diode through the external resistor. When the volume control is adjusted for the minimum level of recovered audio, the current drawn from terminal 16 should be limited to less than 1 milliampere.

This method of controlling the recovered audio has a very predictable volume-control taper, which can be modified to suit the designer's preference by changing the external component values. In addition, it allows for either a one- or two-wire volume control. The one-wire volume control (Fig. 4, alternate volume-control circuit) requires only one wire from the printed circuit board to the external volume control, but requires that the value of the variable resistor be large (approximately 500 kilohms) and that the resistor have an audio taper to assure an acceptable change of audio output level with a linear change (rotation) of the volume-control. The two-wire volume control allows the use of a volume control having a lower value of resistance and a linear taper.

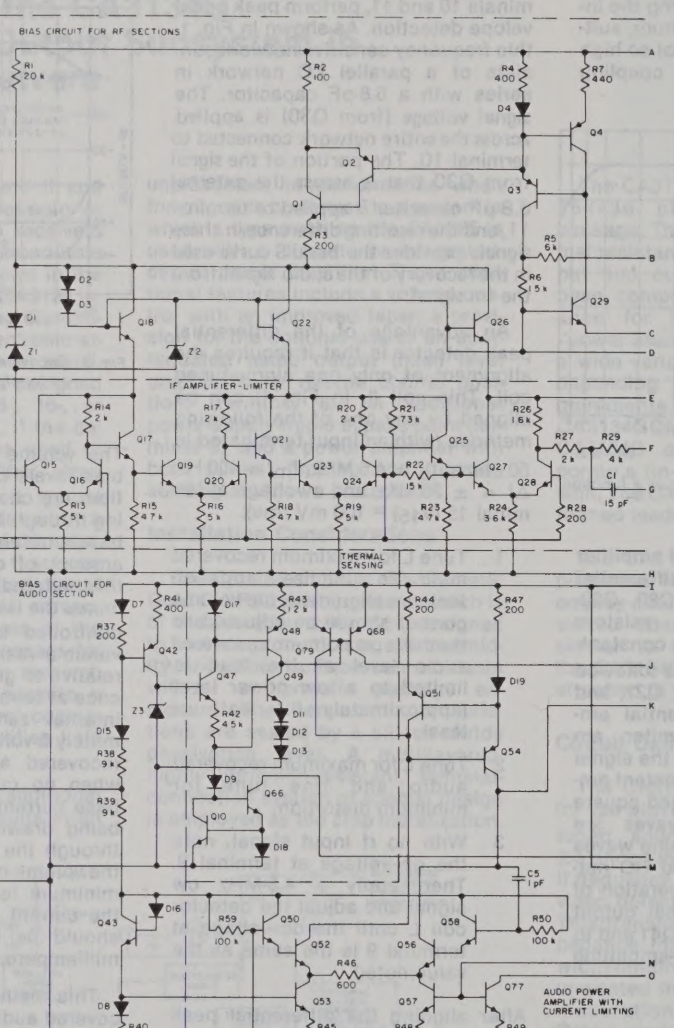


Fig. 4 - Schematic diagram of CA3134.

The output impedance of the electronic attenuator (terminal 9) is typically 7.5 kilohms (R5 + R6). A tone control may be inserted between the output of the electronic attenuator and the input of the audio power amplifier (terminal 7).

Unattenuated Audio Output

The operation of Q38 and Q39 is duplicated by Q33 and Q34 as the volume control is varied. The currents from Q33 and Q34 are combined by the current-mirror configuration produced by D5, Q5, Q6, and Q8, Q12. When an external resistor is placed between terminal 8 and ground, the current from this current-mirror configuration produces a recovered audio voltage at a fixed level independent of volume-control position. This output may be used to mute the sound in the event the broadcasting station loses its sound carrier or broadcast signal or to allow for the direct recording of the audio portion of a program.

Audio Power Amplifier

The audio power amplifier is a quasi-complementary class AB type with a typical voltage gain of 35dB. Internal feedback eliminates the need for external feedback compo-

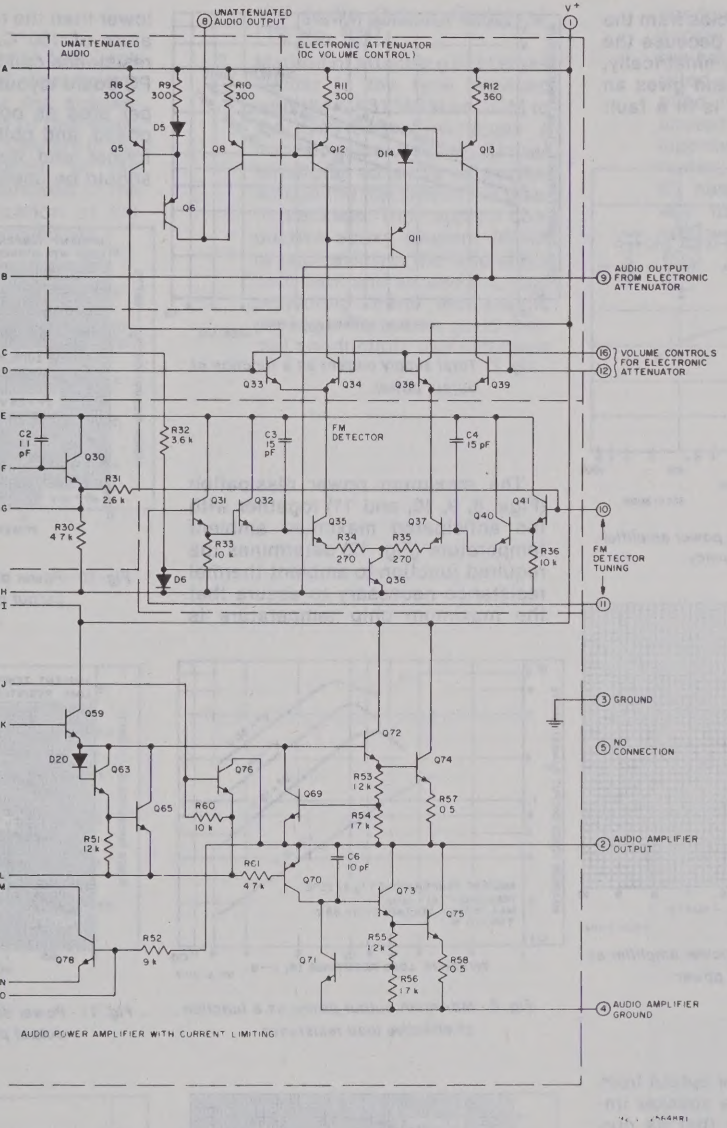


Fig. 4 – Schematic diagram of CA3134.

nents, especially costly electrolytic capacitors. The input impedance (at terminal 7) is typically 100 kilohms (R59). Fig. 5 shows the frequency response of the audio power amplifier and Fig. 6 its efficiency. Both current limiting and thermal shutdown protection are provided. Current limiting is accomplished by limiting the drive to the output transistors from the driver transistors Q72 and Q73. The limiting drive is determined by the feedback from R53, R54, and Q69 to Q72, and R55, R56, and Q71 to Q73. When the peak output current exceeds approximately 0.8 ampere, the voltage developed across the emitters of Q72 and Q73 will cause Q69 and Q71, respectively, to conduct, thereby limiting the drive to the output transistors Q74, Q75.

When the chip temperature exceeds 150 °C, the thermal-sensing portion of the CA3134 begins to shut down the power amplifier by removing the bias from the power amplifier driver stages. The temperature at which the thermal shutdown circuitry is activated is determined by the relative areas of D9, Q66, and D18 and those of Q49, D11, D12, and D13. When Q49 conducts, transistors Q79, Q68, and Q76 are in turn biased into conduction and remove bias from the amplifier driver stages. Because the drive is not removed symmetrically, the signal is distorted and gives an indication that the unit is in a fault condition.

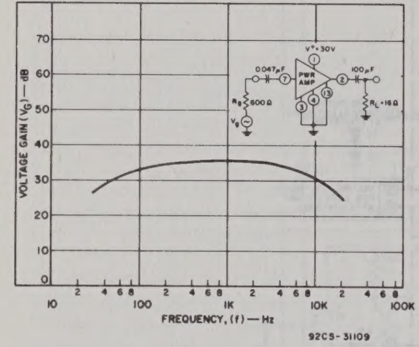


Fig. 5 - Voltage gain of audio power amplifier as a function of frequency.

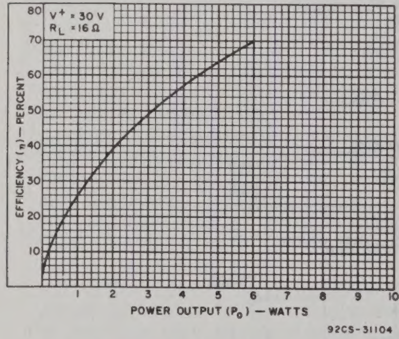


Fig. 6 - Efficiency of audio power amplifier as a function of output power.

Application

For the required power output from the CA3134 (Fig. 7), the speaker impedance must be such that its current drain will be both within the capability of the power supply and less than the current-limiting level of the CA3134. To decouple the CA3134 from the power supply and provide a means for preventing excessive drive to the speaker, a series resistor should be placed between the power supply and terminal 1. The value of this resistor depends upon the required power output level for the worst-case power supply voltage condition. This resistor also reduces the amount of power dissipated in the CA3134.

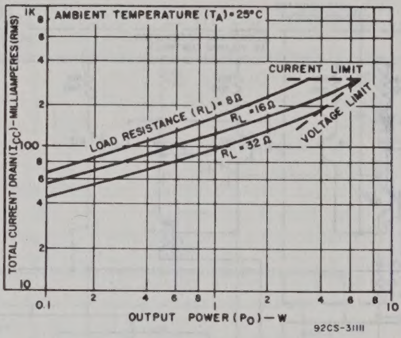


Fig. 7 - Total supply current as a function of output power.

The maximum power dissipation (Figs. 8, 9, 10, and 11) together with the anticipated maximum ambient temperature (Fig. 12) determines the required junction-to-ambient thermal resistance necessary to assure that the maximum chip temperature is lower than the rated junction temperature of 150°C. The overall thermal resistance can be lowered by careful PC board layout. As much of the copper area as possible should be exposed, and coil shields (input transformer and detector tuned circuit) should be used to help radiate heat.

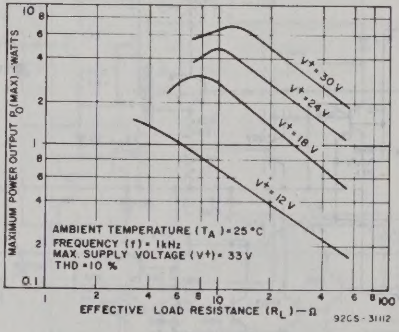


Fig. 8 - Maximum output power as a function of effective load resistance.

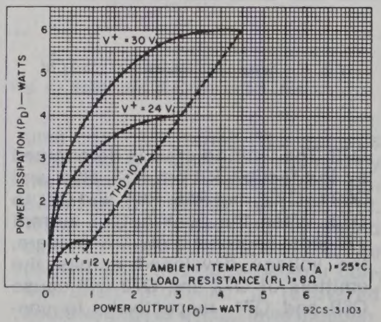


Fig. 9 - Power dissipation as a function of output power at R_L = 8 ohms.

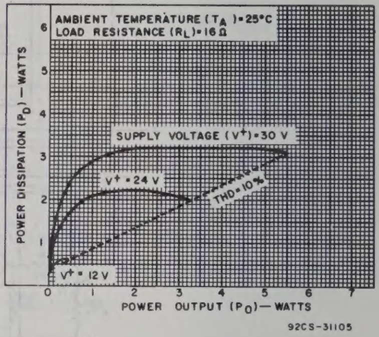


Fig. 10 - Power dissipation as a function of output power at R_L = 16 ohms.

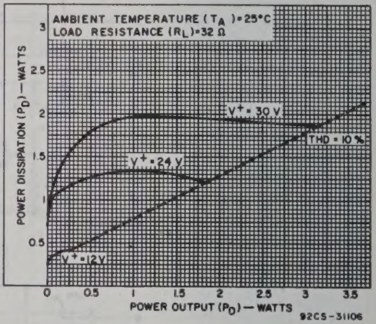


Fig. 11 - Power dissipation as a function of output power at R_L = 32 ohms.

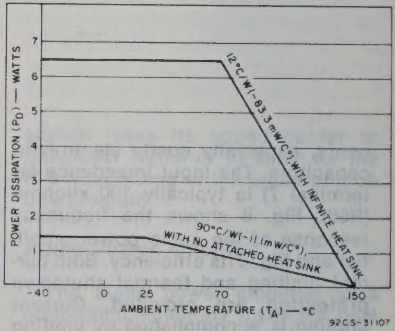


Fig. 12 - Maximum power dissipation as a function of ambient temperature.

Acknowledgment

The author is indebted to both Jack Craft for many helpful discussions and Wayne Austin for his suggestions in the preparation of this Note. The contributions of H. Chinery in the electrical characterization of the CA3134 and Ralph Thompson in the mechanical characterization of the stud package are acknowledged.

References

1. RCA Solid State Data Sheet for CA3134 types, "TV Sound IF and Audio Output Systems," File No. 1097.
2. Method of attaching heat sinks similar to the type provided with the CA3134GM or GQM to the CA3134G. First apply a non-conductive epoxy (Uniset structural adhesive or equivalent) to the top side of the plastic package. Then apply a conductive epoxy (Dupont 5504A or equivalent) in the hole of the heat sink and around the stud projecting from the plastic package. To assure good thermal conduction, use sufficient conductive epoxy to allow the excess to be forced through the hole when the heat sink is fitted over the stud. Stress applied to the stud should be limited to less than 3 in-lbs (approximately 0.35 newton-meter), 15 lbs (approximately 65 newtons) of tension, and 100 lbs (approximately 445 newtons) of compression.

ICAN-6732

Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits

by T. J. Robe

The advent in recent years of very high-gain operational amplifiers operating in the l/f noise-frequency spectrum has placed emphasis on the need for very low-noise devices. This need is particularly true for operational amplifiers which have either low-offset characteristics and/or offset-null capability.

The traditional methods used to select such devices involve the measurement of either spot or wideband (≈ 10 kHz) noise figures in the l/f frequency range (10 Hz to 10 kHz) at various source resistances. This type of measurement, however, only provides an indication of the average noise power at the measurement frequency and does not reveal the burst ("popcorn") noise characteristics of the Device Under Test (DUT). The metering circuits cannot respond fast enough to measure the effects of burst-noise. Fig. 1a shows a photograph of typical burst-noise as a function of time for an operational amplifier having poor burst-noise characteristics. This photo illustrates burst-noise which is characterized by random abrupt output voltage-level changes that persist for periods from approximately 1/2 millisecond to several seconds. Additionally, the random rate at which the bursts occur ranges from approximately several hundred per second to less than one per minute. Furthermore, these rates are not necessarily repetitive and predictable. Consequently, the nature of burst-noise prevents its measurement by means of the standard averaging techniques. Instead, a technique to detect individual bursts must be used and a DUT must be under observation for a period in the order of 10 seconds to one minute. Fig. 1b shows a photo of the output of a virtually burst noise-free operational amplifier, the RCA-CA6741T.

Test Configuration

Some of the major questions relevant to the type of test required are:

1. What characteristics of the burst-noise should be detected?
2. What test-circuit configuration is most suitable to detect these characteristics?

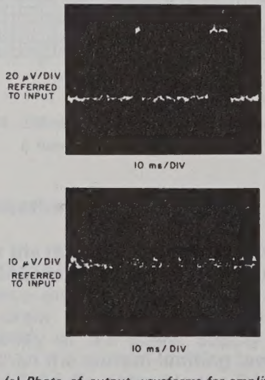


Fig. 1— (a) Photo of output waveforms for amplifier with poor burst-noise characteristics; (b) photo of output waveform for the RCA-CA6741T.

3. What are the "Pass-Fail" criteria?

There are three major characteristics of the noise burst which have an impact on the suitability of a device from the standpoint of applications: burst amplitude, duration, and rate of occurrence. Of these, burst-amplitude and rate of occurrence are of primary interest to potential users of a particular device. Long duration bursts (of sufficient amplitude) seriously degrade the performance of dc amplifiers; however, suitable devices could be selected by the rejection of any unit which produced even one burst during some prescribed test period. Therefore, an absolute measurement of burst duration is not a prime necessity.

The rate of occurrence, on the other hand, as measured by the burst-count in a given test period could conceivably be considered as a variable of prime importance in the selection process. For instance, a burst-rate of 100 per second is clearly objectionable in almost any low-level low-frequency application, whereas the occurrence of only one low-amplitude burst in a one-minute period might be quite acceptable. Consequently, it is desirable to include flexibility in the testing system so that "Pass-Fail" criteria can be established on the basis of burst-noise count in some prescribed period of time. The test equipment described herein detects total noise (l/f noise plus burst noise) bursts with amplitudes above a preset threshold level during a given test period and allows acceptance or rejection on the basis of the number of noise voltage excursions beyond the threshold level, in the selected test period.

Another factor to be considered is the bandwidth of the test system. Excessive bandwidth allows the normal "white" noise of the terminating resistors and the DUT to obscure burst-noise occurrences and does not realistically simulate the low-frequency applications in which burst-noise is particularly objectionable. On the other hand, a test circuit having excessively narrow bandwidth prevents detection of the shorter-duration bursts (≈ 1/2 ms) even if their amplitude is relatively high. A suitable compromise is chosen in which the system rise time permits a burst of "minimum" duration to reach essentially its full amplitude. Because the rise time and bandwidth of an amplifier are related by the equation:

$$BW \approx \frac{0.4}{t_r}$$

the minimum bandwidth to detect a 0.5 ms burst is approximately:

$$BW_{min} = \frac{0.4}{(0.5)(10^{-3})} = 0.8\ \text{kHz}.$$

Consequently, a 1 kHz bandwidth has been selected as a reasonable one for a burst-noise test system and, therefore, prescribes the need for a low-pass filter in the system.

The test requirements outlined above can be implemented with the following circuit elements shown in the block diagram of Fig. 2a. Fig. 2b shows the complete system schematic:

1. A fixed high-gain amplifier incorporating the DUT as the first stage to amplify the microvolt-level burst to an easily detectable level (this should be a burst noise-free unit);
2. A low-pass filter to limit the test bandwidth to approximately 1 kHz,
3. A comparator to produce a fast-rise high-level single-polarity output pulse whenever an input burst-noise pulse (of either polarity) exceeds a preset (but adjustable) threshold level;
4. A counter to tally the number of pulses emanating from the comparator during the test period: a single decade counter is adequate.
5. A latch circuit which trips to the "latched" state when the count exceeds a preselected number (e.g. 1 to n). The latch circuit, if tripped, energizes an indicator lamp.
6. A timer to control the period over which the counter is enabled. It should incorporate the capability to reset both the counter and the latch circuit at the beginning of each test period.
7. Power supplies for the DUT and other auxiliary circuits.

Test Conditions

Some of the conditions which affect the burst-noise performance of the DUT include bias-level, source resistance (Rs), and ambient temperature (T_A).

The quiescent operating conditions in operational amplifiers are normally set by the magnitude of the positive and negative supplies. Many of the newer Op-Amp types, however, have bias-terminals into which fixed currents can be injected to set their performance characteristics. The RCA-CA3060, CA3080, and CA3080A Operational Transconductance Amplifiers (OTA's) and; the RCA-CA3078 and CA3078A Micropower Op-Amps are examples of such devices. For best low-frequency and burst-noise performance, these amplifiers should be operated at the lowest bias

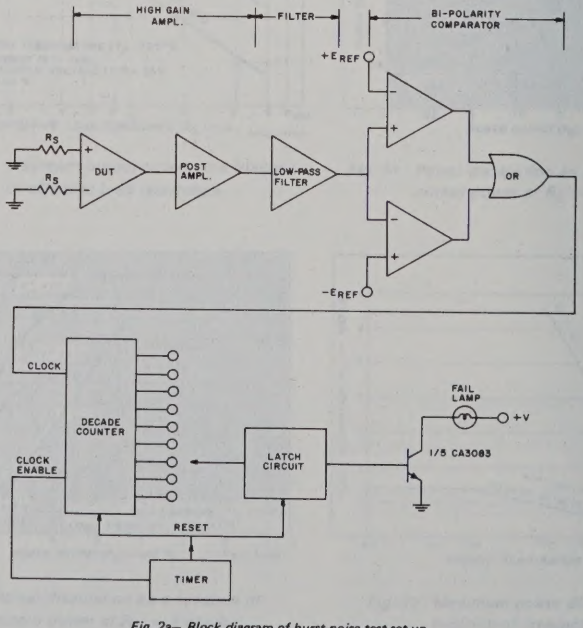
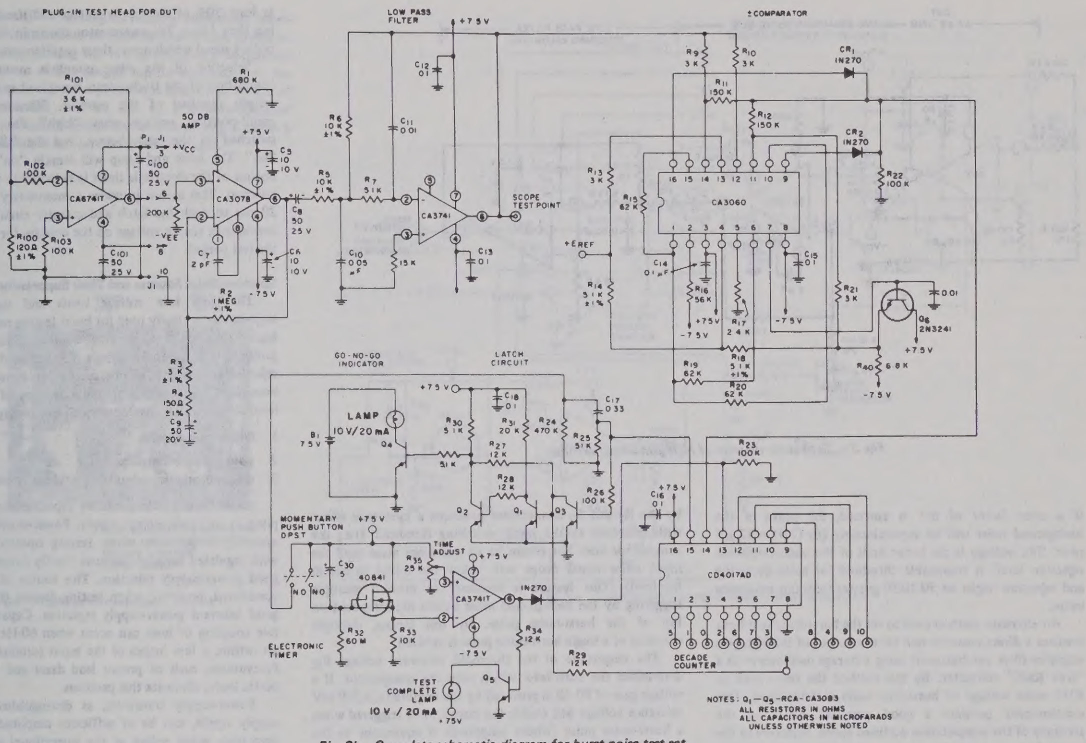


Fig. 2a— Block diagram of burst-noise test set-up.



NOTES: Q1—Q5 -RCA-CA3083
ALL RESISTORS IN OHMS
ALL CAPACITORS IN MICROFARADS
UNLESS OTHERWISE NOTED

Fig. 2b– Complete schematic diagram for burst noise test-set.

currents consistent with the gain-bandwidth requirements of the particular application.

In the test for burst noise, the source resistance (Rs) seen by the input terminals of the DUT, is a key test parameter. Burst noise causes effects which are equivalent to a spurious current-source at the device input and, therefore, burst-noise current generates an equivalent input noise-voltage in proportion to the magnitude of the source resistance through which it flows. Accordingly, to increase the sensitivity of the test system, it is desirable to use the highest source resistance consistent with the input offset-current of the DUT. For example, an Op-Amp which has 0.1 μA inout offset current could realistically be tested with source-resistance in the order of 100KΩ (10 mV input offset), whereas a 1 MΩ source-resistance (100 mV input offset) could cause excessive offset in the output. For 741 type Op-Amps a 100kΩ resistance is recommended.

Burst-noise generation in amplifiers is usually more pronounced at lower temperatures (particularly below 0°C). Consequently, consideration must be given to the temperature of the DUT in relation to the temperature range under which the device is expected to perform in a particular operation.

A test parameter of importance is the time duration of observation. Because the frequency of burst-noise occurrence is frequently less than once every few seconds, the minimum test period should be in the range of from 15 to 30 seconds.

Pass-Fail Criteria

A test system built to accommodate the test philosophy outlined above has the ability to reject or pass a DUT on the basis of two variables: burst-amplitude and the frequency of burst occurrence. The burst-amplitude which will trip the counter can be no lower than the background l/f noise peaks of burst-free units, otherwise normal background noise will fail the DUT.

The background noise peaks depend on the source termination Rs, the wide band l/f noise figure of the DUT, and the test system bandwidth. A good estimate of the normal background noise-peak levels can be computed from the definition of noise factor and an empirically determined noise-crest factor of approximately 6:1. The crest-factor is the ratio of the maximum peak-noise voltage to the RMS noise voltage. The noise factor is defined as the ratio of the total noise power at the amplifier output to the output-noise power due to the source resistors alone. In terms of the RMS noise voltages at the input terminals of the amplifier this is equivalent to:

$$\text{Noise Factor (F)} = \frac{E^2\text{input noise total}}{E^2\text{noise source resist}} = \frac{(E_{NTi})^2}{(E_{NRS})^2} \qquad (1)$$

E_{NTi} is the total input noise-voltage, i.e., the sum of noise generated in the source termination resistance and noise generated by the DUT.

E_{NRs} is that part of E_{NTi} due to Rs alone.

$$\text{Therefore,} \qquad E_{NTi} = (\sqrt{F})\,(E_{NRs}). \qquad (2)$$

E_{NRs} can be computed by using the well known expression for "white-noise" generated across the terminals of a resistor (R):

$$E_{NR}(\text{RMS}) = \sqrt{4kTBR} \qquad (3)$$

where k = Boltzmans Constant = 1.372×10^{-23} j/°K

T = Absolute Temperature in °K
B = Noise Bandwidth in Hz
R = Value of the resistor in ohms.

Thus, at a room temperature of 290°K

$$E_{NR}(\text{RMS}) = 1.28 \times 10^{-10} \sqrt{BR}$$

For example, a 100 kΩ resistor preceding a system with a bandwidth of 1 kHz will generate a noise-voltage of

$$(1.28 \times 10^{-10}) \quad (\sqrt{10^3 \cdot 10^5}\ ) \quad = 1.28\ \mu V_{RMS}$$

Both inputs of an Op-Amp are usually terminated in Rs, hence it is necessary to combine the effects of both resistors to determine the effective E_{NRs} at the input of the DUT. Because the noise voltages from these two resistors are uncorrelated their voltages must be added vectorally rather than algebraically.

$$E_{NRs}\,(\text{effective}) = \sqrt{(E_{NR_{s1}})^2 + (E_{NR_{s2}})^2} \qquad (4)$$

because $E_{NR_{s1}} = E_{NR_{s2}}$, when $R_{s1} = R_{s2}$

$$E_{NRs}\,(\text{effective} = (\sqrt{2})\ (E_{NRs})$$

and for 1 kHz bandwidth at 290°K

$$E_{NRs}\,(\text{effective}) = (\sqrt{2})\,(1.28\ \mu V) = 1.81\ \mu V_{RMS.}$$

If in this example, the DUT has a wideband l/f noise figure of 4 dB (2.5:1 power ratio) the total RMS background noise-voltage at the input will be

$$E_{NTi} = (\sqrt{F})\ (E_{NRs})\ \text{(from eq.(2))}$$
$$= (\sqrt{2.5})\ (1.81) = 2.9\ \mu V_{RMS}$$

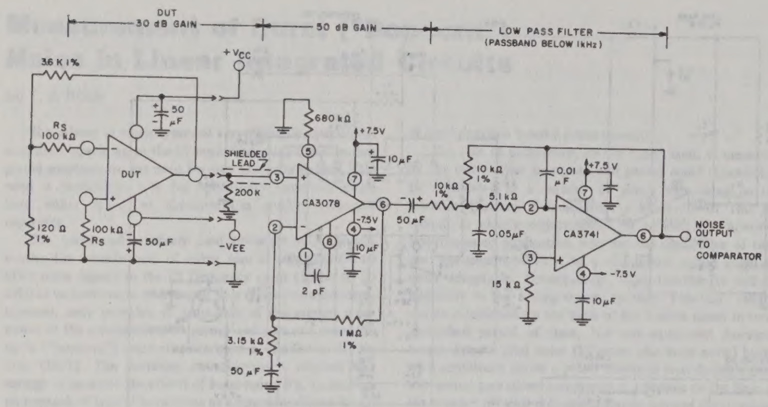


Fig. 3– Schematic diagram of high-gain amplifier/filter.

If a crest factor of 6:1 is assumed, the peaks of the background noise will be approximately $(6)\ (2.9) = 17\ \mu V$ peak. This voltage is the lower limit of the burst-amplitude rejection level. A reasonable threshold for burst detection and rejection might be 50-100% greater than this minimum value.

An alternate method used to set the burst-threshold limit involves a direct measurement (at the output of the high gain amplifier-filter combination) using a storage oscilloscope or a "true RMS" voltmeter. By this method the noise peak or RMS noise voltage of burst-free units is determined. This measurement provides a good practical check on the accuracy of the computation outlined above. Selection of the acceptable number of burst counts in the test period is arbitrary, but dependent on the type of application intended for the DUT. To be acceptable in some critical applications, the DUT may not generate even a single burst-pulse in a relatively long period of time.

Burst-Noise Test System Circuits

1. High gain Amplifier – Filter

Fig. 3 shows the schematic diagram of the high-gain amplifier-filter which provides a fixed gain of 80 dB with a 12 dB octave roll-off above 1 kHz. The gain-function is somewhat arbitrarily distributed between the DUT and post-amplifier: 30 dB and 50 dB respectively. This distribution is based on the need for sufficient gain in the DUT portion to eliminate significant noise-signal contributions from the second stage while simultaneously allowing adequate loop-gain in each stage to provide accurate gain-setting with precise external resistors. The first stage is shown as a plug-in module so that any type of DUT configuration having 30 dB gain can be tested.

The capacitive coupling employed provides a low frequency cutoff of about 1 Hz and eliminates the need for dc-offset zero-adjustments. The dc offset-voltage at the filter output is less than 5 mV which corresponds to less than 0.5 µV error when referred to the noise input (an 80 dB gain is assumed.) Several seconds must be allowed, however, for the DC operating point to stabilize after the power is applied to the DUT.

2. Bi-Polarity Comparator

Fig. 4 shows the schematic diagram for the threshold-detecting comparator. Because bursts of either polarity must be detected and converted to positive output pulses, two comparators are required: one having a positive-threshold reference and the other having a negative-threshold reference of equal magnitude. The RCA CA3060 triple OTA is convenient to use because a single package provides circuits for both comparators plus a reference inverter for the negative threshold reference. The positive feedback provided by the R_f and R_i connections produces a hysteresis effect with reference to the input switching threshold, (i.e., the comparator does not return to its quiescent state until the input noise signal drops well below the initial threshold trip-level). This feature is necessary to prevent multiple triggering by the background noise signals superimposed on top of the burst-noise pulse. By this means, multiple counting of a single burst-noise pulse is avoided.

The magnitude of the threshold reference voltage E_R determines the burst-level which trips the comparator. If a voltage gain of 80 dB is provided by the amplifiers, a 200 mV reference voltage will enable the circuit to be triggered when a burst-noise pulse (whose amplitude is equivalent to the level of 20 µV referred to the DUT input) is present.

3. Counter-Latch-Timer Control Circuits

The remaining circuits of the go-no-go burst-noise tester are shown in Fig. 5. The decade-counter is incorporated in a single COS/MOS IC (RCA CD4017AE) which has clock, reset, and enable inputs, and an output terminal for each of ten count-positions (0 to 9). A carry-out signal is available if the use of more than a single decade is desired. The clock input-signal must be positive-going and have a magnitude of at least 70% of the supply-voltage and rise-time equal to or less than 15 µs. The comparator shown in Fig. 4 provides an output signal which meets these requirements.

Selection of the reject count is made by a pin-jack connection of the latch-circuit input-lead to the appropriate output terminal of the counter. Whenever the selected count-position voltage goes "high" the latch-circuit is switched to the latched-state, and the fail-indicator lamp "on". The latch and lamp will remain "on" until the reset button of the electronic timer is switched to the "Timer On" position. This action provides a momentary reset signal (≈ 20 ms) to both the latch and counter circuits and places a continuous enable voltage on the counter for the duration of the test period.

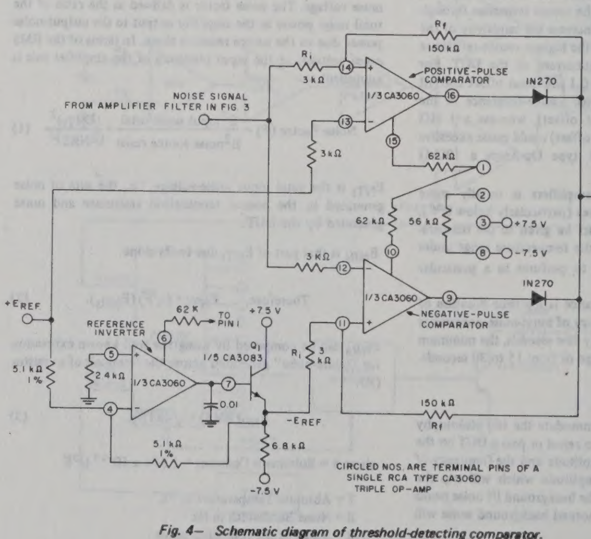
Spurious Noise Sources and Their Suppression

The very low voltage levels and the high source impedances normally used for burst testing render the system highly susceptible to external spurious noise sources. This problem is particularly serious if a test unit is going to be rejected for as little as one or two input burst-noise pulses exceeding 20-30 µV. The major sources of spurious noise encountered in the development of this test system were:

1. 60-Hz hum pickup,
2. power supply transients,
3. electromagnetic pick up of switching transients.

60-Hz hum is introduced by capacitive or inductive coupling or as power-supply ripple. Power-supply ripple is not normally a problem when testing operational amplifiers with regulated supplies, because the Op Amps generally have good power-supply rejection. This source of noise must be considered, however, when testing devices that do not have good inherent power-supply rejection. Capacitive or inductive coupling of hum can occur when 60-Hz line cord leads are within a few inches of the input terminals of the DUT. Precautions, such as proper lead dress and twisting of the 60-Hz leads, eliminate this problem.

Power-supply transients, as distinguished from power-supply ripple, can be of sufficient amplitude to introduce detectable noise pulses at the operational amplifier input. Such transients are produced when other equipment on the same ac line is switched on or off. A typical power-supply rejection ratio for an operational amplifier is 50 µV/V (i.e. a 1 volt transient on the power-supply is equivalent to a 50 µV noise pulse at the DUT input). This example demonstrates that the test system cannot tolerate power-supply transients greater than approximately 100 mV even when testing units with good power-supply rejection. Unless the power-supply is known to be free of such transients, a battery-operated system is recommended. Even when this system is battery-



CIRCLED NOS. ARE TERMINAL PINS OF A SINGLE RCA TYPE CA3060 TRIPLE OP-AMP

Fig. 4– Schematic diagram of threshold-detecting comparator.

operated, "On-Off" switching of nearby equipment introduces detectable transients into the system. These problems are eliminated by placing the test circuitry in a completely shielded enclosure with a hinged top for easy access to the test unit. The external noise problem is best solved by use of a shielded enclosure and by use of a battery-operated power-supply contained within the enclosure. Fig. 6 shows a photo of the circuit board layouts of the test unit.

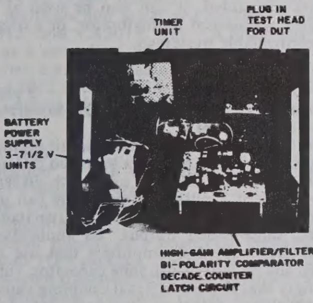

TIMER UNIT
PLUG IN TEST HEAD FOR DUT
BATTERY POWER SUPPLY 3-7 1/2 V UNITS
HIGH-GAIN AMPLIFIER/FILTER
BI-POLARITY COMPARATOR
DECADE COUNTER
LATCH CIRCUIT

Fig. 6— Photo of circuit-board layout.

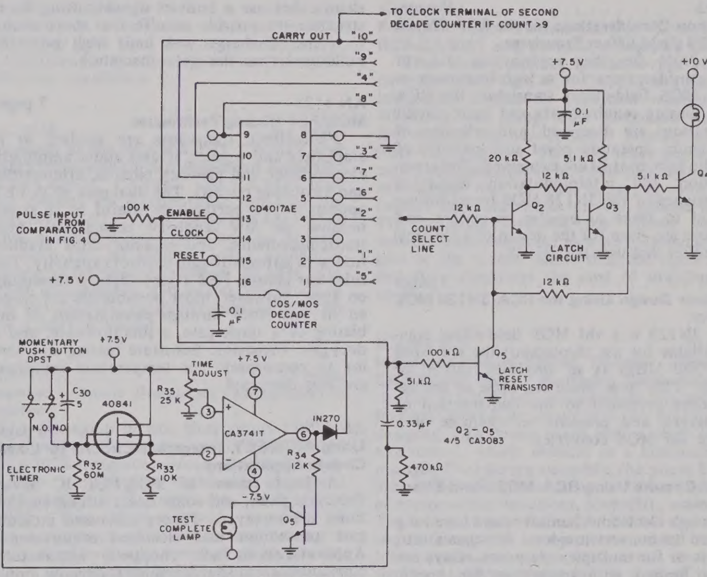


Fig. 5— Counter-latch-timer-control circuit schematic.

Abstracts of Other Application Notes

AN-3193 . . . . 9 pages
Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor

This Note describes applications and vhf circuit considerations for a high-frequency n-channel MOS field-effect transistor, the RCA 3N128. Biasing requirements and basic circuit configurations are discussed, and selection of the optimum operating point and methods of automatic gain control are explained. The cross-modulation and intermodulation distortion characteristics of the 3N128 MOS transistor are compared to those of bipolar transistors, and procedures are given for the design of a practical vhf amplifier that uses the 3N128.

AN-3341 . . . . 3 pages
VHF Mixer Design Using the RCA-3N128 MOS Transistor

The 3N128 is a vhf MOS field-effect transistor suitable for use throughout the vhf band (30 to 300 MHz) as an amplifier, mixer, or oscillator. This Note discusses some of the design criteria pertinent to the construction of MOS mixers, and presents an example of a complete vhf MOS converter.

AN-3452 . . . . 7 pages
Chopper Circuits Using RCA MOS Field-Effect Transistors

Although electromechanical relays have long been used to convert low-level dc signals into ac signals or for multiplex purposes, relays are seriously limited with respect to life, speed, and size. Conventional (bipolar) transistors overcome the inherent limitations of relays, but introduce new problems of offset voltage and leakage currents. This Note describes the use of MOS field-effect transistors in solid-state chopper and multiplex designs that have the long life, fast speed, and small size of bipolar-transistor choppers, but that eliminate their inherent offset-voltage and leakage-current problems.

AN-3453 . . . . 6 pages
An FM Tuner Using an RCA-40468 MOS-Transistor RF Amplifier

This Note describes an FM tuner that incorporates an MOS field-effect transistor as the rf amplifier, and shows how the MOS transistor is instrumental in minimizing the spurious responses normally found in FM receivers.

AN-3535 . . . . 6 pages
An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer

Selection of the transistors for use in FM-tuner stages involves consideration of such device characteristics as spurious response, dynamic range, noise immunity, gain, and feed-through capacitance. MOS field-effect transistors are especially suitable for use in FM rf-amplifier and mixer stages because of their inherent superiority for spurious-response rejection and signal-handling capability. This Note describes an FM tuner that uses an RCA-40468 MOS transistor as the rf amplifier and an RCA-40559 MOS transistor as the mixer.

AN-4018 . . . . 5 pages
Design of Gate-Protected MOS Field-Effect Transistors

MOS (metal-oxide-semiconductor) field-effect transistors are in demand for rf-amplifier applications because their transfer characteristics make possible significantly better performance than that experienced with other solid-state devices. Unless equipped with gate protection, however, MOS transistors require careful handling to prevent static discharges from rupturing the dielectric material that separates the gate from the channel. This Note describes the design of dual-gate MOS field-effect transistors that use a built-in signal-limiting diode structure to provide an effective short circuit to static discharge and limit high potential buildup across the gate insulation.

AN-4125 . . . . 7 pages
MOS/FET Biasing Techniques

Field-effect transistors are applied in rf amplifiers and mixers, if and audio amplifiers, electrometer and memory circuits, attenuators, and switching circuits. The dual-gate MOS/FET appears to be particularly useful in rf stages because of low feedback capacitance, high transconductance, and superior cross modulation with automatic-gain-control capability. The rules for biasing FET's vary slightly depending on type. However, most possibilities are covered in this Note through examination of the biasing of a single-gate, a junction-gate, and a dual-gate transistor. Substrate biasing and biasing to compensate for temperature variations are also discussed.

AN-4590 . . . . 16 pages
Using MOS/FET Integrated Circuits in Linear Circuit Applications

A brief review of MOS/FET IC device theory is given, and some linear circuit applications are surveyed. Theory discussed includes gate protection and electrical requirements. Applications include choppers, attenuators, constant-current sources, general-purpose amplifier circuits, and rf amplifiers, oscillators, and mixers.

ICAN-4072 . . . . 8 pages
Applications of the RCA-CA3048 Integrated-Circuit Amplifier Array

The RCA-CA3048 integrated circuit, an array of four identical amplifiers, each with independent inputs and outputs, all on a single monolithic silicon chip, has an operating and storage temperature range of −25°C to +85°C. Each amplifier in the low-noise array has a typical open-loop gain of 58 dB and input impedance of 90,000 ohms. The gain-frequency response, stability, output swing versus supply voltage, and noise of the device are discussed. Circuit applications include Hartley and Colpitts Oscillators, astable multivibrators, a 4-channel linear mixer, a driver for a 600-ohm balanced line, and a gain-controlled amplifier.

ICAN-5015 . . . . 15 pages
Application of the RCA-CA3008 and CA3010 Integrated-Circuit Operational Amplifiers

This Note describes the circuit arrangement, lists the performance characteristics, explains the major design considerations, and discusses typical applications of the CA3008 and CA3010 operational amplifiers. These amplifiers are silicon monolithic integrated circuits designed to operate from two symmetrical low- or medium-level dc power supplies (at supply voltages in the range from ±3 volts to ±6 volts).

ICAN-5022 . . . . 26 pages
Application of the RCA-CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

The CA3004, CA3005, and CA3006 rf amplifiers are discussed. These silicon-epitaxial monolithic integrated circuits are designed to operate from low or medium levels of dc supply voltage, over a range of ambient temperatures from −55°C to +125°C, and at frequencies from dc to 100 MHz. They may be used with external tuned-circuit, transformer, or resistive load impedances to provide wide- or narrow-band amplification, mixing, limiting, product detection, frequency generation, and generation of pulse or digital waveforms.

ICAN-5030 . . . . 11 pages
Application of the RCA-CA3000 Integrated-Circuit DC Amplifier

This Note describes the RCA-CA3000 dc amplifier, a stabilized and compensated differential amplifier that has push-pull outputs, high-impedance (0.1-megohm) inputs, and gain of approximately 30 dB at frequencies up to one MHz. Its useful frequency response can be increased to several tens of megahertz by the use of external resistors or coils. The CA3000 can be used as a signal switch (with pedestal), a squelchable audio amplifier (with suppressed switching transient), a modulator, a mixer or a product detector. When suitable external components are added, it can also be used as an oscillator, a one-shot multivibrator, or a trigger with controllable hysteresis.

ICAN-5036 . . . . 9 pages
Application of the RCA-CA3002 Integrated-Circuit IF Amplifier

The RCA-CA3002 integrated-circuit if amplifier described in this Note is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled if amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits.

ICAN-5037 . . . . 4 pages
Application of the RCA-CA3007 Integrated-Circuit Audio Amplifier

This Application Note describes the RCA-CA3007 audio driver, a balanced differential configuration with either a single-ended or a differential input and two push-pull emitter-follower outputs. The circuit features all-monolithic silicon epitaxial construction, and is intended for use as a direct-coupled driver in a class B audio amplifier which exhibits both gain and operating-point stability over the temperature range from −55 to 125°C.

ICAN-5038 . . . . 8 pages
Application of the RCA-CA3001 Integrated-Circuit Video Amplifier

The CA3001 silicon monolithic integrated circuit is designed for use in intermediate-frequency or video amplifiers at frequencies up to 20 MHz and in Schmitt-trigger applications. This integrated circuit can be gated, and gain control can be applied. The CA3001 incorporates all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from 55 to 125°C, balanced differential-amplifier configuration with low-impedance double-ended input, and a built-in temperature-compensating network for gain or dc operating-point stability over the temperature range from 55 to 125°C.

ICAN-5213 . . . . 6 pages
Application of the RCA CA3015 and CA3016 Integrated-Circuit Operational Amplifiers

The integrated-circuit operational amplifiers CA3015 and CA3016 are identical in circuit configuration to the CA3008 and CA3010, but have an improved device breakdown voltage that permits operation from +12-volt supplies as well as from +6 volt or +3 volt supplies. This Note describes the operating characteristics of the CA3015 and CA3016 at +12 volts, and discusses applications that take advantage of the higher gain-bandwidth product and increased output signal swing obtained at the higher voltages: a 50-dB amplifier; a 10-dB, 42-MHz amplifier; a twin-T bandpass amplifier; a 20-dB, 10-MHz bandpass amplifier; and a voltage-follower.

ICAN-5269 . . . . 7 pages
Integrated Circuits for FM Broadcast Receivers

This Note describes several approaches to FM receiver design using silicon monolithic integrated circuits. The tuner section is described first, and then the if-amplifier and detector sections. Performance characteristics are described where applicable. The FM receivers discussed are designed for use from a +9-volt supply. The key to design simplicity is the use of the RCA multifunction integrated circuits CA3005, CA3012, and CA3014. The CA3005 may be used as a cascode rf amplifier, a differential rf amplifier, a mixer-oscillator, and an if amplifier; the CA3012 and CA3014 perform if amplification, limiting, detection, and preamplification.

ICAN-5296 . . . . 5 pages
Application of the RCA-CA3018 Integrated-Circuit Transistor Array

The CA3018 integrated circuit consists of four silicon epitaxial transistors produced by a monolithic process on a single chip mounted in a 12-lead TO-5 package. The four active devices, two isolated transistors plus two transistors with an emitter-base common connection, are especially suitable for applications in which closely matched device characteristics are required, or in which a number of active devices must be interconnected with non-integrable components such as tuned circuits, large-value resistors, variable resistors, and microfarad bypass capacitors. Such areas of application include if, rf (through 100 MHz), video, agc, audio, and dc amplifiers.

ICAN-5299 . . . . 6 pages
Application of the RCA-CA3019 Integrated-Circuit Diode Array

The CA3019 integrated circuit diode array provides four diodes internally connected in a diode-quad arrangement plus two individual diodes. Its applications include gating, mixing, modulating, and detecting circuits. Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations. Consequently, the CA3019 is particularly useful in circuit configurations that require either a balanced diode bridge or identical diodes.

ICAN-5337 . . . . 10 pages
Application of the RCA-CA3028A and CA-3028B Integrated-Circuit RD Amplifiers in the HF and VHF Ranges

The CA3028A and CA3028B monolithic-silicon integrated circuits are single-stage differential amplifiers intended for service in communications systems operating at frequencies up to 100 MHz with single power supplies. This Note provides technical data and recommended circuits for use of the CA3028A and CA3028B in rf amplifiers, autodyne converters, if amplifiers, and limiters. The CA3028A and CA3028B are suitable for use in a wide range of applications in dc, audio, and pulse amplifier service; they have been used as sense amplifiers, preamplifiers for low-level transducers, and dc differential amplifiers.

ICAN-5338 . . . . 14 pages
Application of the RCA-CA3021, CA3022, and CA3023 Integrated-Circuit, Wideband Amplifiers

The CA3021, CA3022, and CA3023 integrated circuits are multipurpose high-gain amplifiers designed for use in video and AM or FM if stages in single-power-supply systems. Specifically, they can be used in video amplifiers operating at frequencies through 30 MHz, AM and FM if amplifiers, and buffer amplifiers in which an isolation capability greater than 60 dB at 1 MHz is desired.

ICAN-5380 . . . . 7 pages
Integrated - Circuit Frequency - Modulation if Amplifiers

The discussion in this Note shows that the simplest approach to the use of the CA3012 and CA3028 integrated circuits in FM if-amplifier strips is to replace each stage in present discrete-transistor if strips with a differential amplifier. This integrated-circuit approach requires a minimum of re-engineering because a cascade of individually tuned if stages is used. From a performance point of view, this approach results in better AM rejection than that obtained with discrete circuits because of the inherent limiting achieved with the differential-amplifier configuration.

ICAN-5766 . . . . 8 pages
Application of the RCA-CA3020 and CA3020A Integrated-Circuit Multipurpose Wideband Power Amplifiers

The CA3020 and CA3020A integrated circuits are multipurpose, multifunction power amplifiers designed for use as power-output amplifiers and driver stages in portable and fixed communications equipment and in ac servo-control systems. The flexibility of these circuits and the high-frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video amplifiers, and video line drivers. Voltage gains of 60 dB or more are available with a 3-dB bandwidth of 8 MHz. Applications covered include audio, wideband, and driver amplifiers.

ICAN-5831 . . . . 5 pages
Application of the RCA-CA3044 and CA3044V1 Integrated Circuits in Automatic-Fine-Tuning Systems

This Note describes the use of the CA3044 and CA3044V1 integrated circuits as automatic fine-tuning (AFT) system components and discusses the advantages of integrated circuits in this application. The CA3044V1 is electrically identical to the CA3044, but is supplied with formed leads for easier printed-circuit-board mounting. The construction and performance of a typical automatic-fine-tuning system for a color television system are examined.

ICAN-5841 . . . . 4 pages
Feedback-Type Volume-Control Circuits for RCA-CA3041 and CA3042 Integrated Circuits

This Note describes feedback-type volume controls for use with RCA-CA3041 and CA3042 integrated circuits in television receivers. In television sets using these integrated circuits, the volume control is often located remote from the amplifier. The long leads required in such a configuration sometimes pick up undesirable signals that, in turn, cause the system to exhibit hum and noise at low volume levels. The proposed feedback-type volume control reduces hum and noise pick-up by reducing the gain of the system rather than the signal level, and thus eliminates the cost of shielding the leads.

ICAN-6259 . . . . 10 pages
Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Demodulator

The CA3090AQ integrated-circuit provides features heretofore unavailable to the receiver designer. This device needs only a single tuning adjustment, which reduces to a minimum the manual effort during assembly; the phase-locked loop maintains performance under conditions of temperature variations, humidity, and aging. The compactness of the CA3090AQ and of the required external components, added to the other attributes, makes this stereo decoder a significant advancement in the state of the art of stereo decoder designs.

ICAN-6302 . . . . 9 pages
Description and Application of the RCA-CA3120E Integrated-Circuit TV-Signal Processor

The CA3120E is a 16-pin, dual-in-line-monolithic-silicon integrated circuit that processes a video signal and provides the following outputs: non-inverted video output; noise-processed, inverted video output; dual-polarity, composite synchronization signals; and automatic gain-control signals (agc). The IC, which can be used in color or monochrome TV receivers, requires a single-polarity power supply (positive) and includes impulse noise inversion and delay circuits that reduce the deleterious effects of impulse noise in the receiver agc and synchronization (sync) circuits. Standard agc strobing techniques are also used. The agc and impulse-noise thresholds are automatically set and require no controls. The if maximum-gain bias and the tuner agc delay may be adjusted for optimun. TV-receiver performance; the time constant for the sync-separator input can also be optimized by the set designer.

ICAN-6724 . . . . 8 pages
A Flexible Integrated-Circuit Color Demodulator for Color Television

This Note describes the circuit operation and application of the CA3067 in a color television receiver. The CA3067, which is supplied in a quad-in-line 16-lead plastic package, provides the following color-demodulator circuit functions: amplification, balanced chroma demodulation, dc-operated tint (phase) control, and zener-diode voltage regulation.

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